MODELING AND PERFORMANCE ANALYSIS OF DUAL MATERIAL DOUBLE GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

THIS THESIS IS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

HIMELI CHAKRABARTI

MZU REGN NO : 1800282

PH.D REGN NO : MZU/PH.D./1287 of 27.07.2018

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SCHOOL OF ENGINEERING AND TECHNOLOGY

SEPTEMBER 2021

MODELING AND PERFORMANCE ANALYSIS OF DUAL MATERIAL DOUBLE GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

BY

HIMELI CHAKRABARTI
Department of Electronics & Communication Engineering

Name of Supervisor : Dr. Niladri Pratap Maity

Submitted

In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Electronics and Communication Engineering of Mizoram University, Aizawl

Department of Electronics and Communication Engineering
School of Engineering and Technology
MIZORAM UNIVERSITY
(*A Central University*)
Tanhril**,** Aizawl – 796 004, Mizoram

CERTIFICATE

This is to certify that the thesis entitled "**Modeling and Performance Analysis of Dual Material Double Gate Metal Oxide Semiconductor Field Effect Transistor"** submitted to Mizoram University for the award of the degree of **Doctor of Philosophy Electronics and Communication Engineering** by **Himeli Chakrabarti**, Ph.D. Registration No. **MZU/Ph.D./1287 of 27.07.2018**, is Ph.D scholar in the Department of Electronics and Communication Engineering, under my guidance and supervision and has not been previously submitted for the award of any degree in any Indian or foreign University. She has fulfilled all criteria prescribed by the UGC (Minimum Standard and Procedure governing Ph.D. Regulations). She has fulfilled the mandatory publication (Publication enclosed) and completed Ph.D. course work. It is also certified that the scholar has been admitted in the Department through an entrance test, followed by an interview as per UGC Regulation of 2016.

Date: September, 2021
Place : Aizawl

(Dr. Niladri Pratap Maity)
Supervisor

MIZORAM UNIVERSITY
Aizawl -796 004

September 2021

DECLARATION

I, Himeli Chakrabarti, hereby declare that the subject matter of this thesis entitled "**Modeling and Performance Analysis of Dual Material Double Gate Metal Oxide Semiconductor Field Effect Transistor"** is the record of work done by me, that contents of this thesis did not form basis of the award of any previous degree to me or to do the best of my knowledge to anybody else, and that the thesis has not been submitted by me for any research degree in any other University/Institute.

This is being submitted to the Mizoram University for the degree of Doctor of Philosophy in **Electronics and Communication Engineering.**

Date:

(Himeli Chakrabarti)
Candidate

(Dr. Niladri Pratap Maity)
Supervisor

(Dr. Niladri Pratap Maity)
Head of the Department

Acknowledgement

At the outset, I express my gratitude to the almighty God for his grace, which has enabled me to complete my task successfully. I wish to express my heartfelt gratitude to my supervisor and mentor **Dr. Niladri Pratap Maity,** the Head of Department of Electronics and Communication Engineering, MZU, for his constant support, guidance, encouragement and patience throughout my research work. I am also thankful to **Dr. Reshmi Maity**, Associate Professor, for extending all the facilities. I am also thankful to all the faculties and technical staff of the department for their help, support and kind cooperation.

I would like to express my deepest gratitude to **Pulak Mazumder**, HOD of ECE department and all colleagues of Regent Education and Research Foundation Group of Institutions for their kind support, without whom, this work would not have been possible.

I would like to express my deepest gratitude to my colleagues, **Avik Ghosh Dastidar**, **Dr. Rajdeep Chakravarty**, **Dr. Anindita Das**, **Dr. Dipankar Biswas** and **Suparna Panchanan** for providing opportunity and constant support so that I can manage my responsibilities in my working sector and do my research work to complete Ph.D. I am grateful to **Dr. Moumita Pal** for her recommendations and assistance, which have aided me in numerous parts of my job.

Also, I would like to thank my parents, **Sitanshu Narayan Chakrabarti** and **Madhumita Chakrabarti**, parents in law, **Baidyanath Saha** and **Purabi Saha**, husband, **Partha Saha**, daughter **Doivangee Saha** and son **Deeptagni Saha** for their constant support, love and prayers. Last but not the least; I place on record, my sense of gratitude to one and all who, directly or indirectly, have lent their helping hand in this venture.

HIMELI CHAKRABARTI

Table of Content

List of Figures

List of Tables

CHAPTER

1

Introduction

1.1 . Overview of MOSFET

"A technological innovation is like a river- its growth and development depending on its tributaries and on the conditions it encounters on its way. The tributaries to an innovation are inventions, technologies and scientific discoveries, the conditions are the vagaries of the market-place." - Ernest Braun and Stuart Macdonald (Schaller, 2004).

During World War II, the researchers realized the importance of semiconductor technology in the communication system. They also noticed the importance of silicon, germanium materials in the device structure. Around the year 1940 Teal and Gordon invented p-type and n-type semiconductors by applying impurities to the extrinsic ones. Down the path, following the vacuum tube, diode, the bipolar transistor was invented in 1947 (Fig. 1.1). After that silicon on insulator metal oxide semiconductor field effect transistor (SOI MOSFET) was first demonstrated by Mohamed Atalla and Dawon Kahng of Bell Labs in the year 1960 (Kahng, 1976). Today it has become the most important device in the integrated circuit (IC) design (Neaman). The invention of the microprocessor in the year 1971 was a milestone of this technology. Nowadays all the automation industries depend on microprocessors and microcontrollers. After inventing the complementary MOS technology the total electronic world started its journey to the very large scale integration (VLSI) era. The total evaluation path describes in Fig. 1.1.

MOSFET is a planner semiconductor structure with four contacts named source (S), drain (D), gate (G) and body (B) or substrate as represented in Fig. 1.2. The doping concentration of the source and drain regions are the same and that is opposite to the

substrate region. Thus a depletion region is established between source, drain and substrate junction. Source terminal serves as the source of carriers (holes or electrons).

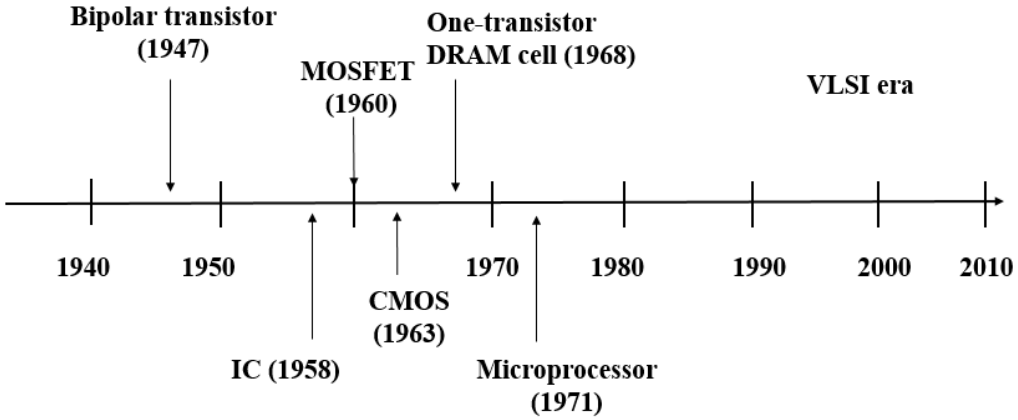

FIGURE 1.1. A brief chronology of the development in VLSI (Ghosh, 2013)

The drain terminal collects the carriers flown from the source through the channel. The gate terminal has total controllability over the channel formation and on the performance of the MOSFET by application of the bias. Depending on the channel formation, the MOSFET is of two types, (a) enhancement mode and (b) depletion mode. In enhancement mode, the channel is formed electrically on account of applied voltage at the gate terminal and in depletion mode, the channel is formed physically by manufacturing a physical layer between the source and drain (Tsividis, 1987). In the case of enhancement type MOSFET when the gate voltage reaches up to threshold voltage, the minority carriers are accumulated below the oxide region. Thus forming a conducting medium called a channel.

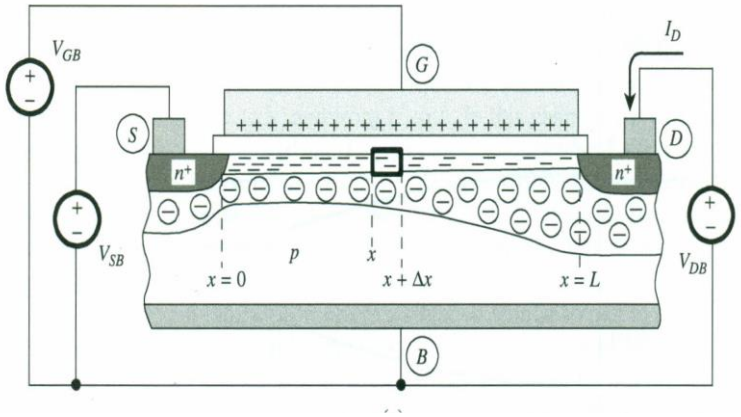

FIGURE 1.2. Cross-sectional view of a 4 terminals planar MOSFET (Tsividis, 1987)

This phenomenon is called inversion. Depending on the gate biasing, the channel transfer from the weak inversion mode to strong inversion. Also, the concentration of the minority carriers increases at the channel region during this period. Hereafter, on the application of drain-source biasing, the minority carriers move and start conducting, called drain current. Before reaching the threshold voltage channel is not formed and the current does not conduct. At this time the MOSFET is in 'OFF' state and the mode is called subthreshold. When the current starts to flow, at that time the MOSFET is in 'ON' condition (Streetman & Banerjee, 2006). A cross-sectional view of MOSFET has been represented in Fig. 1.2 with its four terminals. It has a p type substrate with n type doped source and drain. Due to p-n junction, a depletion region has been formed. On application of reverse bias voltage at the gate terminal, minority carriers are accumulated below the oxide level and formed a channel like formation. Through this channel drain current flows from drain to source on account of proper source-drain bias.

In the present technology, the MOSFET is the chief factor of advancement because of several advantages over others. Simple applications, planar structure easy to fabricate, less power consumption, high packing density, immunity to short channel effects (SCEs) and high switching speed are few among them. The high switching capability from off to on state and the proficiency during the low voltage operation make it a unique device.

1.2. Sketch on MOSFET- Scaling

In the year 1965, researcher and co-founder of Intel Corporation, Gordon Moore stated in his research paper, "Cramming more components onto integrated circuits" (Moore, 1998) that the number of transistors per chip would become double every year and that trend will continue for at least next ten years. Later on, in 1975 he slightly modified his statement and predicted that the component count per chip will be double twice the year (Moore, 2006). The prediction is illustrated as graphical representations in Fig. 1.3. It illustrated the number of components required for integrated function in log form with respect to the year. The representation clearly shows that while it required 1 or 2 components in 1960 it went up to 16 components in only 15 years. Initially, this prediction was based on 50-60 component chips and thought that this will

continue up to 1980 (Faggin et al., 1996; Moore, 1975). But this trend line continues till now in the semiconductor industry and it is so popular to gain the status of a "LAW".

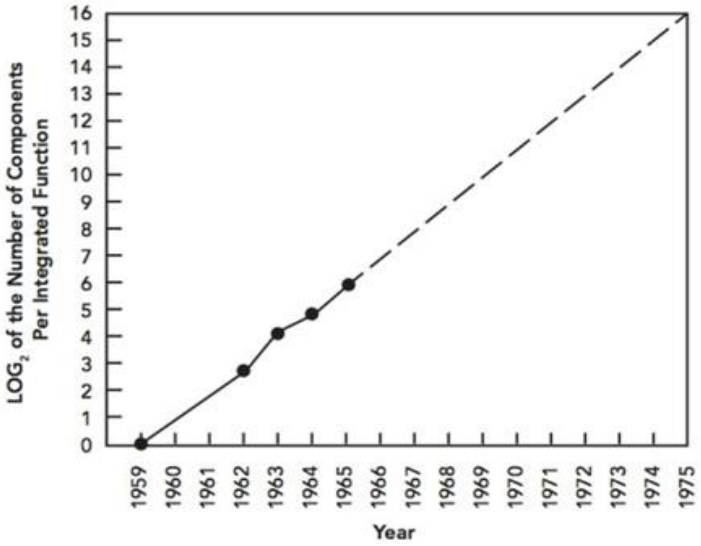

FIGURE 1.3. Moore's original 1965 Graph (Dennard, 1974)

Recent trends in the semiconductor industry according to the law have been depicted in Fig. 1.4. It shows the number of components required in the advanced microprocessor and microcontroller technology starting from 1970 to now. Later Intel executive David House modified the law a little bit. He foretold that the chip performance would double every 18 months. In 1971, the first microprocessor on IC, Intel's 4004 was fabricated. The device has 16 pins and contained 2300 transistors (Plummer, 2001; Faggin, 1996). Nowadays Intel launches a microprocessor that contains nearly 2-billion components on a chip. Consequently, the component size becomes smaller approximately in every alternative year so that they can be housed in the small space. As per Moore's law (Moore, 1975), the transistor dimension is reduced by a factor of 0.7 in each technological generation (Plummer & Griffin, 2001). Recent trends of the dimension of the channel length of transistors present in the device over the year are illustrated in Fig. 1.5. The scaling of the components to smaller dimensions generates several advantages such as improve packing density, low standby power, low operating power, high performance and high speed, etc. As a result, the cost per transistor is reduced, the device can perform a more complex function and switching time is reduced. The scaling down process is represented in

Fig. 1.6. With due respect to the scaling effect, every geometrical dimension of the device like channel length, width, oxide thickness, doping concentration of substrate even applied voltage has been scaled down to a factor.

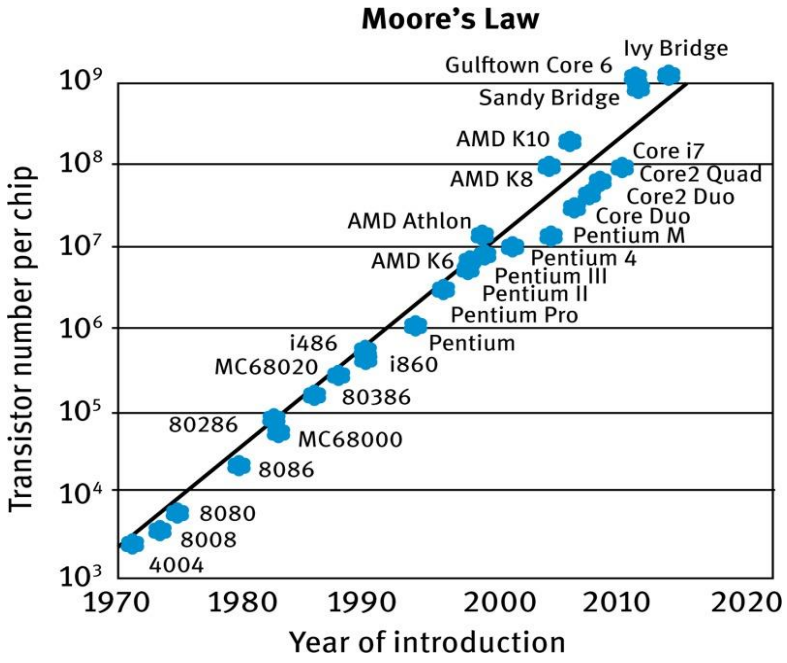

FIGURE 1.4. Recent trends in semiconductor industry according to Moore's law (Wikipedia)

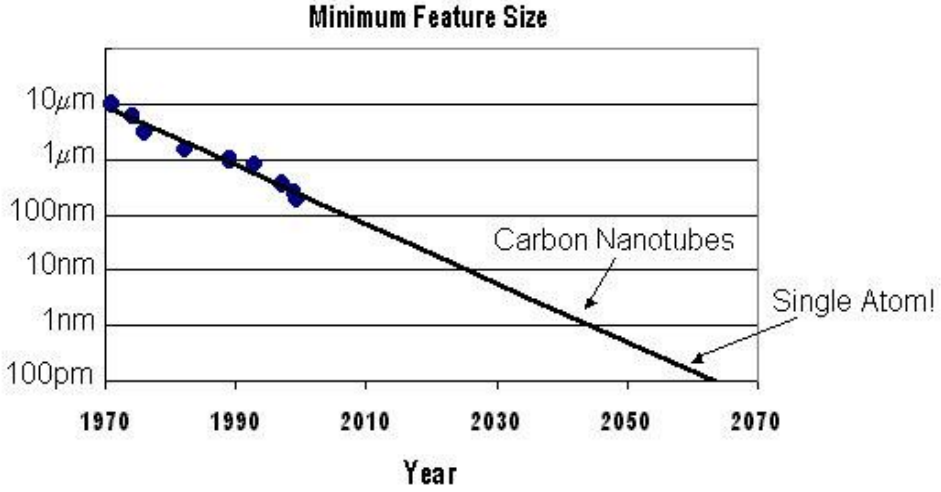

FIGURE 1.5. Component size over the time period (Wikipedia)

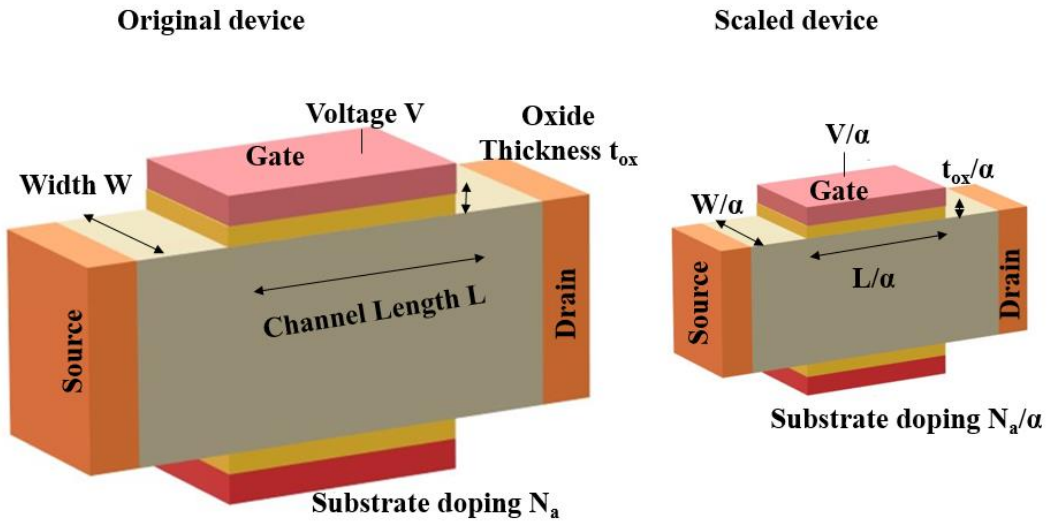

FIGURE 1.6. Scaling down process (Buvaneswari, 2019)

For scaling down, several other structural parameters have to decrease to work properly. There are two types of scaling process namely constant voltage scaling and constant field scaling. Due to constant voltage scaling, the lateral dimensions such as channel length, width are scaled down and it is a purely geometrical process. However, several SCEs have been introduced for it. In the case of constant field scaling (Dennard et al., 1974), the vertical dimensions such as source-drain junction depth, oxide thickness, power supply voltage, etc. are scaled-down and this is not a geometrical process. In the last 50 years, the channel length declines from a few hundred micrometres to the sub 20 nm range. Effectively the device faces low threshold voltage and high off current.

1.3. Limitations of Scaling Effects

The required device dimensions for high performance MOSFET over the years are represented in Table 1.1 (Hoefflinger, 2011; Zeitzoff & Chung, 2005). International technology roadmap for semiconductor (ITRS) report on 2003 conveyed that the new advancement in the device technology requires at about 1 nm oxide thickness range. Due to scaling down of the gate oxide thickness, it fails to perform as an insulator and a huge amount of charged particles starts to move through the channel region. It boosts the motion of the current across the channel. Frequently it goes up to 1A leakage current. This is sufficient to damage the device. Moreover, this current cannot be measured with the drain current (Hoefflinger, 2011).

Below 1.2 nm oxide thickness the quantum mechanical tunneling effect increases, accordingly a huge amount of gate leakage current flows through the gate region (Frank et al., 2001; Garduño et al., 2011; Orouji & Rahimian, 2012). Due to the excess tunneling current, the gate oxide material SiO_2 breaks down. Resultantly power loss and power dissipation increase and produces surplus heat of the device (Garduño, 2011).

Table 1.1. Required dimensions for high performance over the year

Year of Production	Technology Generation	Physical Length	EOT	Inversion Layer Thickness	Gate Dielectric Thickness	Maximum Gate Leakage Limit	Power Supply Voltage	Saturation Threshold Voltage	Sub Threshold Slope Adjustment Factor (Full depleted DG)	Source/Drain Subthreshold off-state Current	Mobility Enhancement Factor
Units		nm	Å	Å	Å	A/cm^2	V	V		µA/µm	
2003		45	13	8	21	2.20E+02	1.2	0.21	1	0.03	1
2004	hp90	37	12	8	20	4.50E+02	1.2	0.2	1	0.05	1.3
2005		32	11	7	18	5.20E+02	1.1	0.2	1	0.05	1.3
2006		28	10	7	17	6.00E+02	1.1	0.21	1	0.05	1.4
2007	hp65	25	9	4	13	9.30E+02	1.1	0.18	1	0.07	2
2008		22	8	4	12	1.10E+03	1	0.17	0.8	0.07	2
2009		20	8	4	12	1.20E+03	1	0.16	0.7	0.07	2
2010	hp45	18	7	4	11	1.90E+03	1	0.15	0.6	0.1	2
2012		14	7	4	11	2.40E+03	0.9	0.14	0.5	0.1	2
2013	hp32	13	6	4	10	7.70E+03	0.9	0.11	0.5	0.3	2
2015		10	6	4	10	1.00E+04	0.8	0.12	0.5	0.3	2
2016	hp22	9	5	4	9	1.90E+04	0.8	0.1	0.5	0.5	2
2018		7	5	4	9	2.40E+04	0.7	0.11	0.5	0.5	2

Boron that has been used to produce p type material, penetrates from the p^+ polysilicon gate to the channel which enhances the detrimental impact of polysilicon depletion in the polysilicon gate region. The mobility of free carriers in the channel at inversion mode will not be sufficient to reach the required transistor performance (Yeo et al., 2003; Zeitzoff & Chung, 2005). With the scaling down of channel length, declining

from 45 nm in 2003 to 7 nm in 2018 (Schaller, 2004) increases the line edge roughness which has encountered a great challenge for the device performance.

1.4. Short Geometry Effects due to Scaling

A semiconductor device is considered to be short when the device length is comparable with a depth of source/drain junction (X_j) and depletion layer width (X_{sd}) for source depletion region and (X_{dd}) for drain depletion region. The matter represents in Fig. 1.7. The effects are classified into two types (Das, 2015)

(i) Short channel effects

(ii) Narrow channel effects

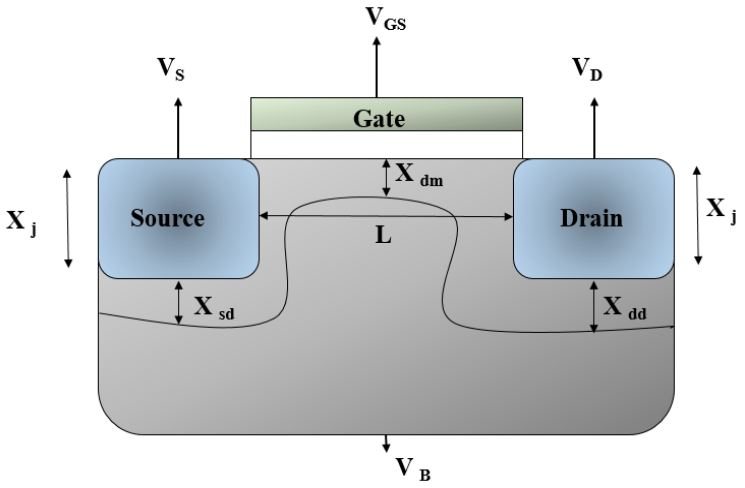

FIGURE 1.7. Cross sectional view of MOSFET with depletion region (Ghosh, 2013)

1.4.1. Short Channel Effects (SCEs)

When the channel length is comparable to the source-drain junction then it is called a short channel. However, different SCEs engender due to shortening the device dimensions are discussed below (Chaudhry & Kumar, 2004; Young, 1989).

1.4.1.1. Threshold Voltage Roll Off

The depletion region charge in the channel is not created totally by the gate voltage. It is also controlled by the drain voltage specifically near the drain end. As a result, the depletion region charge which is created solely for gate voltage is reduced

by the application of drain voltage. Therefore, the threshold voltage is reduced. This effect is not only valid for short channel devices, it is applicable for long channels also. However, at the long channel, this effect can be ignored because here the amount of charges that have been generated for drain voltage is negligible (Das, 2015). Reduction or roll off nature of threshold is not desirable for any device, because for this small geometrically scaled devices can be reached to 'ON' condition at a very small gate voltage value. The depletion charge is monitored by gate voltage as well as drain voltage is shown as the triangular region in Fig. 1.9. It represents the influences of drain, source and gate terminals over the depletion region.

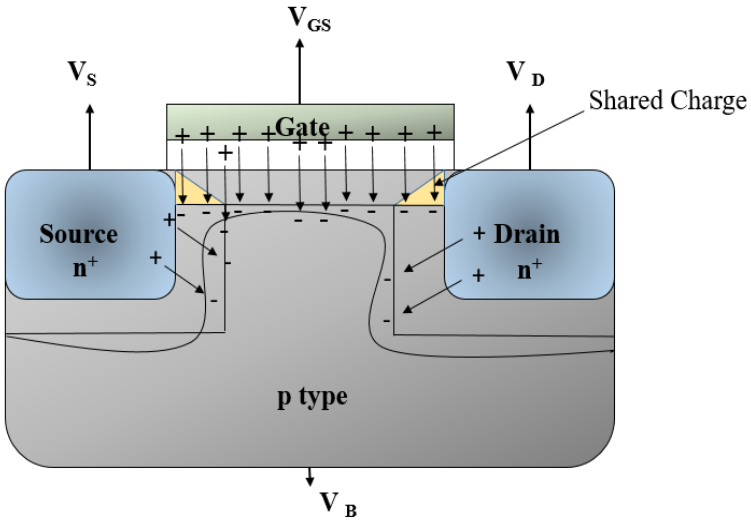

FIGURE 1.8. Cross sectional view of MOSFET with depletion charge sharing (Dhiman, 2018)

1.4.1.2. Sub threshold Swing (SS)

Before reaching the threshold voltage, at weak inversion mode, some amount of minority carriers are accumulated below the gate and formed a channel. As a result, before reaching the 'ON' condition mode, a small amount of current will flow through the channel. This current is called subthreshold current because before reaching the threshold voltage it flows. This can be measured analytically by the slope of the log of drain current with gate voltage (Tosaka et al., 1994),

$$S = \frac{dV_{GS}}{d(\log I_D)} \tag{1.1}$$

Here, S represents SS, V_{GS} is the gate to source voltage and I_D is the drain current.

1.4.1.3. Drain Induced Barrier Lowering (DIBL)

At small geometry conditions, the source and the drain regions come close together and their depletion regions approach each other. Consequently potential barrier decreases, electrons easily cross the potential barrier and carrier concentration in the channel increases. In this situation, if the drain voltage increases the drain field penetrates to the source and further decreases the barrier. This phenomenon is called 'DIBL' (Lee et al., 2010). The variation of conduction energy band edge changes its position with drain-source voltage V_{DS} is represented in Fig. 1.9. (Tsividis, 1987). At equilibrium condition, when V_{GS} is equal to flat band voltage and for $V_{DS} = 0$ V the variation of conduction band edge is represented in Fig. 1.9 (a). However, on the application of high V_{DS}, the conduction band edge decreases Fig. 1.9 (c). Lowering the band edge is the effect of V_{DS} and the difference between the two conduction bands are represented as DIBL.

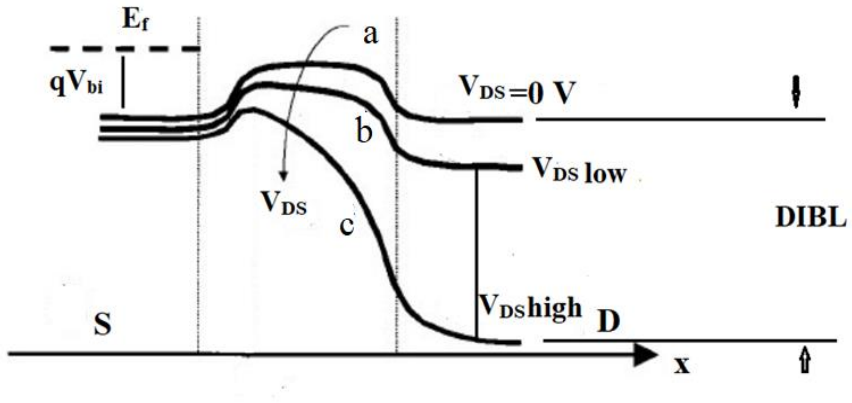

FIGURE 1.9. Conduction energy band edge at the surface along longitudinal direction for short channel MOSFET (a) V_{GS} equal to flat band voltage and V_{DS} is 0V, (b) Strong inversion mode, (c) strong inversion with large V_{DS} (Tsividis, 1987)

1.4.1.4. Channel Length Modulation (CLM)

At the saturation region, the effective channel length (ΔL) of the MOSFET is decreased from the actual channel length (L). This is occurred due to 'pinch off' and it is a function of drain to source voltage. In long channel MOSFET, this reduction of

the channel length becomes insignificant but for small scale channel length, this reduction has to be considered. This is called CLM (Das, 2015), expressed as,

$$\Delta L = L \ln\left(1 + \frac{\left(V_{DS} - V_{DS,sat}\right)}{V_{pp}}\right) \tag{1.2}$$

Here, V_{DS} is drain-source voltage, $V_{DS,sat}$ represents saturation voltage and V_{pp} is pinch off voltage. The pinch off voltage is represented in Fig. 1.10 where the channel length touched the oxide surface and it can be represented by the difference between V_{GS} and threshold voltage V_{th}. In small dimension devices, this effect enhances to block the channel length and reduces I_D.

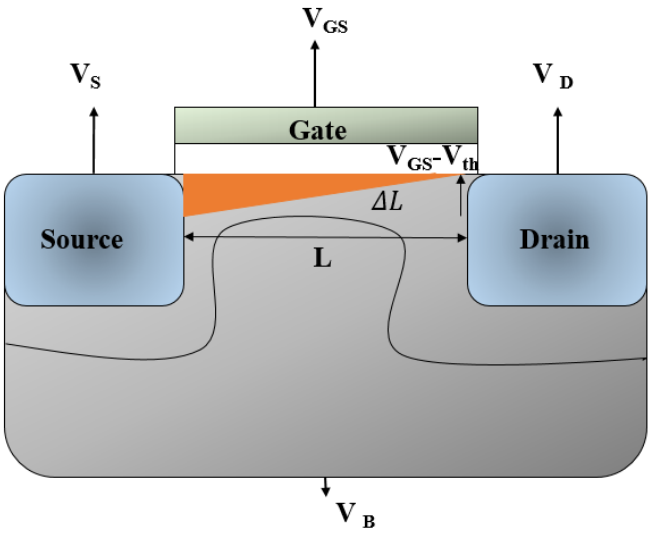

FIGURE 1.10. Schematic representation of CLM (Ghosh, 2013)

1.4.1.5. Velocity Saturation

The drift velocity of the carrier increases with the increasing value of the electric field. But at a very high value of the electric field, this becomes saturates. This phenomenon is called velocity saturation. In a small scale MOSFET, this velocity saturation occurs at an earlier stage than a long scale device. This will reduce the 'ON' state condition of the MOSFET.

1.4.1.6. Gate Oxide Leakage

Due to scaling down the MOSFET, the insulator oxide thickness goes to the 2 nm range. At this thickness level, silicon dioxide (SiO_2) won't be able to perform as

good dielectric material and increases the gate tunneling current (Haensch et al., 2006). Different types of tunneling currents are represented in Fig. 1.11. The free charged particles directly penetrate the oxide level and go to the gate terminal from the source end and generate gate-source tunneling current $\left(I_{gs}\right)$, whereas the current flow between drain and gate terminal due to movement of the charged carrier from gate to drain is called gate-drain tunneling current $\left(I_{gd}\right)$. However, some of the carriers directly move to the channel and generate tunneling current $\left(I_{gc}\right)$. These currents cannot contribute to drain current and damage the device. Using high-k material this problem can be overcome.

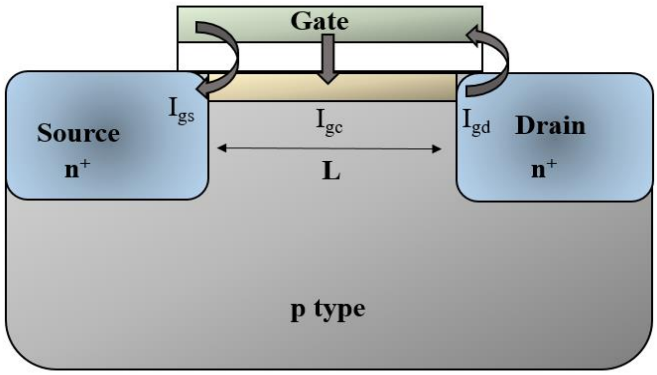

FIGURE 1.11. Schematic diagram of gate oxide tunnelling (Buvaneswari, 2019)

1.4.2. Narrow Channel Effects

When the channel width is comparable to depletion region thickness then the device is called a narrow channel device. The narrow channel width of the MOSFET generates some effects that are discussed below (Das, 2015).

1.4.2.1. Gate Induced Drain Leakage (GIDL)

Normally, MOSFET will be at 'ON' condition after reaching the threshold voltage and that voltage is a function of gate voltage. So when the gate voltage is zero generally n-channel MOSFET will be in an 'OFF' state. However, on account of high drain voltage, the narrow width of the depletion region and band bending, a leakage current will flow. This current is known as GIDL (Tsividis, 1987). The generated

electron-hole pair that have been created due to high drain voltage and causes of leakage current is depicted in Fig 1.12. Numerous electron-hole pairs are generated and they move to the substrate by penetrating the depletion region. This is the cause of the GIDL leakage current.

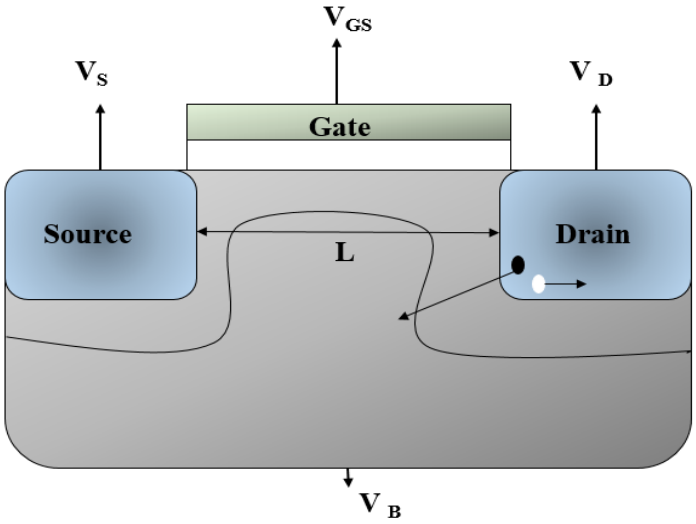

FIGURE 1.12. Schematic diagram of GIDL effect (Ghosh, 2013)

1.4.2.2. Fringing Field Effects

Due to the reduction of device length and width the gate region is overlapped with the source and drain. So that the electric lines have become dense at the sidewall region of the channel. These lines help to increase the concentration of free charge particles in the channel and have a great impact on the device's performance. This phenomenon is called the fringing field effect (Han & Ferry, 1998). Fig. 1.13 illustrates different fringing lines that have been generated in the case of short channel MOSFET. These lines directly affect the channel performance.

1.4.2.3. Hot Carrier Effects (HCEs)

The MOSFET dimensions are scaled quite faster than the supply voltage. As a result, the horizontal and vertical parts of the electric field in the channel region increase. A higher electric field provides high kinetic energy to the free particles (hot holes and electrons). These hot carriers are injected into the gate oxide and affect the oxide interface charge distribution, current-voltage characteristics of the MOSFET. Some pictorial representation of HCEs is illustrated in Fig. 1.14 (Garrigues & Belland,

1986; Takeda, 1984). Due to high kinetic energy, several electron-hole pairs are generated and are injected into gate, drain or source terminal.

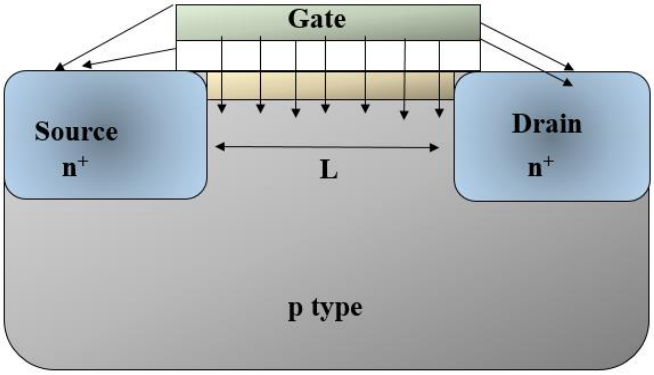

FIGURE 1.13. Cross sectional view of short channel MOSFET with fringing lines (Dhiman, 2018)

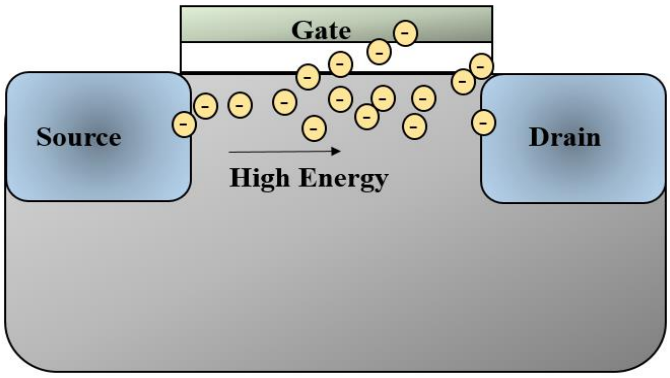

FIGURE 1.14. Cross sectional view of MOSFET with hot electrons (Ghosh, 2013)

1.4.2.4. Impact Ionization

The primarily generated hot carriers collide with other atoms and generate new electron-hole pairs. This process is called impact ionization. The primary and secondary electrons both take part in the flow of drain current whereas the holes that are generated by the impact ionization flow into the substrate and generate substrate current (I_b) as in Fig. 1.15. This current is monitored by the heating effect of the device and drain electric field. The high value of substrate current increases the probability of circuit breakdown (Reddy & Kumar, 2005).

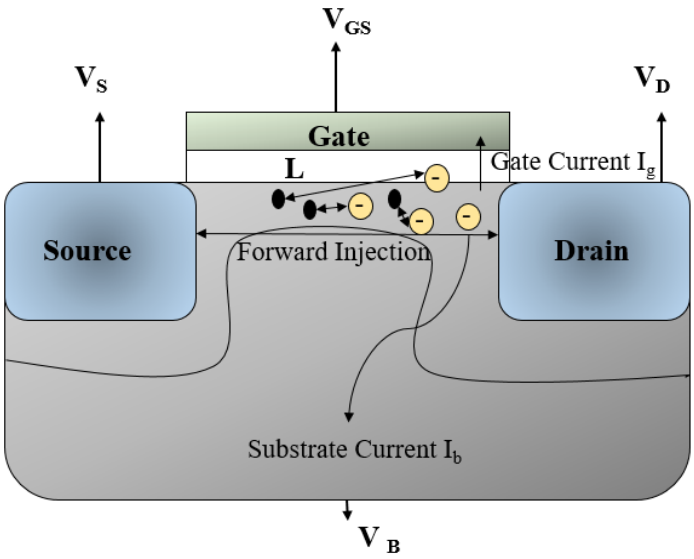

FIGURE 1.15. Cross sectional view of MOSFET showing impact ionization (Ghosh, 2013)

1.4.2.5. Parasitic BJT Effect

The depletion region between source-drain and substrate generates capacitance and resistance effects. In a narrow channel, these parasitic effects become so high that they decrease the driving capability and switching speed of the device (Reddy & Kumar, 2005).

Several exclusive architectural changes have been introduced in the planar structure MOSFET to overthrow these problems. Gate engineering aspects, gate material engineering, oxide material engineering are few among them. Instead of using classical planar structure, two-dimensional or three-dimensional structures with multiple gates emerges the MOSFET technology into a new dimension. These ideas also give practical solutions to the problems. The different multiple-gates structures that have been used to fabricate the MOSFET for better performance are explained in Fig. 1.16 (Colinge et al., 1990). In this figure, several MOSFET structures with different dimensions have been shown and compare with one-dimensional planar MOSFET. Instead of using one gate, researchers use double gate structures like gate all around (GAA), multiple independent gate field effect transistor (MIGFET), double gate fin field effect transistor (FINFET) to overcome the SCEs. Among triple gate structures, trigate field effect transistor (FET), Π gate, Ω gate, triple gate FINFET are renowned. These structures will provide better coverage over the channel due presence

of three gates. In the surrounding gate structure i.e cylindrical gate, quadruple gate FET covers the channel throughout all the directions. For better coverage of gate voltage, the effects of SCEs reduce.

1.5. MOSFET Technology-Evaluation

Instead of using a single gate structure, many multi-gate (MuG) MOSFETs like double gate (DG), trigate (TG) and surrounding gate (SG) structures are proposed as an alternative structure over bulk MOSFET (Colinge, 2004). The double gate (DG) structure is the simplest of all MuGs. In 1967, Farrah and Steinberg of Bendix Corporation first proposed the concept of the double-gate transistor followed by Sekigawa of ETL the concept of DG MOSFET in 1980 (Farrah & Steinberg, 1967). In this structure, the channel gets covered from top to bottom by the gates. The presence of two gates gives better coverage over the small channel. On application of gate voltage from both sides of the device, the channel changes to inverting mode easily. With the better coverage of gate voltage over the channel, the uncontrolled leakage current flow is reduced. Thus this planar structure helps to reduce SCEs, improves punch through properties and also reduces the capacitance generated at the junctions (Nakagawa et al., 2003). The schematic view of DG MOSFET is represented Fig. 1.17. Two gates are represented by a grey colour on the top and at the bottom of the device. They are also called the top gate and bottom gate. Below the gates oxide layer has been fabricated showing by yellow colour representation.

In view of gate material engineering, dual material gate (DMG) architecture is another unique model used to diminish the problems of SCEs (Kumar & Chaudhry, 2004). Fig. 1.18 represents the schematic view of DMG. In this architecture, the gates are made up of two different materials with non-identical work functions such as polysilicon. In the preferred structure, the gate near the source side is used high work functioned p^+ polysilicon material and low work functioned n^+ polysilicon material is used at the gate near the drain side. Due to the dissimilarity of work function materials assembling at the gate junction, a voltage drop has been introduced. As a result, two different lobes with different values are generated at the surface potential. The generated potential profile of the surface region is modified to increase the efficiency of electron transport. The lower surface potential is generated under high work

functioned gate material and a higher one is generated under low work functioned polysilicon material.

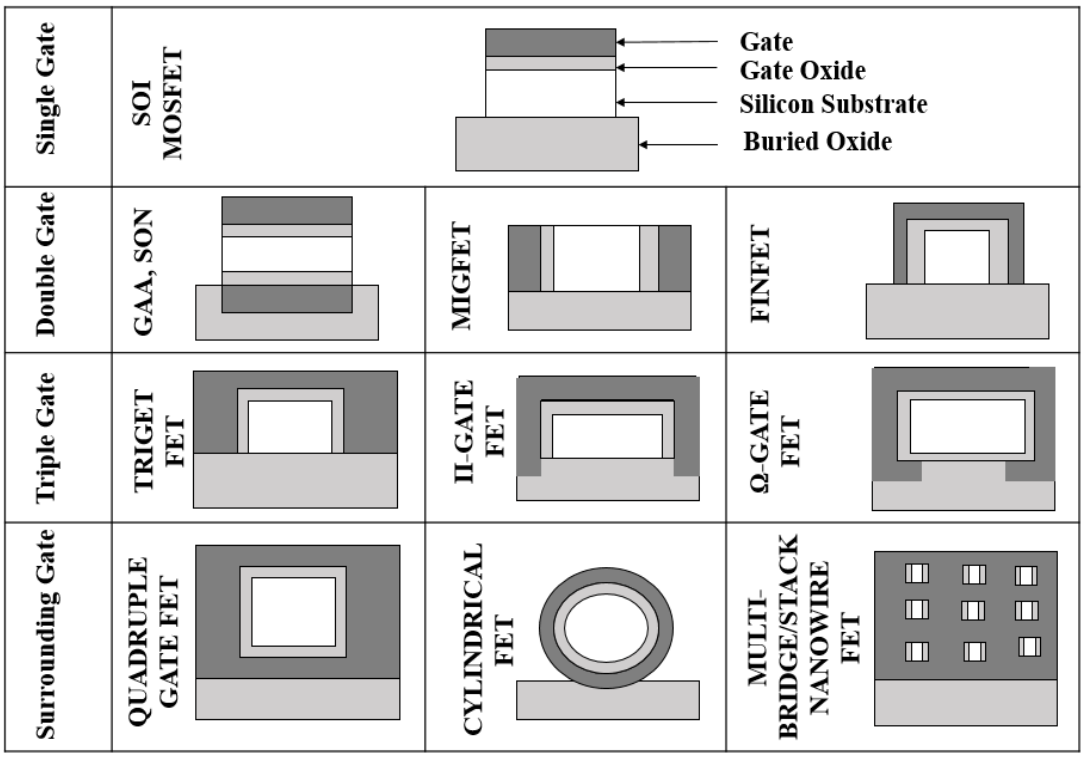

FIGURE 1.16. Possible devices with multi-gate structure (Buvaneswari, 2019)

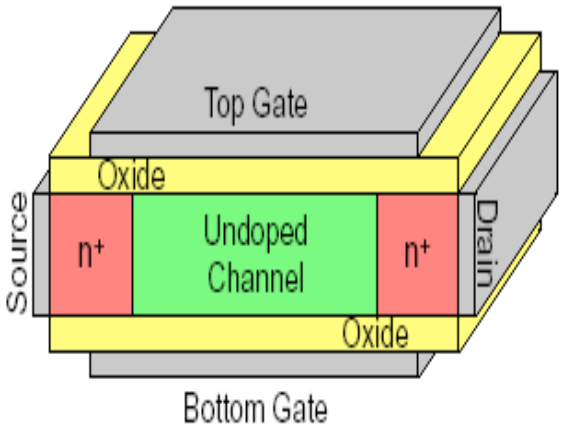

Figure 1.17. Schematic representation of DG MOSFET (Ghosh, 2013)

Consequently, a step function like formation has been generated. The generated threshold voltage has a low value under the first gate (near the source end) than under the second gate (near the drain end). This feature helps to increase the transportation

effectiveness of the gate. At the gate junction, the surface potential, as well as the electric field, are also adjusted according to the manner. The average lifetime of the DMG device is increased by the increment of the electric field under the gate terminal. However, due to using different work functions polysilicon materials, the step like function has been generated in the surface potential and electric field. The presence of two different lobes helps to reduce the SCEs (Kumar & Chaudhry, 2004; Saxena et al., 2002).

A unique planar model naming dual material double gate silicon on insulator (DMDG SOI) MOSFET structure is engendered in combination with these two structures. This architecture integrates the advantages of two different structures stated above.

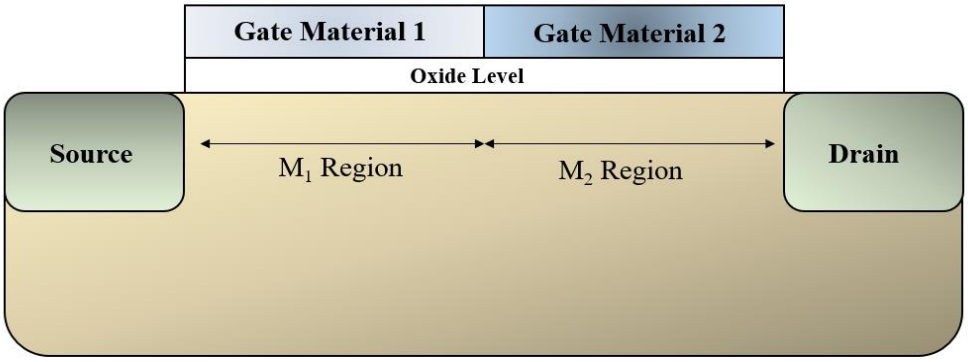

Figure 1.18. Schematic representation of DMG MOSFET (Ghosh, 2013)

1.5.1. Concept and Operation of Dual Material Double Gate SOI MOSFET

DMDG SOI MOSFET structure is superior to the common planar MOSFET structure. It is formed by merging the DG and DMG concepts. It has two gates at the top and the bottom, whereas the gates consist of two different polysilicon materials of different work functions. Subsequently, the drain conductance, as well as the SCEs and DIBL reduces and the drain potential variation increases due to the presence of step function characteristics in the surface potential and electric field over the channel region. Reduction of the highest value of the electric field than other devices helps to generate uniformly extended drift velocity of the free carrier along the channel,

decreases the hot carrier effects and improves drain breakdown voltages. It has a higher transconductance value which helps to reduce SCEs and enhances the voltage gain. DMDG SOI MOSFET structure with all these physical aspects upgrades itself as a major topic to the research candidates for future technology (Reddy et al., 2005; Goel et al., 2016; Kaur et al., 2008).

Schematic representation of fully depleted DMDG structure has been shown in Fig. 1.19. In this research work, different physical attributes like surface potential, electric field, threshold voltage and drain current are analysed of this structure. It has two gates at the top and bottom, where the top gate contains two different materials p^+ polysilicon and n^+ polysilicon. However, the bottom gate consists of only one material (n^+ polysilicon). An oxide material present between gate and substrate to serve the dielectric medium. The thickness of the oxide material for top and bottom gates are same. The total channel length is divided into two equal parts so that the particular effects of different gate materials can be studied. Simultaneously, silicon dioxide (SiO_2) and high-k materials are used as gate oxides for the comparative analysis. It has two different values of surface potential and electric field for two different region. Two different types of threshold voltages are also generated due to presence of two surface potentials. However, using high-k material, it generate low value of surface potential. The slope of the surface potential near the drain side increases with high-k. This also helps to decrease the SCEs. Details analytical features and its characteristics are studied in this research work.

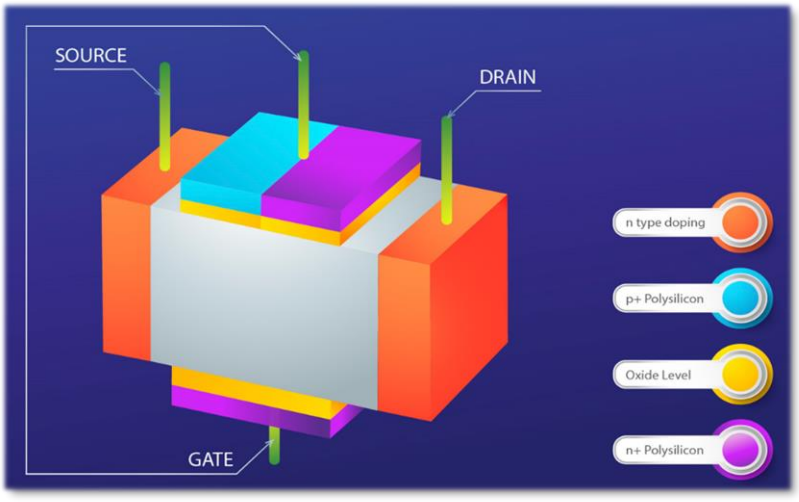

FIGURE 1.19. Schematic 3D structure of the asymmetrical DMDG

1.5.2. Concept and Operation of Graded Channel Dual Material Double Gate SOI MOSFET

The graded channel DMDG (GCDMDG) design is another modified MOSFET structure with an asymmetrically doped channel. In this structure, the doping concentration of the substrate is not uniform. It is greater on the source side than the drain side. Because of the "Doping engineering" concept, this type of structure is more feasible to fabricate than uniformly doped DMDG structure (Goel et al., 2016). Due to this type of doping nature the graded channel structure provides very good susceptibility against the SCEs, helps to improve the hot carrier movements of the device and reduces the impact ionization. Excluding all these superiorities, the GC design also generates a larger pilot current and increases transconductance in contrast with other uniformly doped devices.

An illustrative presentation of GC DMDG SOI MOSFET is portrayed in Fig. 1.20. The diagram describes that at the front gate terminal, M_1 side of the gate which locates nearer to the source is made of p^+ polysilicon and M_2 side of the gate which locates nearer to the drain, is made of n^+ polysilicon. The length of the gates are L_1 and L_2 by agreement, whereas the gate at the backside is constructed with n^+ polysilicon only (Reddy et al., 2005; Khan et al., 2008; Vadthiya et al., 2018). The constant parameters that have been used to construct the DMDG and GCDMDG device model for surface potential, electric field, threshold voltage and drain current have been given in Table 1.2. These parameters with respective values have been used throughout this research work.

To overcome the quantum mechanical tunneling effects, gate oxide leakage current, etc. that have been generated due to scaling down the oxide thickness, some oxide materials with higher k values have been used instead of SiO_2. It can be seen that due to some unique features they provides better result in MOSFET performance than SiO_2.

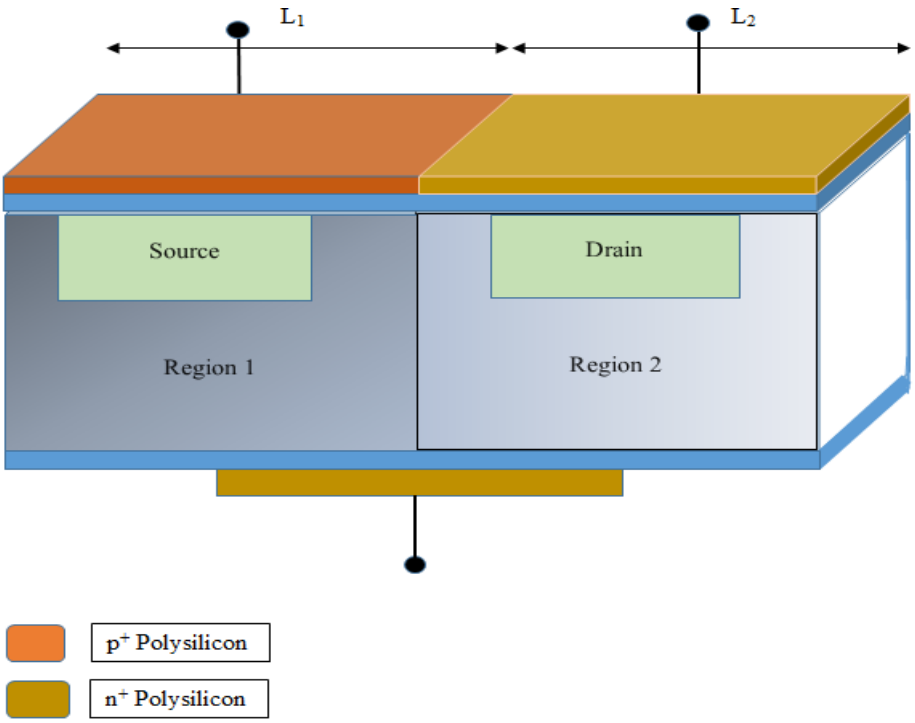

FIGURE 1.20 Schematic 3D view of GC DMDG SOI MOSFET

Table 1.2. Design parameters

Sl. No.	Parameters	Values
1.	ε_{si} - Dielectric constant of Si	11.7
2.	ε_{ox} - Permittivity of oxide	3.9 (SiO_2), 22 (HfO_2)
3.	ϕ_{M1} - Work function of p^+ polysilicon	5.25 eV
4.	ϕ_{M2} - Work function of n^+ polysilicon	4.17 eV
5.	E_g - Silicon bandgap at 300K	1.14 eV
6.	X_{si} - Electron affinity of Silicon	4.05 eV
7.	q - Electronic charge	1.6×10^{-19} C
8.	K - Boltzmann's constant	1.38×10^{-23} m^2 kg s^{-2} K^{-1}
9.	T - Absolute temperature	300K
10.	C_{air} - Permittivity of Air	1

1.6. High-k materials - Its Advantages

The term "High-k dielectric" refers to the material, which has a higher relative dielectric value (k) compared to the SiO_2 (k=3.9). The k defines the capability of the material to store energy/charge. A higher k value means a greater capacitance at a greater thickness. The uses of conventional SiO_2 based device reaches to physical limitation when the oxide thickness becomes a few atomic layers thick. These scaling limitations encouraged the researchers for an extensive investigation to find out new material instead of SiO_2 to serve as a gate oxide. When the oxide thickness becomes below 15 Å the gate leakage current exceeds about 1 A/cm^2 (Ribes et al., 2005). Though the usage of the high-k dielectric materials (i.e. HfO_2, ZrO_2, Ta_2O_5) as gate oxide decreases the tunnelling current and leakage power drastically however they provide amazing performance and greater energy effectiveness (Maity et al., 2016). The equivalent capacitance value of the gate parallel plate capacitor can be calculated as (Electronic Article; Choi et al., 2011),

$$C = \frac{k\varepsilon_o A}{t_{ox}} \tag{1.3}$$

Here, k represents the dielectric constant of the oxide, ε_o is the permittivity, A is the area of the plate and t_{ox} refers to the thickness of the oxide layer, respectively. Since the value of k is higher so it requires more thickness to obtain the same capacitive value. Qualitatively this material provides a physically thicker layer to suppress the quantum mechanical tunnelling current.

A promising high-k material should have a dielectric constant value of 10 to 30, bandgap value above 5 eV and band offset with a semiconductor substrate above 1 eV to minimize the carrier injection. A good high-k material should be thermally stable with the silicon substrate and its required thermal budget value should be below 1000 K and 90 s. The dielectric materials are mainly formed by the elements having higher atomic numbers and make ionic bonding with oxygen. At the high frequency range, the dielectric materials generate electronic polarization. So, the transition metal oxides (especially heavy metals) produce a promising high-k substance. As mentioned in (Choi et al., 2011) the properties of $SrTiO_3$ (k = 200; bandgap E_g = 3 eV; electrical breakdown field, E_{bd} = 2.2-2.3) are the most favourable for high-k material but

incompatible with MOSFET. Therefore, a perfect balance has to be considered between all the parameters to optimize the circuit performance. Remembering all these practical aspects, hafnium, zirconium and aluminium-based oxides are the best suitable with MOSFET device structure for the circuit operation as the gate leakage current is reduced by 2-3 times.

1.6.1. Hafnium Dioxide and Gate Stack Concept

In this research work, hafnium dioxide HfO_2 (k=22) has been used as a high-k dielectric material. HfO_2 has some unique advantages over the other high-k materials that assist to enhance the device performance. The high dielectric constant combines with comparatively larger bandgap (5.7 eV), larger heat of formation (271 kcal/mol,), good thermal and chemical stability on silicon and larger barrier heights at the interface with Si. Despite so many advantages, high-k oxide material cannot be used directly on the Si substrate interface. It will create a large amount of interface charge due to a fabrication problem. Also, Si-SiO_2 bonding is much better than any other substrate-oxide bonding. To overcome this problem the gate stack concept has been introduced. A thin layer of SiO_2 has been incorporated on the Si surface then high-k oxide material has deposited. This architecture helps to overcome the generation of unwanted interface charge density. The oxide thickness can be calculated by combining the oxide thickness of the duo and called the effective oxide thickness (EOT) (Kaur et al., 2008; Maity et al., 2017). It can be calculated as,

$$t_{oxeff} = t_{si} + \left\{ \left(\frac{\varepsilon_{si}}{\varepsilon_{highk}} \right) \times t_{highk} \right\} \tag{1.4}$$

Here, t_{oxeff} represents the effective oxide thickness, t_{si} and t_{highk} are the thickness of silicon dioxide and high k material layer respectively, ε_{si} and ε_{highk} are the dielectric constant of SiO_2 and high-k material respectively. Normally, the thickness of the SiO_2 and HfO_2 layers are being considered as 1nm (Maity & Maity, 2020; Maity et al., 2017).

1.7. Scope of Study

The DMDG SOI MOSFET structure is the most basic MuG MOSFET structure, and it outperforms other planar MOSFET structures. This structure incorporates the best features of both the DG and DMG structures. Because it has a larger transconductance and a lower drain conductance value, so it may reduce all forms of SCEs and improves drain breakdown voltages (Goel et al., 2016; Reddy & Kumar, 2005). As a result, it will be easier to create the model for removing SCEs using the DMDG structure. The GCDMDG structure has several advantages over the uniform structure because of the varied doping concentrations (Noor et al., 2016; Kaur et al., 2008; Vadthiya et al., 2018). Furthermore, a graded doping concentration channel is practically implementable. It may be more capable of reducing SCEs in terms of threshold voltage roll off, providing improved surface potential, and lowering the electric field's peak value.

According to many review studies, the surface potential and electric field characteristics of the DMDG structure and GCDMDG exhibit good similarities of simulated data with analytical data. When compared to the analytical and matching simulating model, these structures are predicted to deliver a wide variety of benefits as well as many parts of the research. The generated step function-like characteristics in the surface potential and electric field over the channel (smaller in the higher work function region than the lower work function region (Reddy & Kumar, 2005) can be predicted to increase the drain potential variation and drain conductance while reducing SCEs and DIBL. As the highest value of the electric field distribution helps to generate uniformly expanded drift velocity of the electron along the channel so it will help to minimize the HCEs which is a major problem of general MOSFET. The step potential will increase with the influence of temperature, interface charge effect, etc. However, instead of utilising a uniform channel length ratio for different gate materials, it is expected that if it is increased, improved performance can be produced.

Two threshold voltages have been generated for DMDG and GCDMDG structures due to differing gate materials (Goel et al., 2016). Two threshold voltages may provide improved leakage current coverage. It is the most important aspect of a device performance. Because of the small scale dimension, it is expected that the

threshold voltage in the DMDG and GCDMDG structures will remain nearly the same up to 20 nm channel length and provide the lowest roll off factor. The generated threshold voltage may be less than 1V to improve switching characteristics. The DMDG device will have the ability to consume low power while also potentially lowering the power dissipation factor. The GCDMDG structure may also be more resistant to SCEs than a uniform doping DMDG structure. Both types of DMDG structure will provide excellent performance over the current characteristics. It will increase the voltage gain property in terms of transconductance and drain conductance. The structure is expected to give improved on current and off current features. DMDG might be a better option for removing DIBL and SS. As per the report, the uniform doping DMDG structure will provide a better switching capability.

HfO_2, a high-k material, can improve all of the above features (Ribes et al., 2005; Maity et al., 2016). It is anticipated that it will improve immunity to SCEs. The high-k features that are developed may provide better outcomes than typical SiO_2.

Despite all the benefits, the DMDG structure has a major disadvantage due to its asymmetric structure. . It is having some structural issues incorporating contemporary MOS technology. But with the change in few steps in the device fabrication process researchers may be overcome the problem. This work will enhance the prospect of fabricating a DMDG MOSFET with high-k to achieve the respective advantages which it promises.

1.8. Thesis Organisation

The Thesis is organized as follows

Chapter 2 states the detailing of literature review of different MUG MOSFETs structures with the application of gate material engineering. DG and DMG structures are elaborately discussed here. Various doping engineering aspects, i.e use of uniformly doping nature and graded doping nature over DMDG structure are also documented. Detail discussions on the performance exploration also have been depicted based on different architectures. Vast usage of the high-k materials and the most promising high-k, which is compatible with MOSFET is also being documented.

Chapter 3 describes the analytical modeling part of surface potential and electric field of DMDG structure using SiO_2 as an oxide interface. The modeling structure

depends on the two-dimensional Poisson's equation and some boundary conditions. All these things are clearly described in this chapter. The surface potential and electric field characteristics of the device depend on some external parameters like temperature, oxide thickness, gate-source voltage, interface charge, etc. All these parameters are incorporated in the modeling and try to investigate the variation of performance. This chapter also describes the detailed comparison of the influence of high-k material over the device characteristics and compares it with conventional SiO_2. All the characteristics of surface potential and electric field that have been generated from the analytical model are also compared with the simulation result.

Chapter 4 derives the surface potential and electric field modeling of GCDMDG MOSFET structure simultaneously. This model also can be derived with the help of two-dimensional Poisson's equation and boundary conditions. The influence of several parameters over the characteristics is illustrated here. Like the earlier one, these characteristics also try to compare using the high-k material as the oxide interface. All results are confirmed with respective simulation results.

Chapter 5 elaborates the threshold voltage of DMDG and GCDMDG structure. The analytical model of the threshold voltage can be derived with the help of surface potential. The analytical model of subthreshold swing and DIBL is incorporated in the threshold voltage model and discusses the performances over the SCEs. In this chapter, the impact of different parameters over the model, like reduction of channel length and film thickness, temperature effects, etc. have been derived. Using HfO_2 on the threshold voltage model relates the performances over SiO_2 on the ground of SCEs. All the characteristics that have been generated are also confronted with the simulation result.

Chapter 6 also simultaneously represents the detailing of drain current of DMDG and GCDMDG structure and tries to relate the performances concerning amplification factor. The variation of transconductance, drain conductance and voltage gain over the channel length for different devices have been compared over the SCEs and performance ground. Here also, the influence of different parameters have derived over the basic model. At last, all the derived representations are related to the simulation results.

At the end of the thesis, in chapter 7 the total research work has been concluded. The total research work mainly deals with two different types of devices DMDG and GDMDG with high-k material. In this chapter, the conclusion has been derived based on the capability of swapping the SCEs keeping in mind the performance analysis using high-k. Some future aspects of this work are also being discussed in short.

CHAPTER

2

DMDG MOSFET-A Review

2.1. Overview of Semiconductor Technology

In 1926 scientist Julius Edgar Lilienfeld first demonstrated semiconductor-based technology in his patent "Method and Apparatus for Controlling Electric Currents" (Lilienfeld, 1926). He first introduced a field-effect transistor (FET) with three electrodes made of copper sulfide. But he was unable to fabricate the device. In the year 1940, the p-n junction diode was discovered by Russell Shoemaker Ohl (Ohl, 1946; Scaff & Ohl, 1947). After this William Shockley introduced a p-n junction-based transistor (Shockley, 1949; Shockley et al., 1951) in 1948. This was the milestone in the advancement of the semiconductor industry. Bell laboratory fabricated the transistor successfully in 1951 (Shockley et al., 1951). Sooner it became very essential in the circuit design sector because of its rectification and amplification property. IC was demonstrated by scientist Jack Kilby of Texas Instruments in 1958 (Kilby, 1976). After that, MOSFET was presented by John Atalla and Dawon Kahng of Bell Labs in 1960 (Kilby, 1976). MOSFET is a common device structure (Nicollian et al., 1982) and has become an essential device in the modern electronic world because of its switching and amplification properties. The input impedance of a MOSFET is extremely high, of the order of several Mega-Ohm (MΩ). The circuit consumes extremely low power due to its high input impedance which helps in the generation of high-level IC and very complex performance in simpler manner. The low power consumption of MOSFET, allow the circuitry to adjust more components per chip surface area. In package form its physical dimension goes below 4 mm^2 (Wikipedia). Apart from that it has the ability to shorten its size while the performance remains almost same. It has a very thin active area so that the size will be in more compact

form. It has no gate diode so that it can operate directly on the application of positive or negative voltage. So the device structure is used widely in the complementary MOS (CMOS) logic IC.

The gate voltage induces the channel in between drain and source and monitors the current flow through it. MOSFET is used in logic integrated circuits, oscillators, microprocessors, and discrete IC technology for its exclusive characteristics. For switching and amplifying the electronics signals it is used extensively (Moore, 1998). Apart from the semiconductor unit, it has wide applications in the mechanical and electrical segment also. It is used for several passive devices like capacitors, inductors, etc. For the operation of brushless DC motor, DC relay, switch mode power supply (SMPS) it shows excellent performance. Scientist Colinge described the fabrication process of SOI MOSFET elaborately in his research work (Colinge, 2008; J.-P. Colinge et al., 1990; J. Colinge et al., 1990). He also demonstrated the electrical properties that are exhibited by MOSFET concerning channel, gate oxide and gate electrodes. For high switching speed and high input impedance enhancement type MOSFET have a vast usage in the digital circuitry world. After the invention of MOSFET, Bell Labs demonstrated the fabrication process of p-type MOS (PMOS) and n-type MOS (NMOS) structures. In 1963, combining these two structures, C. T. Sah and Frank Wanlass of Fairchild Research & Development laboratory introduced CMOS (Wanlass, 1967; Wanlass & Sah, 1991). Two important characteristics of CMOS structure are high noise immunity and static power consumption. The waste heat production of the CMOS circuit is very low than other logic circuits like transistor-transistor logic (TTL), NMOS logic (Wikipedia). Today this technology is well known as CMOS technology.

Every second year, the number of components in the inner section of the IC doubles while their size reduces to half (Frank et al., 2001). For proper packaging and to accommodate, all the discrete components have to be scaled-down. However, the aim is to maximize the transistor speed and minimize the chip power dissipation. But due to the reduction of drain-source distance with the scaling factor of device dimension the channel length of the MOSFET also decreases. The declining of channel length helps to increases several scaling problems i.e. HCEs, SCEs, DIBL, impact ionization effects (Orouji & Rahimian, 2012) extensively. Free charged particles are

associated with charge present in the source-drain region as the distance between them decreases, resulting in SCEs. A detailed description of all different types of SCEs is discussed in the previous chapter. With the device dimension, the gate threshold voltage reduces and increases the subthreshold leakage current (Garduño et al., 2011; Yeo et al., 2003; Young, 1989). The leakage current does not adjust with the drain current, but it does generate excess heat and raising the temperature of device. As a consequence device's turn-off becomes a very serious issue (Chaudhry & Kumar, 2004a; J. Colinge et al., 1990; Garduño et al., 2013). Scientists Zeitzoff et al. (Zeitzoff & Huff, 2005) stated in their research paper that the SCEs have an impact on some key features of planar MOSFET structure like applied gate voltage, channel length, EOT, on current and leakage current, etc. Researchers accept the challenges to overcome SCE-problems generated due to scaling down the device. Numerous technologies have been introduced by the potential solution of ITRS to overcome the problems. Industries are trying their level best to incorporate all those implementations and enhance the methodology and characterization techniques to incorporate all these technical innovations at the fabrication level.

After 2007, the scaling limits are inadequate to maintain the performance of the planar MOSFET device side by side reduce the leakage current. The high-performance logic circuits are scaled more rapidly than the low-performed circuit. So the major problems have been generated in the case of ‘on’ current, switching capability, etc (Zeitzoff & Huff, 2005). To overcome the problems researchers move to non-planar structures. As an alternative to bulk MOSFET, ultrathin body silicon on insulator (UTB SOI) MOSFET, MuGs (Lou et al., 2012) like DG (Alvarado et al., 2010; Balestra et al., 1987; Cerdeira et al., 2013; Antonio Cerdeira et al., 2008; A Cerdeira et al., 2008; Chen et al., 2003; Chen & Kuo, 1996; Chiang, 2012, 2016), tri-gate (Long et al., 1999) and surrounding gate structure have been proposed. Among all MuGs, DG is the simplest structure of all that can be used for the high-performance logic circuit. The active area of the device is present within the silicon film. The thickness of the film is maintained in such a manner that when the channel is depleted it cover the total width of the film. This mechanism is called fully depleted (FD) SOI MOSFET. The DG structure consists of UTB FD SOI MOSFET (Srivastava et al., 2011). The advantage of UTB techniques is that it requires lighter doping

concentration over planar structure side by side reduces the parasitic capacitance effects. The presence of two gates improves coverage capability and helps to reduce SCEs (Abd El Hamid et al., 2007; Cerdeira et al., 2013; Contreras et al., 2010; Diagne et al., 2008; Francis et al., 1994; Jin et al., 2010; Lazaro et al., 2009; Lin & Taur, 2017; Liu et al., 2008; Lu & Taur, 2006; Maity, Maity, & Baishya, 2019; Nandi et al., 2018; Ortiz-Conde et al., 2005; Ortiz-Conde et al., 2006; Prégaldiny et al., 2006; Raskin et al., 2006), increase punch through qualities, and reduce junction capacitance. (Maity, Maity, Maity, et al., 2019; Prégaldiny et al., 2006; Raskin et al., 2006; Sallese et al., 2010; Sharma et al., 2011; Song et al., 2009; Tanaka et al., 1991; Taur et al., 2004; Venkatesan et al., 1992; Yu et al., 2007). The bottom gate is self-aligned and used the same gate oxide thickness over the substrate as the top gate. Mainly the bottom gate covers the channel in such a way that the charges of the source-drain region cannot influence it. However, the presence of the self-aligned two gates increases the device complexity and enhances the cost of the fabrication process.

Another model for overcoming SCEs is the DMG MOSFET structure (Chaudhry & Kumar, 2004b; Ghosh; Kumar & Chaudhry, 2004; Saurabh & Kumar, 2010). This device is being built as “Gate Material Engineering” rather than “Doping Engineering” due to the architectural aspects. Designing with different materials improves carrier transport properties while lowering SCEs (Long et al., 1999; Tsormpatzoglou et al., 2008; Tsormpatzoglou et al., 2007). In a DMG construction, two separate materials with non-identical work functions are linked side by side. One gate material has a higher work function than the other (Zhou, 2000). Normally p^+ and n^+ polysilicons are used as the gate material. The calculated threshold voltage near the source side is higher than the drain end for DMG n channel MOSFETs. As a result, the charged carrier accelerates throughout the channel, creating a screening effect that reduces SCEs (Pal & Sarkar, 2014). A hypothetical step function across the channel region is initiated by this arrangement. As a result, transconductance rises and the electric field in the channel becomes more equally distributed. In terms of DIBL, on current, off current, threshold voltage roll off, and the device's ratio of transconductance and drain conductance, the DMG SOI structure outperforms its SMG SOI counterpart (Kumar et al., 2017; Maria Jossy et al., 2019).

Earlier aluminium (Al) metal is used as a gate material but it has been found that depletion of polysilicon material as metal gate electrode enhances the resistivity of SCEs. It helps to enhance the EOT of the device. At 'on condition' of the MOSFET the channel is fully depleted. If the width of the channel depletion region is denoted as w_d , then the effective electrical thickness of gate oxide will be (Schaller, 2004; Zeitzoff & Huff, 2005)

$$EOT_{elec} = EOT + \Delta_{poly} \tag{2.1}$$

Here, $\Delta_{poly} = \left(\frac{t_{ox}}{\varepsilon_{si}} \right) w_d$, the value of w_d will be as much as 0.4 nm. In consequence, the resultant EOT value increases while using polysilicon material. Assimilation of these two design structures generates DMDG SOI MOSFET structure which combines the benefits of them (Goel et al., 2016; Reddy & Kumar, 2005). The combination of gate and gate material engineering techniques is utilized to enhance the device's performance. The p^+ polysilicon material (with a higher work function) is used near the source junction. This is also known as the control gate because all the key features on which the MOSFET performed depend on it. Another gate near the drain junction is made up of lower work function n^+ polysilicon. A step function like a potential profile is generated at the channel interface due to the presence of two different gate materials. This gate helps to prevent the influence of drain voltage hence it is known as a screening gate. It reduces the drain conductance by lowering the utmost value of the electric field at the drain section. It boosts the drain breakdown voltage and produces the required threshold voltage roll up for specific channel lengths (less than 100 nm) (Goel et al., 2016; Noor et al., 2016; Reddy & Kumar, 2005). The generated step potential scaled-down the subthreshold leakage current and DIBL effects. If the gate material work function of the control gate increases then it further reduces the subthreshold current (Gupta, 2019).

Ramesh and Reddy (Ramesh, 2017; Reddy & Kumar, 2005) stated that below 100 nm channel length, the DMDG structure reduces the electric field near the drain region. Mohankumar (Mohankumar et al., 2008) depicted that DMDG provides better noise immunity than any other DG structure.

To enhance the mobility of free-charged particles and generate the required device's performance, one solution is to use a strained silicon channel. The effect can be described as (Kaur et al., 2008)

$$\mu = \frac{q\tau_{scatter}}{m^*} \tag{2.2}$$

Here, μ represents the mobility of electron, m^* is effective mass and $\tau_{scatter}$ represents the mean free time against scattering (Taur & Ning, 2013). Combination of a thin layer of Si with Si-Ge layer epitaxially deposited on the top of the Si substrate. By this process strained Si layer is generated. Because of lattice mismatch, scattering lifetime increases. As a result, the mobility of the free particle increases hence the device's performances are also enhanced. With this process, an enhancement factor of 1.8 can be achieved.

The GCDMDG is another modified MOSFET structure with an asymmetrically doped channel (Abdi et al., 2009; Kaur et al., 2008). The source side has a higher doping concentration than the drain side. Because of this form of doping, the GC structure has a high immunity to SCEs, which helps to reduce the device's hot carrier effects and impact ionization (Panigrahy & Sahu, 2013; Sharma et al., 2013). A high doping channel near the source side decreases DIBL and low doping nature in the drain side increases mobility and reduces (Baishya et al., 2007) the peak value of the electric field (Kaur et al., 2007). Apart from all these superiorities, in comparison to other evenly doped devices, the GC design generates a higher driving current and increases transconductance (Baishya, 2009; Vadthiya et al., 2018). Chiang (Chiang, 2009) reported that with asymmetrical DMDG structure an improved SS and threshold voltage can be achieved over any symmetrical structure. Ramesh and Kumari (Kumari et al., 2014; Ramesh, 2017) stated that the GCDMDG structure helps to reduce SCEs and increase the on current (I_{on}) and off current (I_{off}) ratio.

Apart from planar structure, some 3D structural MOSFETs like FINFET (Panchanan et al., 2021; Seoane et al., 2018), GAA structure, triple Gate MOSFET (Colinge, 2007), surrounding gate MOSFETs (Auth & Plummer, 1997), quad gate structure (Kumar & Mahapatra, 2009), junction-less transistor (Terrill et al., 1984) also present excellent performance over the SCEs. FINFET is the most promising structure

for future ultrashort channel device structure because it provides better immunity over SCEs. But, to fabricate such a three-dimensional structure is still very difficult over the planar structure like DMDG.

2.2. Significance of MOSFET Parameters

The device performance can be measured based on some electrical parameters like surface potential, electric field, threshold voltage and drain current. Surface potential can be measured from the band bending generated in the MOS structure. Due to the assimilation of different work function materials and different band gaps like semiconductor, oxide (insulator) and metal, it has introduced a step function like formation. The generated step surface potential reduces the SCEs, however, the slope of the curve near the drain side and its peak value help to minimize the DIBL. Depending on applied gate voltage the band bending or the surface potential can be increased or decreased. Surface potential also can be increased by changing oxide thickness, film thickness, temperature, etc. In asymmetrical doped GCDMDG structure, due presence of different doping the surface potential increases more than the uniformed one. However, the step formation also remains here. These are very essential parameters of MOSFET to analyze its performance. Depending on surface potential, electric field and threshold voltage will be generated (Reddy & Kumar, 2005).

Analytically, the electric field can be calculated from the generated surface potential. It is the voltage difference between the two plates of the MOS structure. Generally, MOSFET has two parts of the electric field, they are parallel to the channel and longitudinal to the channel. It depends on the applied gate voltage. Like surface potential, the DMDG structure has a step-like electric field due to two different materials (Kumar & Chaudhry, 2004). Moreover that, the average value of the generated electric field is almost constant and it changes near the source and drain only. For the GCDMDG structure, the generated electric field is the same as the uniform DMDG structure and they change for high temperatures (Buvaneswari; Goel et al., 2016; Kumar et al., 2017).

The threshold voltage is the key factor to trigger on the device. This voltage specifically indicates the switching characteristics of the device. This also depends on

the gate voltage. Quantitatively threshold voltage can be measured from the minimum value of the surface potential. With the shrinking technology, the voltage required for the switching characteristics of the MOSFET is also lowered down. That means threshold voltage decreases. As a result power consumption, power dissipation also decreases. N. Gupta (Gupta, 2019) calculated the threshold voltage of fully depleted DMDG MOSFETs using the 2D Poisson equation. To find it, the concept of minimal surface potential is applied. K. Suzuki (Suzuki & Sugii, 1995) reported that the DMDG structure can be separated into two DG structures to determine the threshold voltage. According to the research, there are two distinct threshold voltages for two different structures.

Drain current is another important electrical parameter to monitor the amplification property of the device. Drain current will flow after achieving the threshold voltage. At that time device is on and performs all its necessary circuitry requirements. Depends on the trans and drain conductance, which can be measured from the drain current, the voltage gain can be calculated. T. K. Chiang (Chiang, 2009) depicted that the transconductance of the DMDG structure grows up and the drain conductance drops. As a result voltage gain increases. These are the basic electrical parameters to analyze the device's performance. It should be mentioned that these parameters are also affected by several other factors (Guha et al., 2015; Hosseini et al., 2007; Parker, 2002) that have been generated environmentally or at the fabrication time or to scale down the device. So before analyzing the device performance these parameters also have to be considered and they may help to enhance the surface potential and, as a result, lower leakage current according to the electric field. Some of them have been included in this research work. These constraints are temperature effects (Narang et al., 2013) and interface charge effects (Stesmans & Afanas' ev, 1998) etc.

The bandgap, carrier concentration, and thermal voltage of the semiconductor alter as the temperature varies. Consequently other physical attributes like fermi potential, effective gate voltage also alters. So it has a significant effect on device performance. Similarly, the oxide capacitance, flat band voltage, and effective gate voltage are all affected by the interface charge created at the interface of two distinct materials during fabrication (Maity et al., 2014).

2.3. Scaling Limits of SiO_2

SiO_2 has several advantages easy fabrication, stability up to temperature 1000^0C, low defect density, large bandgap (9 eV) so that it is used as the dielectric material for MOS structure over the years. The channel length, as well as gate oxide thickness, reduce with the scaling down of the device structure. The gate leakage tunneling current becomes significantly large when the gate oxide thickness is below 1 nm (Chen et al., 2016; Choi et al., 2011; Maity et al., 2014; Salmani-Jelodar et al., 2016). Scientist Muller in his research paper (Muller et al., 1999) stated that with the decreasing value of film thickness the band offset of SiO_2 with Si decreases. In his electron energy loss spectroscopy performed on 0.7 to 1.5 nm thickened SiO_2 revealed that full band gap of SiO_2 obtained only up to two monolayers of SiO_2-Si interface. Below this value, SiO_2 won't show the 'bulk' properties.

Researchers (Tang et al., 1998) also confirmed that a minimum thickness of 0.7 nm is required for SiO_2 material to obtained bulk properties. Below this value, the channel interface and polycrystalline Si gate interface overlap with each other and gradually SiO_2 losses its dielectric property. Instead of using SiO_2 as a gate oxide material, usage of high-k dielectric material (k>3.9) can resolve the problems (Maity et al., 2016). The 2010 ITRS report confirmed that the current trend is to use high-k material instead of SiO_2 in MOSFET. As a result, EOT increases and reduces the problems generated due to the shrinking of the oxide thickness (Maity et al., 2016).

However, if HfO_2 is used directly over the semiconductor surface then a rough interface scattering effects has been generated among the oxide and bulk silicon interface. These effects can be reduced by depositing a thin layer of SiO_2 just between the Si and the high-k oxide interface which is also helps to keep the EOT same. The term "gate stack" refers to this style of design (Maity et al., 2017; Maity et al., 2011). Using high-k, the thickness of EOT can be reached to 1 nm range to serve the purpose. Moreover, Zeitzoff (Zeitzoff & Huff, 2005) depicted graphically in their research paper that with the increment of EOT value leakage current density decreases. So using high-k dielectric material with lesser physical thickness is to be used for MuG MOSFET to overcome the SCEs problems (Khan et al., 2008). Remember that, to

incorporate high-k material in VLSI technology several factors have to be optimized like grain size, particle size, atomic distance, conductivity, etc.

2.4. High-k Materials

There are several oxide materials to be used as high-k dielectric material, i.e.

Aluminum oxide (Al_2O_3) has a k value of 7.5, a large bandgap (8.8.eV), good thermal stability, high barrier offset, compatible with fabrication (Yang et al., 2006). It has very good interface quality (Bouazra et al., 2008) but its wafer leakage uniformity is not meet the expectation.

Lanthanum oxide (La_2O_3) has dielectric constant 27 with EOT 0.48 nm to 1.2 nm range, low leakage current density (0.06 A/cm^2) at -1V, high breakdown field of 13.5 MV/cm, low interface trap density of 3e10 eV^{-1}/cm^2 and good reliability (Wu et al., 2000). But it is not suitable for the sub 22 nm regime.

Titanium dioxide (TiO_2) has a very high dielectric value (110) with a low bandgap energy (3-5 eV). But it is not preferable because its thermal stability is not very good.

Zirconium dioxide (ZrO_2) preferably can be used as a high-k material. It has a k value of 25 with a large energy bandgap of 5.16 eV to 7.8 eV (De Almeida & Baumvol, 2003). Also it has good thermal stability and there are no issues that have arisen as a result of the manufacturing process.

Hafnium dioxide (HfO_2) is a rare earth material and lV-B metal oxide. It is the most favorable high-k material with dielectric constant lying between 22 to 25, large band gaps (5.8 eV), high breakdown field (3.9-6.7 MV/cm). It has very good thermal and chemical stability with Si, larger barrier height and good compatibility with p^+ and n^+ polysilicon. Choi (Chiu & Horng, 2011) reported that in the operation voltage 1-1.5 V the value of leakage current will be lower than that of SiO_2 for the same EOT (0.9-2 nm). The impact of crystal structure on crucial material properties such as dielectric constant, stability, bandgap, and the energy required for point defect formation has long been recognized as important from a scientific and practical standpoint, and hence is of natural interest for HfO_2. The effects of stoichiometry, temperature, and pressure have been investigated, as well as the phase diagram. Hafnium-oxygen bond generates sevenfold coordinated when exposed to ambient conditions. Baddeleyite is a sevenfold

coordinated dioxide with a common structure. At room temperature and pressure, HfO_2 has the monoclinic baddeleyite structure with the lowest free energy of formation and the biggest volume (Quan et al., 2002; Wu et al., 2006).

The electrical properties like barrier heights or band offsets at the oxide-semiconductor heterojunction have been determined using X-ray photoemission spectroscopy (XPS), transport methods (capacitance voltage and current–voltage techniques), infrared absorption or photoluminescence excitation spectroscopy and internal photo emissivity spectroscopy. Angle-resolved photoemission experiments were used to investigate the 4f–5d hybridization in HfO_2 thin films on Si (Puthenkovilakam & Chang, 2004). By creating defect states inside the bandgap, an oxygen vacancy in a large bandgap oxide alters electrical properties. The energy position of this defect level in hafnium oxide has been calculated theoretically and empirically to be above the center of the bandgap (Desgreniers & Lagarec, 1999). Extensive defects in metal oxides, such as grain boundaries and dislocations, have a major impact on electronic characteristics (Chiu & Horng, 2011; Lowther et al., 1999). Leakage reduction is a major reason for replacing SiO_2 with high-k materials (Lowther et al., 1999). Accurate direct tunnelling modeling is essential for understanding scaling limits and ensuring that the chosen materials are highly scalable and useable for many future generations of technology.

With all these qualities this oxide material is used as a dielectric constant in CMOS technology. Fig. 2.1 represents (Maity et al., 2016) the most promising high-k materials that are used for the MOSFETs and compare them with k values. Table 2.1 represents different high-k materials with some physical parameters. Comparing the data sets of promising high-k materials given in Table 2.1, it can be said that HfO_2 and ZrO_2 are best to use as the high-k with dielectric value 22-25 and bandgap energy of 5.8 to 6 eV. HfO_2 has been chosen as a high-k material for this research work and compares its performances over SiO_2 in surface potential, electric field, and threshold voltage and drain current and tries to investigate how this model performs over the SCEs. It can be seen that using HfO_2 the performance is much better.

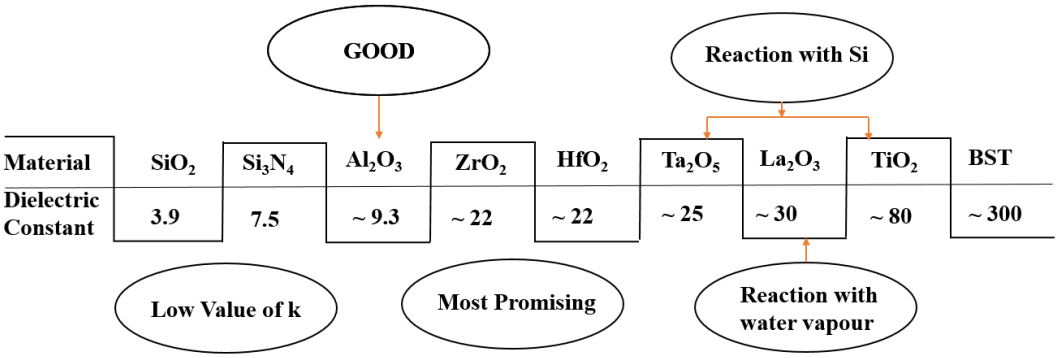

FIGURE 2.1. Most promising high-k materials

Table 2.1. Comparative study of all high-k materials (Lowther et al., 1999)

Sl No.	Dielectric Material	Relative Dielectric Constant	Band Gap (E_g in eV)	Electron Offset(eV)	Hole Offset (eV)	Breakdown field (MV/cm)
1.	SiO_2	3.9	8.9	3.5	4	10
2.	Al_2O_3	9-10	8.8	3	4.7	10
3.	TiO_3	80	3.5	1.1	1.3	3
4.	La_2O_3	27	4.3	2.3	2	13.5
5.	ZrO_2	25	5.8	1.4	3.3	4-5
6.	HfO_2	22-25	6	1.5	3.4	4-5

CHAPTER

3

Surface Potential and Electric Field of DMDG

3.1. Introduction

The band bending that occurs in the MOS structure can be used to calculate the surface potential in MOSFETs. It is very much related to the applied gate voltage. On application of it, free charge particles accumulate just below the oxide level and the energy band difference reduces, as a result, surface potential increases. The surface potential can be measured from the application of Gauss's Law, Poisson's equation, potential balance equation and considering the assumptions that the oxide interface is charge free. The electric field can be quantified from surface potential by differentiating it. It measures the voltage difference between gate and substrate (acting as the two plates of the MOS capacitor) above and below the insulator material (Nicollian et al., 1982; Ramesh, 2017).

There are two electric fields in a typical MOSFET: one parallel to the channel and the other normal to the channel. When the positive voltage is applied to the gate, the field normal to the channel keeps on increasing which results in the depletion of holes from the region below the oxide layer. Further increase in the gate voltage, starts to attract electrons onto the interface of the gate oxide layer and substrate (Hosseini et al., 2007; Parker, 2002).

Combining DG (Mohankumar et al., 2010; Sharma et al., 2011) and DMG (Kumar & Chaudhry, 2004; Saxena et al., 2002) architectural points of view, the DMDG structure (Reddy & Kumar, 2005) achieves a reduction of the peak electric field and an increase in breakdown voltage near the drain end, better transconductance than other MOSFETs, and reduction of drain conductance. For single material double gate structure (SMDG), one single lobe can be found in

surface potential characteristics whereas in the DMDG structure a step function like feature is obtained in surface potential as well as in the electric field. It originates from the presence of two different work functioned materials that exist at the upper gate as well as the lower gate. This double lobe surface potential structure helps to reduce SCEs (Young, 1989) a lot. One lobe of the characteristic curve has a lower value than the other. The lower lobe is generated at the high work-functioned material. These gates are composed of different materials and generate different electric fields as well as different threshold voltages (Goel et al., 2016; Kaur et al., 2008; Sarkar et al., 2012). Changes in temperatures (Narang et al., 2013; Streetman & Banerjee, 2006), interface charge present at the oxide interface (Maity et al., 2014) also has an influence over the performance of the device.

Generally, the high-k dielectric materials reduce the gate tunneling current and the leakage power as well as it depicts higher performance with greater energy efficiency (Kumar et al., 2011). Here, HfO_2 (Chen et al., 2016; Choi et al., 2011; Maity et al., 2017; Maity et al., 2016) is used as a high-k dielectric material. It has several benefits over the other commonly used high-k materials described earlier. Comparing with SiO_2, to obtain the same surface potential the thickness of dielectric material can be increased with HfO_2 though the layer can't be fabricated directly on the silicon substrate. To overcome such types of difficulties gate stack concept (Eqn. 1.4) is applied. In this chapter, the surface potential and electric field of the DMDG structure has been investigated using SiO_2 as well as high-k material HfO_2 through analytical modeling and simulation. All the characteristics made from the analytical model are compared with the TCAD simulation. Very good similarities can be found between them.

3.2. Analytical Model of Surface Potential of DMDG MOSFET

The surface potential distribution of the DMDG MOSFET structure can be described with the help of 2D Poisson's equation. The approximated vertical potential distribution can be solved with the help of the boundary conditions. The surface potential of the device can be solved out by the subsequent equations. The 2D schematic diagram for the cross-sectional view of the DMDG SOI MOSFET is

shown in Fig. 3.1. Here a uniform doping concentration is considered for the substrate region.

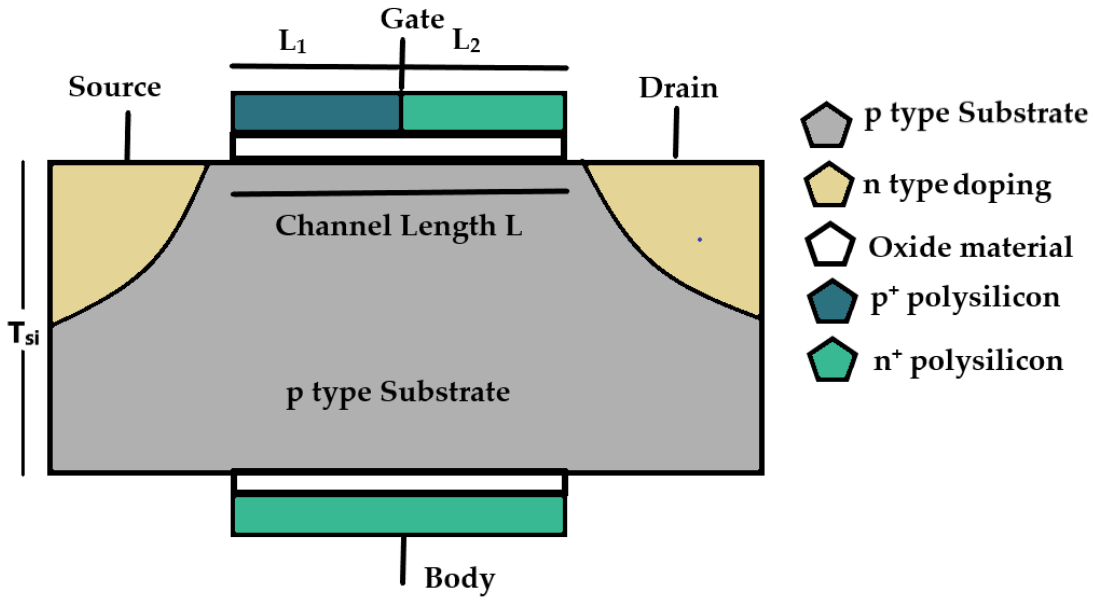

FIGURE 3.1. 2D Schematic view of the DMDG SOI MOSFET

In the schematic diagram of DMDG, the upper gate consists of material M_1 (p^+ polysilicon) and material M_2 (n^+ polysilicon) of lengths L_1 and L_2 respectively and the lower gate is of n^+ polysilicon only. The potential distribution in the silicon thin film before the moderate inversion can be written in the form of Poisson's equation. Two dimensional Poisson's equation can be described in terms of (Reddy & Kumar, 2005),

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi(x,y)}{dy^2}=\frac{qN_a}{\varepsilon_{si}} \qquad 0\le x\le L, 0\le y\le T_{si} \tag{3.1}$$

Here N_a is uniform body doping concentration independent of gate length, q is the electronic charge, ε_{si} is the permittivity (dielectric constant × absolute permittivity) of Si, L is the device channel length and T_{si} is the thickness of the film.

The potential distribution in the vertical direction $\phi(x,y)$ can be approximated by a simple parabolic function for fully depleted SOI MOSFET,

$$\phi(x,y) = \phi_S(x) + a_{d1}(x)y + a_{d2}(x)y^2 \tag{3.2}$$

where, $\phi_S(x)$ is the surface potential of DMDG and $a_{d1}(x), a_{d2}(x)$ are the arbitrary constant depends on x only. In the DMDG MOSFET structure, there are two different materials used in the gate region as M_1 and M_2 (p^+ polysilicon and n^+ polysilicon) with two different work functions of ϕ_{M1} and ϕ_{M2} respectively. Therefore, the flat-band voltages of the p^+ polysilicon $\left(V_{FB_d,fp}\right)$ and n^+ polysilicon $\left(V_{FB_d,fn}\right)$ at the front gate would be dissimilar and can be calculated as,

$$V_{FB_d,fp} = \phi_{MS1} = \phi_{M1} - \phi_{si}$$

$$V_{FB_d,fn} = \phi_{MS2} = \phi_{M2} - \phi_{si} \tag{3.3}$$

Here, ϕ_{si} is the work function of silicon and can be expressed as,

$$\phi_{si} = X_{si} + \frac{E_g}{2q} + \phi_F \tag{3.4}$$

where, X_{si} is the electron affinity of silicon, E_g is the silicon bandgap at 300 K, q is the electronic charge and ϕ_F is the Fermi potential.

The expression of fermi potential is

$$\phi_F = V_T \ln\left(\frac{N_a}{n_i}\right) \tag{3.5a}$$

Here V_T is the thermal voltage and denoted by

$$V_T = KT/q. \tag{3.5b}$$

Here K is Boltzmann's constant, T is the absolute temperature of the environment and n_i is the intrinsic carrier concentration. Surface Potential under p^+ polysilicon (M_1 gate) and n^+ polysilicon (M_2 gate) can be written as,

$$\phi_{d1}(x,y) = \phi_{S1}(x) + a_{d11}(x)y + a_{d12}(x)y^2 \qquad 0 \le x \le L_1, 0 \le y \le T_{si} \tag{3.6a}$$

$$\phi_{d2}(x,y) = \phi_{S2}(x) + a_{d21}(x)y + a_{d22}(x)y^2 \qquad L_1 \le x \le L_1 + L_2, 0 \le y \le T_{si} \tag{3.6b}$$

where, $\phi_{S1}(x)$ and $\phi_{S2}(x)$ are the Surface Potential under p^+ polysilicon and n^+ polysilicon and $a_{d11}(x), a_{d12}(x), a_{d21}(x), a_{d22}(x)$ are arbitrary constant depends on x. Some boundary conditions must be studied in order to determine the surface potentials under two different gate materials of the DMDG structure.

3.2.1. Boundary Conditions

1. For DMG, the electric flux is constant at the front gate oxide interface. So,

$$\frac{d\phi_{d1}(x,y)}{dy}|_{y=0} = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\phi_{S1}(x) - V_{GSf1}}{t_{ox}}\right) \quad \text{under } M_1 \tag{3.7}$$

$$\frac{d\phi_{d2}(x,y)}{dy}|_{y=0} = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\phi_{S2}(x) - V_{GSf2}}{t_{ox}}\right) \quad \text{under } M_2 \tag{3.8}$$

where ε_{ox} is the permittivity (dielectric constant × absolute permittivity) of oxide and t_{ox} is the gate oxide thickness, M_1 is the p^+ polysilicon of length L_1 and M_2 is the n^+ polysilicon of length L_2.

Now,

$$V_{GSf1} = V_{GS} - V_{FB_d,fp} \tag{3.9a}$$

$$V_{GSf2} = V_{GS} - V_{FB_d,fn} \tag{3.9b}$$

V_{GS} is the gate-source voltage

2. Uninterrupted electric flux at the back channel's gate oxide.

$$\frac{d\phi_{d1}(x,y)}{dy}|_{y=T_{si}} = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{V_{GS,b} - \phi_B(x)}{t_{oxb}}\right) \quad \text{under } M_1 \tag{3.10}$$

$$\frac{d\phi_{d2}(x,y)}{dy}|_{y=T_{si}} = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{V_{GS,b} - \phi_B(x)}{t_{oxb}}\right) \quad \text{under } M_2 \tag{3.11}$$

$V_{GS,b} = V_{GS} - V_{FB_d,bn}$ is the gate-source voltage at the back gate (3.12)

$V_{FB_d,bn}$ is the flat band voltage for the back gate. Here we are using n^+ polysilicon for the back gate, so, $V_{FB_d,bn} = V_{FB_d,fn}$. So, it can be written as,

$$V_{GS,b} = V_{GS} - V_{FB_d,fn} = V_{GSf2} \tag{3.13}$$

t_{oxb} is the back gate oxide thickness and the potential function along the back gate oxide-silicon contact is $\phi_B(x)$.

3. Continuous surface potential at the front gate's boundary,

$$\phi_{d1}(L_1,0) = \phi_{d2}(L_1,0) \tag{3.14}$$

4. At the interface of two different materials of the front gate, the electric flux is continuous,

$$\frac{d\phi_{d1}(x,y)}{dx}|_{x=L_1} = \frac{d\phi_{d2}(x,y)}{dx}|_{x=L_1} \tag{3.15}$$

5. The surface potential at the source end,

$$\phi_{d1}(0,0) = \phi_{S1}(0) = V_{bi} \tag{3.16}$$

V_{bi} is the built-in-potential across the body source junction. The expression is

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{3.17}$$

N_d is the doping concentration of source and drain region.

6. The surface potential near the drain end,

$$\phi_{d2}(L_1+L_2,0) = \phi_{S2}(L_1+L_2) = V_{bi} + V_{DS} \tag{3.18}$$

where, V_{DS} is the applied drain-source voltage. Using these boundary conditions, the constant terms $a_{d11}(x), a_{d12}(x), a_{d21}(x), a_{d22}(x)$ can be solved. To solve $a_{d11}(x)$, $a_{d12}(x)$ put y=0 in Eqn. 3.6a

$$\phi_{d1}(x,y) = \phi_{S1}(x) + 0 + 0 \tag{3.19}$$

Differentiating Eqn. 3.6a concerning y and putting $y = 0$,

$$\frac{d\phi_{d1}(x,y)}{dy}|_{y=0} = 0 + a_{d11}(x) + 2a_{d12}(x)y = a_{d11}(x)$$

From the first boundary condition stated in Eqn. 3.7, comparing the value of derivative,

$$a_{d11}(x)=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\phi_{S1}(x)-V_{GSf1}}{t_{ox}}\right) \tag{3.20}$$

Putting $y=T_{si}$ in Eqn. 3.6a,

$$\phi_{d1}(x,y)=\phi_{S1}(x)+a_{d11}(x)T_{si}+a_{d12}(x){T_{si}}^2 \tag{3.21a}$$

At $y=T_{si}$ the back gate potential $\phi_B(x,y)$ has to be considered here

$$\phi_B(x,y)=\phi_{S1}(x)+a_{d11}(x)T_{si}+a_{d12}(x){T_{si}}^2 \tag{3.21b}$$

Considering the derivative of the Eqn. 3.21b with respect to y and comparing with Eqn. 3.10,

$$\frac{d\phi_{d1}(x,y)}{dy}|_{y=T_{si}}=\frac{d\phi_B(x,y)}{dy}|_{y=T_{si}}=a_{d11}(x)+2a_{d12}(x)T_{si}=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{V_{GS,b}-\phi_B(x)}{t_{oxb}}\right) \tag{3.22}$$

$$\Rightarrow\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxb}a_{d11}(x)+\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{d12}(x)T_{si}^2=V_{GS,b}-\phi_B(x)$$

Putting the value of $\phi_B(x)$ from Eqn. 3.21b to Eqn. 3.22,

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{d12}(x)T_{si}^2=V_{GS,b}-\left(\phi_{S1}(x)+a_{d11}(x)T_{si}+a_{d12}(x){T_{si}}^2\right)-\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxb}a_{d11}(x)$$

Putting the value of $a_{d11}(x)$ from Eqn. 3.20 in the above equation and simplifying it,

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{d12}(x)T_{si}^2=V_{GS,b}-\left\{\phi_{S1}(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S1}(x)-V_{GSf1}}{t_{ox}}T_{si}\right)+a_{d12}(x){T_{si}}^2\right\}-\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}}\left(\frac{\phi_{S1}(x)-V_{GSf1}}{t_{ox}}\right)$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{d12}(x)T_{si}^2=V_{GS,b}-\phi_{S1}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)-a_{d12}(x)T_{si}^2$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{d12}(x)T_{si}^2+a_{d12}(x)T_{si}^2=V_{GS,b}-\phi_{S1}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)$$

$$\Rightarrow\left(2\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}+1\right)a_{d12}(x)T_{si}^2=V_{GS,b}-\phi_{S1}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)$$

$$\Rightarrow a_{d12}(x)=\frac{V_{GS,b}-\phi_{S1}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)}{\left(1+2\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}\right)T_{si}^{2}} \quad (3.23)$$

Considering, $c_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$, $c_{oxb}=\frac{\varepsilon_{ox}}{t_{oxb}}$ and $c_{si}=\frac{\varepsilon_{si}}{T_{si}}$,

$$\Rightarrow a_{d12}(x)=\frac{V_{GS,b}-\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)+V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^{2}} \quad (3.24)$$

Similarly, solving for $a_{d21}(x)$ and $a_{d22}(x)$ put $y=0$ in Eqn. 3.6b,

$$\phi_{d2}(x,y)=\phi_{S2}(x)+0+0 \quad (3.25)$$

Differentiating Eqn. 3.6b with respect to y and putting $y=0$,

$$\frac{d\phi_{d2}(x,y)}{dy}|_{y=0}=0+a_{d21}(x)+2a_{d22}(x)y=a_{d21}(x)$$

From the first boundary condition stated in Eqn. 3.8, comparing the values,

$$a_{d21}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S2}(x)-V_{GSf2}}{t_{ox}}\right) \quad (3.26)$$

Putting $y=T_{si}$ in Eqn. 3.6b, the surface potential will be,

$$\phi_{d2}(x,y)=\phi_{B}(x,y)=\phi_{S2}(x)+a_{d21}(x)T_{si}+a_{d22}(x)T_{si}{}^{2} \quad (3.27)$$

At $y=T_{si}$, the device dimension signifies the back gate, so the back gate potential consider here, differentiating Eqn. 3.27 with y and comparing the equation with the 2nd boundary condition given in Eqn. 3.11,

$$\frac{d\phi_{d2}(x,y)}{dy}|_{y=T_{si}}=\frac{d\phi_{B}(x,y)}{dy}|_{y=T_{si}}=a_{d21}(x)+2a_{d22}(x)T_{si}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{V_{GS,b}-\phi_{B}(x)}{t_{oxb}}\right) \quad (3.28)$$

$$\Rightarrow \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxb}a_{d21}(x)+\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{d22}(x)T_{si}^{2}=V_{GS,b}-\phi_{B}(x) \quad (3.29)$$

Putting the value of $\phi_{B}(x)$ from Eqn. 3.27,

$$\Rightarrow \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{oxb} a_{d21}(x) + \frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}} 2a_{d22}(x) T_{si}^2 = V_{GS,b} - \left(\phi_{S2}(x) + a_{21}(x) T_{si} + a_{22}(x) T_{si}^{\,2}\right)$$

$$\Rightarrow \frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}} 2a_{d22}(x) T_{si}^2 = V_{GS,b} - \left(\phi_{S2}(x) + a_{d21}(x) T_{si} + a_{d22}(x) T_{si}^{\,2}\right) - \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{oxb} a_{d21}(x)$$

Putting the value of $a_{d22}(x)$ from Eqn. 3.26 and simplifying it,

$$\frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}} 2a_{d22}(x) T_{si}^2 = V_{GS,b} - \left\{\phi_{S2}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S2}(x) - V_{GSf2}}{t_{ox}}\right) T_{si} + a_{22}(x) T_{si}^{\,2}\right\} - \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si}}\left(\frac{\phi_{S2}(x) - V_{GSf2}}{t_{ox}}\right)$$

$$\Rightarrow \frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}} 2a_{d22}(x) T_{si}^2 = V_{GS,b} - \phi_{S2}(x)\left(1 + \frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right) + V_{GSf2}\left(\frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right) - a_{d22}(x) T_{si}^2$$

$$\Rightarrow \frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}} 2a_{d22}(x) T_{si}^2 + a_{d22}(x) T_{si}^2 = V_{GS,b} - \phi_{S2}(x)\left(1 + \frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right) + V_{GSf2}\left(\frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right)$$

$$\Rightarrow \left(2\frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}} + 1\right) a_{d22}(x) T_{si}^2 = V_{GS,b} - \phi_{S2}(x)\left(1 + \frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right) + V_{GSf2}\left(\frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right)$$

$$\Rightarrow a_{d22}(x) = \frac{V_{GS,b} - \phi_{S2}(x)\left(1 + \frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right) + V_{GSf2}\left(\frac{\varepsilon_{ox} T_{si}}{\varepsilon_{si} t_{ox}} + \frac{\varepsilon_{si} t_{oxb} \varepsilon_{ox}}{\varepsilon_{ox} \varepsilon_{si} t_{ox}}\right)}{\left(1 + 2\frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox} T_{si}}\right) T_{si}^2} \tag{3.30}$$

Considering, $c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $c_{oxb} = \frac{\varepsilon_{ox}}{t_{oxb}}$ and $c_{si} = \frac{\varepsilon_{si}}{T_{si}}$,

$$a_{d22}(x) = \frac{V_{GS,b} - \phi_{S2}(x)\left(1 + \frac{c_{ox}}{c_{si}} + \frac{c_{ox}}{c_{oxb}}\right) + V_{GSf2}\left(\frac{c_{ox}}{c_{si}} + \frac{c_{ox}}{c_{oxb}}\right)}{\left(1 + 2\frac{c_{si}}{c_{oxb}}\right) T_{si}^2} \tag{3.31}$$

To calculate the surface potential under the p^+ polysilicon gate material and putting the values of $a_{11}(x)$ and $a_{12}(x)$ from Eqn. 3.20 and 3.24 in Eqn. 3.6a,

$$\phi_{d1}(x, y) = \phi_{S1}(x) + a_{d11}(x) y + a_{d12}(x) y^2$$

$$\phi_{d1}(x,y)=\phi_{S1}(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S1}(x)-V_{GSf1}}{t_{ox}}\right)y+\frac{V_{GS,b}-\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)+V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}y^2 \quad (3.32)$$

Differentiating the Eqn. 3.32 twice with respect to x,

$$\frac{d^2\phi_{d1}(x,y)}{dx^2}=\frac{d^2\phi_{S1}(x)}{dx^2} \quad (3.33)$$

Differentiating the Eqn. 3.32 twice with y,

$$\frac{d^2\phi_{d1}(x,y)}{dy^2}=\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}+\frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (3.34)$$

Putting the values of Eqn. 3.33 and 3.34 in Poisson's equation for DMDG,

$$\frac{d^2\phi_{d1}(x,y)}{dx^2}+\frac{d^2\phi_{d1}(x,y)}{dy^2}=\frac{qN_a}{\varepsilon_{si}} \quad (3.35)$$

$$\frac{d^2\phi_{S1}(x)}{dx^2}+\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}+\frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}=\frac{qN_a}{\varepsilon_{si}}$$

$$\Rightarrow\frac{d^2\phi_{S1}(x)}{dx^2}-\frac{2\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}=\frac{qN_a}{\varepsilon_{si}}-\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (3.36)$$

Putting $\alpha=\frac{2\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}$ and $\beta_1=\frac{qN_a}{\varepsilon_{si}}-\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}$

Then,

$$\frac{d^2\phi_{S1}(x)}{dx^2}-\alpha\phi_{S1}(x)=\beta_1 \quad (3.37)$$

To calculate the surface potential under the n^+ polysilicon gate material putting the values of $a_{d21}(x)$, $a_{d22}(x)$ from Eqn. 3.26 and 3.31 in Eqn. 3.6b,

$$\phi_{d2}(x,y) = \phi_{S2}(x) + a_{d21}(x)y + a_{d22}(x)y^2$$

$$\phi_{d2}(x,y) = \phi_{S2}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S2}(x) - V_{GSf2}}{t_{ox}}\right)y + \frac{V_{GS,b} - \phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right) + V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}y^2 \quad (3.38)$$

Differentiating the Eqn. 3.38 twice with x,

$$\frac{d^2\phi_{d2}(x,y)}{dx^2} = \frac{d^2\phi_{S2}(x)}{dx^2} \quad (3.39)$$

Differentiating Eqn. 3.38 twice with y,

$$\frac{d^2\phi_{d2}(x,y)}{dy^2} = \frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \frac{2\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} + \frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (3.40)$$

Putting the values of Eqn. 3.39 and 3.40 in Poisson's equation for DMDG,

$$\frac{d^2\phi_{d2}(x,y)}{dx^2} + \frac{d^2\phi_{d2}(x,y)}{dy^2} = \frac{qN_a}{\varepsilon_{si}}$$

$$\frac{d^2\phi_{S2}(x)}{dx^2} + \frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \frac{2\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} + \frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} = \frac{qN_a}{\varepsilon_{si}}$$

$$\Rightarrow \frac{d^2\phi_{S2}(x)}{dx^2} - \frac{2\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} = \frac{qN_a}{\varepsilon_{si}} - \frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (3.41)$$

Putting, $\alpha = \dfrac{2\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}$ and $\beta_2 = \dfrac{qN_a}{\varepsilon_{si}} - \dfrac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \dfrac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}$

Then,

$$\frac{d^2\phi_{S2}(x)}{dx^2} - \alpha\phi_{S2}(x) = \beta_2 \tag{3.42}$$

3.2.2. Solution of Partial Differential Equation

From Eqn. 3.37, $\frac{d^2\phi_{S1}(x)}{dx^2} - \alpha\phi_{S1}(x) = \beta_1$. Let, $\phi_{S1}(x) = e^{mx}$ where, $e^{mx} \neq 0$, so the trial solution will be $\frac{d^2\phi_{S1}(x)}{dx^2} - \alpha\phi_{S1}(x) = 0$. Now, $\phi_{S1}(x) = e^{mx}$,

so, $\frac{d^2\phi_{S1}(x)}{dx^2} = m^2 e^{mx}$. From the trial solution,

$$m^2 e^{mx} - \alpha e^{mx} = 0$$

$$\Rightarrow e^{mx}\left(m^2 - \alpha\right) = 0 \qquad \text{as} \quad e^{mx} \neq 0$$

$$\Rightarrow \left(m^2 - \alpha\right) = 0$$

$$\Rightarrow m^2 = \alpha$$

$$\Rightarrow m = \pm\sqrt{\alpha}$$

So, the roots are real and distinct. Now, the complementary functions (C.F.) are

$$\text{C.F.} \Rightarrow x_c = Ae^{\sqrt{\alpha}x} + Be^{-\sqrt{\alpha}x} \tag{3.43}$$

A and B are two arbitrary constant. Particular integral (P.I.) of the Eqn 3.43 is

$$\text{P.I.} = \frac{1}{D^2 - \alpha}\beta_1 \tag{3.44}$$

[if, $\frac{d}{dx} = D$ then $\frac{d^2\phi_{S1}(x)}{dx^2} - \alpha\phi_{S1}(x) = \beta_1$ can be written as $\left(D^2 - \alpha\right)\phi_{S1}(x) = \beta_1$]

$$\Rightarrow \frac{1}{-\alpha\left(1 - \frac{D^2}{\alpha}\right)}\beta_1$$

$$= -\frac{1}{\alpha}\left(1 - \frac{D^2}{\alpha}\right)^{-1}\beta_1$$

$$= -\frac{1}{\alpha}\left(1 + \frac{D^2}{\alpha}\right)\beta_1 \qquad \text{[Binomial expansion]}$$

$$= -\frac{\beta_1}{\alpha} \qquad \text{[Taking the derivatives]}$$

So, the total equation will be $\phi_{S1}(x) =$ C.F.+P.I.

$$\phi_{S1}(x) = Ae^{\sqrt{\alpha}x} + Be^{-\sqrt{\alpha}x} - \frac{\beta_1}{\alpha}$$

$$\Rightarrow \phi_{S1}(x) = Ae^{\lambda x} + Be^{-\lambda x} + \sigma_1 \qquad [\text{putting } \sqrt{\alpha} = \lambda \text{ and } -\frac{\beta_1}{\alpha} = \sigma_1] \qquad (3.45)$$

Similarly, $\phi_{S2}(x) = Ce^{\lambda(x-L_1)} + De^{-\lambda(x-L_1)} + \sigma_2 \qquad [\text{putting } -\frac{\beta_2}{\alpha} = \sigma_2] \qquad (3.46)$

From the boundary condition Eqn. 3.14,

$$\phi_{d1}(L_1, 0) = \phi_{d2}(L_1, 0)$$

Putting the values from Eqn. 3.45 and 3.46

$$Ae^{\lambda L_1} + Be^{-\lambda L_1} + \sigma_1 = Ce^{\lambda(L_1 - L)_1} + De^{-\lambda(L_1 - L_1)} + \sigma_2$$

$$\Rightarrow Ae^{\lambda L_1} + Be^{-\lambda L_1} + (\sigma_1 - \sigma_2) = C + D \qquad (3.47)$$

Form the boundary condition Eqn. 3.15,

$$\frac{d\phi_{d1}(x,y)}{dx}|_{x=L_1} = \frac{d\phi_{d2}(x,y)}{dx}|_{x=L_1}$$

Putting, the values of $\phi_{S1}(x)$, $\phi_{S2}(x)$ and considering the derivatives

$$\frac{d\phi_{S1}(x)}{dx}|_{x=L_1} = \lambda Ae^{\lambda L_1} - \lambda Be^{-\lambda L_1}$$

$$\Rightarrow \frac{d\phi_{S1}(x)}{dx}|_{x=L_1} = \lambda\left(Ae^{\lambda L_1} - Be^{-\lambda L_1}\right) \qquad (3.48)$$

Similarly, $\frac{d\phi_{S2}(x)}{dx}|_{x=L_1} = \lambda Ce^{\lambda(L_1 - L_1)} - \lambda De^{-\lambda(L_1 - L_1)}$

$$\Rightarrow \frac{d\phi_{S2}(x)}{dx}|_{x=L_1} = \lambda(C - D) \qquad (3.49)$$

According to the boundary condition

$$\frac{d\phi_{S1}(x)}{dx}|_{x=L_1} = \frac{d\phi_{S2}(x)}{dx}|_{x=L_1} = \lambda(C - D) = \lambda\left(Ae^{\lambda L_1} - Be^{-\lambda L_1}\right)$$

$$\Rightarrow (C - D) = \left(Ae^{\lambda L_1} - Be^{-\lambda L_1}\right) \qquad (3.50)$$

Solving Eqn. 3.47 and 3.50

$$C = \left(Ae^{\lambda L_1} + \frac{\sigma_1 - \sigma_2}{2} \right) \tag{3.51}$$

and $D = \left(Be^{-\lambda L_1} + \frac{\sigma_1 - \sigma_2}{2} \right)$ (3.52)

From the boundary condition of Eqn. 3.16 and 3.18,

$$\phi_{d1}(0,0) = \phi_{S1}(0) = V_{bi} \text{ and } \phi_{d2}(L_1 + L_2, 0) = \phi_{S2}(L_1 + L_2) = V_{bi} + V_{DS}$$

Putting the values in the equation $\phi_{S1}(x) = Ae^{\lambda x} + Be^{-\lambda x} + \sigma_1$

$$\phi_{S1}(0) = Ae^{\lambda 0} + Be^{-\lambda 0} + \sigma_1$$

$$\Rightarrow \phi_{S1}(0) = A + B + \sigma_1 = V_{bi}$$

$$\Rightarrow A = V_{bi} - B - \sigma_1 \tag{3.53a}$$

$$\Rightarrow B = V_{bi} - A - \sigma_1 \tag{3.53b}$$

From another condition, Eqn. 3.18, put the value in,

$$\phi_{S2}(x) = Ce^{\lambda(x - L_1)} + De^{-\lambda(x - L_1)} + \sigma_2$$

$$\Rightarrow \phi_{S2}(L_1 + L_2) = Ce^{\lambda(L_1 + L_2 - L_1)} + De^{-\lambda(L_1 + L_2 - L_1)} + \sigma_2 = V_{bi} + V_{DS}$$

$$\Rightarrow \phi_{S2}(L_1 + L_2) = Ce^{\lambda(L_2)} + De^{-\lambda(L_2)} + \sigma_2 = V_{bi} + V_{DS}$$

Putting the values of C and D from Eqn. 3.51 and 3.52,

$$\phi_{S2}(L_1 + L_2) = \left(Ae^{\lambda L_1} + \frac{\sigma_1 - \sigma_2}{2} \right) e^{\lambda(L_2)} + \left(Be^{-\lambda L_1} + \frac{\sigma_1 - \sigma_2}{2} \right) e^{-\lambda(L_2)} + \sigma_2 = V_{bi} + V_{DS}$$

$$\Rightarrow Ae^{\lambda L_1} e^{\lambda(L_2)} + \frac{\sigma_1 - \sigma_2}{2} e^{\lambda(L_2)} + Be^{-\lambda L_1} e^{-\lambda(L_2)} + \frac{\sigma_1 - \sigma_2}{2} e^{-\lambda(L_2)} + \sigma_2 = V_{bi} + V_{DS}$$

$$\Rightarrow Ae^{\lambda L} + Be^{-\lambda L} + \frac{\sigma_1 - \sigma_2}{2} \left(e^{\lambda(L_2)} + e^{-\lambda(L_2)} \right) = V_{bi} + V_{DS} - \sigma_2$$

$$\Rightarrow Ae^{\lambda L} + Be^{-\lambda L} + (\sigma_1 - \sigma_2)\cosh(\lambda L_2) = V_{bi} + V_{DS} - \sigma_2 \tag{3.54}$$

Putting the value of B from Eqn. 3.53b,

$$\Rightarrow Ae^{\lambda L} + (V_{bi} - A - \sigma_1)e^{-\lambda L} + (\sigma_1 - \sigma_2)\cosh(\lambda L_2) = V_{bi} + V_{DS} - \sigma_2 \tag{3.55}$$

$$\Rightarrow Ae^{\lambda L} - Ae^{-\lambda L} + (V_{bi} - \sigma_1)e^{-\lambda L} + (\sigma_1 - \sigma_2)\cosh(\lambda L_2) = V_{bi} + V_{DS} - \sigma_2$$

$$\Rightarrow A=\left\{\left(V_{bi}+V_{DS}-\sigma_2\right)-\left(V_{bi}-\sigma_1\right)e^{-\lambda L}-\left(\sigma_1-\sigma_2\right)\cosh\left(\lambda L_2\right)\right\}\frac{e^{-\lambda L}}{\left(1-e^{-2\lambda L}\right)} \tag{3.56}$$

Putting the value of A from Eqn. 3.53b to 3.54

$$Ae^{\lambda L}+Be^{-\lambda L}+\left(\sigma_1-\sigma_2\right)\cosh\left(\lambda L_2\right)=V_{bi}+V_{DS}-\sigma_2$$

$$\Rightarrow\left(V_{bi}-B-\sigma_1\right)e^{\lambda L}+Be^{-\lambda L}+\left(\sigma_1-\sigma_2\right)\cosh\left(\lambda L_2\right)=V_{bi}+V_{DS}-\sigma_2$$

$$\Rightarrow\left(V_{bi}-\sigma_1\right)e^{\lambda L}-Be^{\lambda L}+Be^{-\lambda L}+\left(\sigma_1-\sigma_2\right)\cosh\left(\lambda L_2\right)=V_{bi}+V_{DS}-\sigma_2$$

$$\Rightarrow B\left(e^{\lambda L}-e^{-\lambda L}\right)=\left(V_{bi}-\sigma_1\right)e^{\lambda L}-\left(V_{bi}+V_{DS}-\sigma_2\right)+\left(\sigma_1-\sigma_2\right)\cosh\left(\lambda L_2\right)$$

$$\Rightarrow B=\left\{\left(V_{bi}-\sigma_1\right)e^{\lambda L}-\left(V_{bi}+V_{DS}-\sigma_2\right)+\left(\sigma_1-\sigma_2\right)\cosh\left(\lambda L_2\right)\right\}\frac{e^{-\lambda L}}{\left(1-e^{-2\lambda L}\right)} \tag{3.57}$$

With the variation of the temperature, the bandgap, carrier concentration, and thermal voltage of the semiconductor changes obeying the relation

$$E_g\left(T\right)=E_g\left(T_0\right)-\frac{\alpha T^2}{T+\beta} \tag{3.58}$$

where, $E_g\left(T_0\right)$ is the bandgap at 0 K, α and β are arbitrary constants (Narang, 2013). Similarly, the substrate concentration $N_a\left(T\right)$, doping concentration $N_d\left(T\right)$ and intrinsic carrier concentration $n_i\left(T\right)$, thermal voltage values will act as a function of temperature (Streetman & Banerjee, 2006) .

$$V_T\left(T\right)=V_T\left(T_0\right)\times\left(\frac{T}{T_0}\right) \tag{3.59}$$

$$N_a\left(T\right)=N_a\left(T_0\right)\left(\frac{T}{T_0}\right)^{\frac{3}{2}} \tag{3.60}$$

$$N_d\left(T\right)=N_d\left(T_0\right)\left(\frac{T}{T_0}\right)^{\frac{3}{2}} \tag{3.61}$$

$$n_i\left(T\right)=n_i\left(T_0\right)\left(\frac{T}{T_0}\right)^{\frac{3}{2}} \tag{3.62}$$

If SiO_2 is replaced by high-k materials as the gate oxide, some difficulties will arise. Though higher capacitance value can be achieved by using high-k materials however it generates poor electrical quality at the oxide-semiconductor interface. Consequently, the breakdown voltages that have been generated in the dielectric region become lower and decrease the lifetime of the device. Further, due to the difference in work function and the presence of the trap charges at the interface (Maity et al., 2014), the characteristics do not match with the ideal MOS device. The device with flat band voltage, V_{FB} and threshold voltage, V_{th} are strongly affected by the interface oxide charges. The interface trap charge is,

$$\phi_{ox} = \frac{Q_0}{c_{ox}} \tag{3.63}$$

So the flat band voltages for two different materials are from Eqn. 3.3

$$V_{FB_d,fp} = \phi_{MS1} = (\phi_{M1} - \phi_{si}) - \phi_{ox} \tag{3.64a}$$

$$V_{FB_d,fn} = \phi_{MS2} = (\phi_{M2} - \phi_{si}) - \phi_{ox} \tag{3.64b}$$

and the effective gate source voltages are from Eqn. 3.9

$$V_{GSf1} = V_{GS} - V_{FB_d,fp} \text{ and } V_{GSf2} = V_{GS} - V_{FB_d,fn} \tag{3.65}$$

The electric field can be evaluated by differentiating the surface potential expression. The electric fields for two different regions are,

$$E_1(x) = \frac{d\phi_{S1}(x)}{dx}|_{y=0} = A\lambda e^{\lambda x} - B\lambda e^{-\lambda x},\ 0 \le x \le L_1 \text{ under } M_1 \text{ and} \tag{3.66a}$$

$$E_2(x) = \frac{d\phi_{S2}(x)}{dx}|_{y=0} = C\lambda e^{\lambda(x-L_1)} - D\lambda e^{-\lambda(x-L_1)},\ L_1 \le x \le L \text{ under } M_2 \tag{3.66b}$$

3.3. Results and Discussions

The generated surface potential throughout the channel for fully depleted DMDG SOI MOSFET structure is compared with its SMDG SOI MOSFET counterpart (Fig. 3.2). All the design parameters have been listed in Table 3.1. All the defined characteristics of the proposed model computation has shown an excellent agreement with the results of the TCAD simulation. The surface potential of the uniformly doped DMDG structure is a parameter-dependent element in the theoretical model. Table 3.1 lists all of the parameter values and device dimensions

required to calculate the surface potential. From the literature review, device dimensions such as channel length, film thickness, doping concentration, and gate material work functions have been taken into account. (Reddy, 2005). To establish the doping concentration of the substrate, some experimental work (Bhattacherjee, 2007) has been explored. The temperature variation's arbitrary constant has been takeninto consideration (Narang, 2013). For both situations, the same interface charge (Maity et al., 2014) has been used for the same oxide thickness.

Table 3.1: Design Parameter Values for Surface Potential

Sl. No.	Parameters	Values
1.	N_a - Uniform body doping concentration	1×10^{15} cm^{-3}
2.	N_d - Source/ Drain doping concentration	5×10^{19} cm^{-3}
3.	T_{si} - Film Thickness	12 nm
4.	L - Device channel length	100 nm
5.	L_1 - Gate length of M_1 p^+ Polysilicon	50 nm
6.	L_2 - Gate length of M_2 n^+ Polysilicon	50 nm
7.	n_i - Intrinsic carrier concentration	1.5×10^{10} cm^{-3}
8.	t_{ox} - Gate oxide thickness	1nm
9.	t_{oxb} - Back gate oxide thickness	1nm
10.	V_{DS} - Drain source voltage	0.8 V
11.	V_{GS} - Gate source voltage	0.15 V
12.	β - Arbitrary constant	636
13.	α - Arbitrary constant	4.73×10^{-4}
14.	Q_0 - Interface Charge	1.6×10^{-9} C/cm^2

Fig. 3.2 shows the change of surface potential with the position along the channel for the SMDG structure using SiO_2 and HfO_2 as the gate insulator material. Here the work function of the polysilicon that has been used in the gate is 5.25 eV for both cases. It is found that only a single lobe is present in the surface potential characteristics and it tends to SCEs as the single material is used. The presence of single material is unable to reduce DIBL and HCE effects compared with dual material (Ramesh, 2017). When HfO_2 is used as gate oxide material the tendency of surface potential characteristics is more flattened than SiO_2. Whereas for both materials the average value of the surface potential is the same.

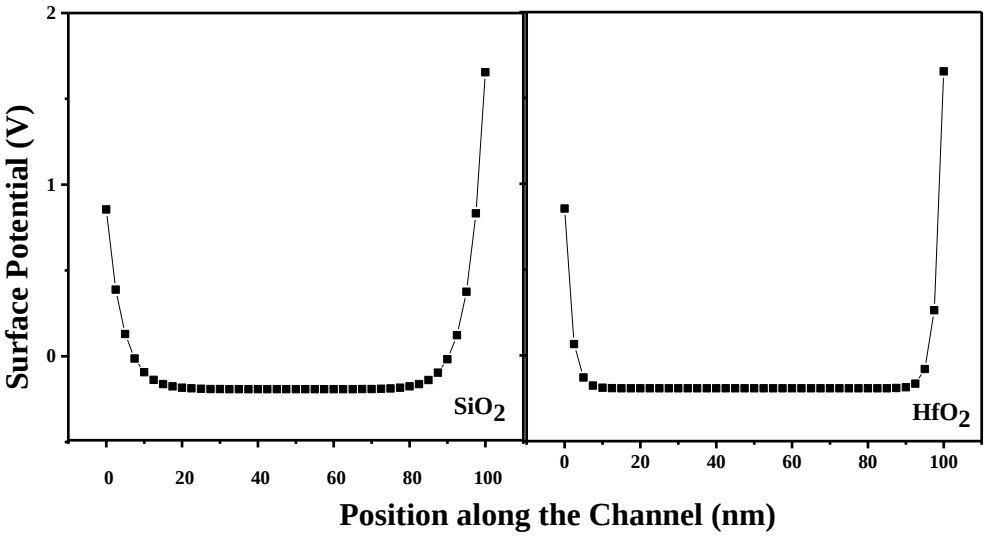

FIGURE 3.2. Surface potential profile for SMDG

In comparison with DMDG SOI MOSFET, it is found that the surface potential has two lobes (Figure 3.3). The characteristics also show that a distinct step function has been generated between two lobes for both SiO_2 and HfO_2, respectively. Like SMDG, the characteristics are more flattened using high-k material than conventionally used SiO_2. It is also revealed from Fig. 3.3 that, in case of high-k material the jump of surface potential from one lobe to another is more stiff using high-k. However, when HfO_2 has been used the surface potential becomes lower than SiO_2 for the same conditions applied. The step function in surface potential is generated mainly due to materials with different work functions used at the gates.

Usually, in higher work function material, the generated surface potential is lesser than lower functioned one. Due to the difference, it looks like a step function (Fig. 3.3).From the above figures (Fig. 3.2 and 3.3) it is clearly evident that the surface potential increases in DMDG structure when compared with SMDG structure. Additional step change increases the screening in the channel region from the drain potential as stated in (Ramesh, 2017).

An increment of surface potential also helps to increase the electric field as well as the threshold voltage of the device. The slope of the surface potential of the DMDG structure near the drain side is lower than the SMDG device. As mentioned in (Sarkar et al., 2012), these characteristics help in the reduction of the electric field near the drain end and become immune to SCEs generated due to drain voltage (DIBL effect) (Sarkar et al., 2012; Saxena et al., 2002). As the unwanted current is automatically suppressed out in this condition, the DMDG structure can be utilized to overcome the SCEs problem. It is also revealed that (Fig. 3.3) for the equivalent parameters, specifically for the similar oxide thickness values the generated surface potential for the high-k material, HfO_2 is lower than conventional one. Earlier in (Kumar et al., 2011), it was also observed that the obtained surface potential is higher for lower k value. So, it can be stated that by generating the same surface potential using SiO_2 the oxide thickness of HfO_2 can be increased as the gate dielectric material.

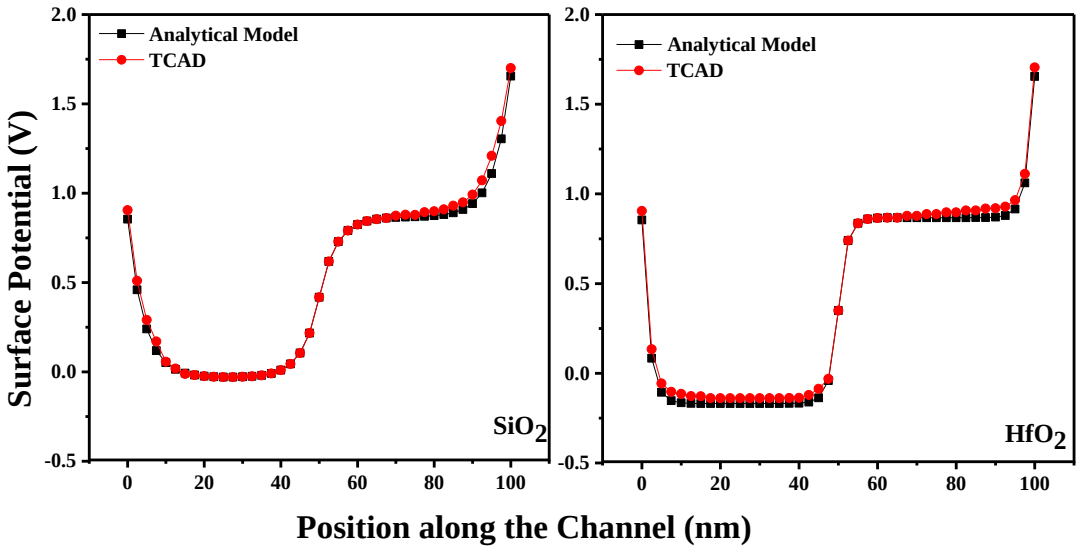

FIGURE 3.3. Surface potential profile for DMDG

It is depicted that the (Fig. 3.4) surface potential profiles with position along the channel for different oxide thickness with SiO_2 as well as HfO_2 respectively. It is revealed that the surface potential decreases with decreasing oxide thickness. From 1nm of oxide thickness, the value of surface potential becomes negative using SiO_2. Whereas, all the values of surface potential under the same oxide thickness becomes negative when HfO_2 is used. So, it can be stated that for identical parameters especially for the same oxide thickness the surface potential obtained from HfO_2 material is lesser than SiO_2 as evident from Fig. 3.4. Due to scaling down, the oxide thickness also decreases with the length of the device. But to obtain the same value of surface potential the oxide thickness can be increased using HfO_2 (Reddy & Kumar, 2005). For validation of the proposed model, TCAD simulating data is presented in the figure. Here, oxide thickness is considered as 1 nm and 2 nm for both the materials used.

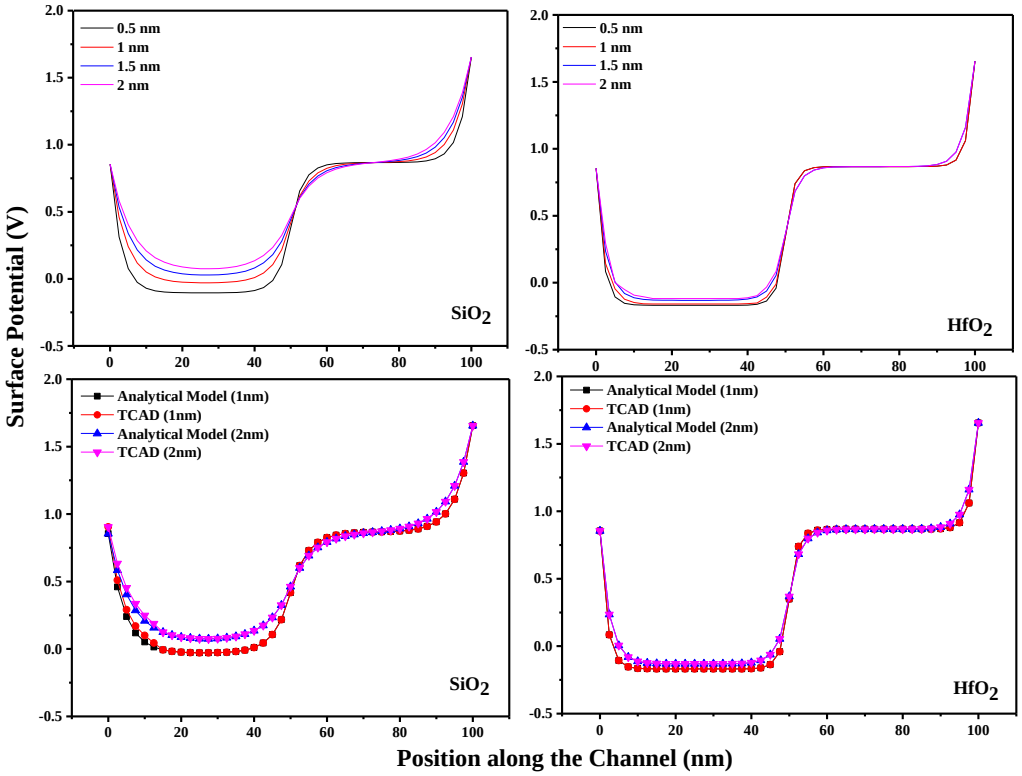

FIGURE 3.4. Change of surface potential with the channel position using different oxide thicknesses

The surface potential with the position along the channel for different substrate doping using the oxide material SiO_2 and HfO_2 have been represented in Fig. 3.5, respectively. The different values of the doping concentration that have been considered here are (a) N_a =1.5×10^{17} cm^{-3}, (b) N_a = 5×10^{17} cm^{-3}, (c) N_a =1×10^{18} cm^{-3}, (d) N_a = 5 × 10^{18} cm^{-3}, (e) N_a = 1 × 10^{19} cm^{-3}, (f) N_a = 1.5 × 10^{20} cm^{-3}, respectively. With the increment of substrate doping the surface potential increases for both the oxide materials, but for the same substrate doping the surface potential of the device using HfO_2 is lower than SiO_2 as evident from the result. The slope of the curve near the drain side using HfO_2 is almost the same for all the characteristics with different substrate doping. Therefore, it can be concluded that, with the increasing value of substrate doping, the Fermi potential of the silicon, gate voltage increases but the flat band voltage decreases. As a result the consequent surface potential increases. For the same device performance, a low doped device using HfO_2 can be used than SiO_2. The DIBL effect is also low because the slopes are nearly the same at the drain side using HfO_2. The results are validated with TCAD simulations for N_a =1.5×10^{17} cm^{-3} and N_a = 1.5×10^{20} cm^{-3} with SiO_2 as well as HfO_2. Extremely good conformity can be found between the analytical model and the TCAD plot.

The variations of surface potential for different gate-source voltages using two different oxide materials are explained in Fig. 3.6. It can be stated from the representation that, with the increasing value of gate voltage the surface potential increases. The gate-source voltage is the key feature of MOSFET. The gates act like a capacitor that accumulate energy in the form of a charged particle. The device transforms from the accumulation region to the strong inversion region by the application of appropriate gate-source voltage. With the increment of voltage, more number of charged particles accumulate at the edge of the channel under the gates and the surface potential increases.

Surface potential variation with position along the channel for different temperatures using two different oxide materials have been illustrated in Fig. 3.7. For both cases, the potential profile increases with increasing temperature. When the applied temperature is below room temperature (300K), the generated surface potential becomes negative by using SiO_2 and above that, the value of surface

potential becomes positive. Nevertheless, in the case of high-k, the generated surface potential becomes positive after 410K.

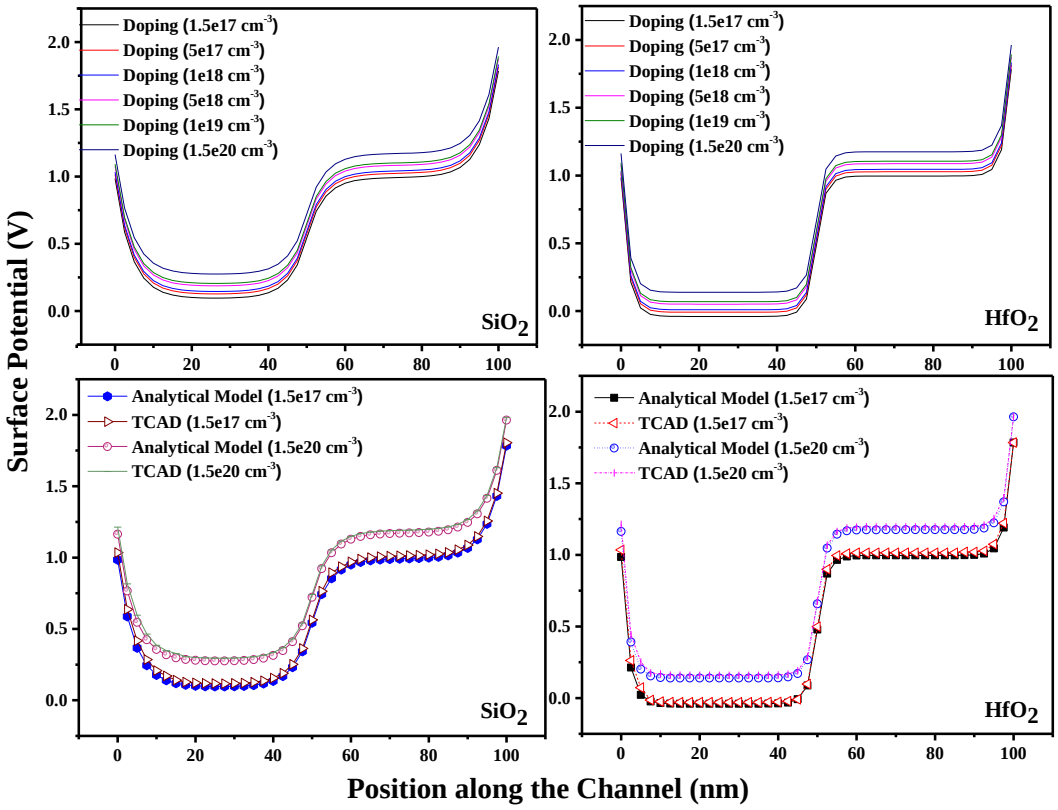

FIGURE 3.5. Change of surface potential with the channel position using different substrate doping

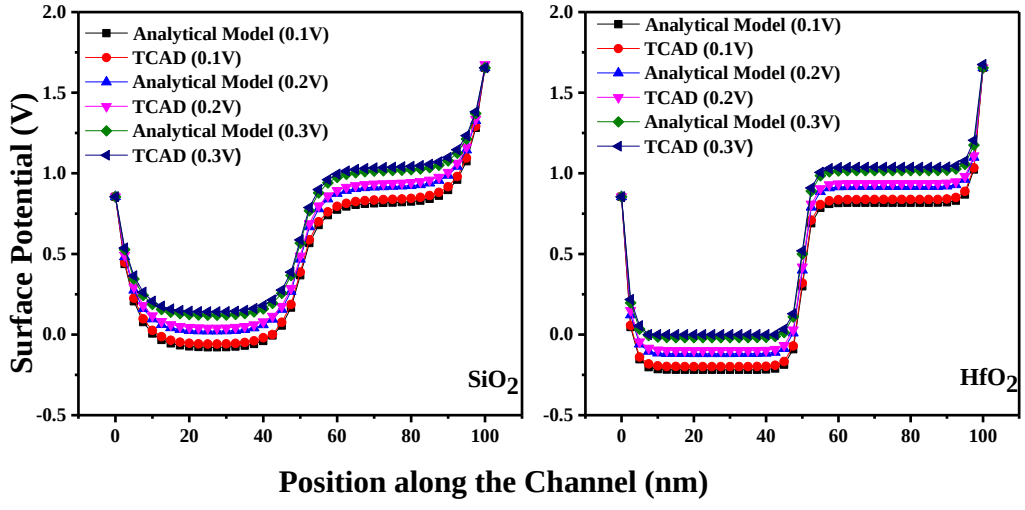

FIGURE 3.6. Surface potential with the channel position for different gate-source voltage

Therefore, it can be specified that, when other parameters of the device are scaled down, with the proper maintaining of device temperature the device performance can be sustained. It is stated in (Narang et al., 2013), that with the increasing temperature, the bandgap of the semiconductor reduces. Also with the changes in temperature semiconductor concentration profile as well as Fermi function changes. It has direct impacts on the surface potential. Henceforth surface potential also rises with the increment of the temperature. As the threshold voltage is depends on minimum potential so, with the variation of temperature the threshold voltage shows unique behaviour that will be discussed in next chapter. However, the influence of temperature is weak at high gate voltage value due to good controllability of two gates upon the channel.

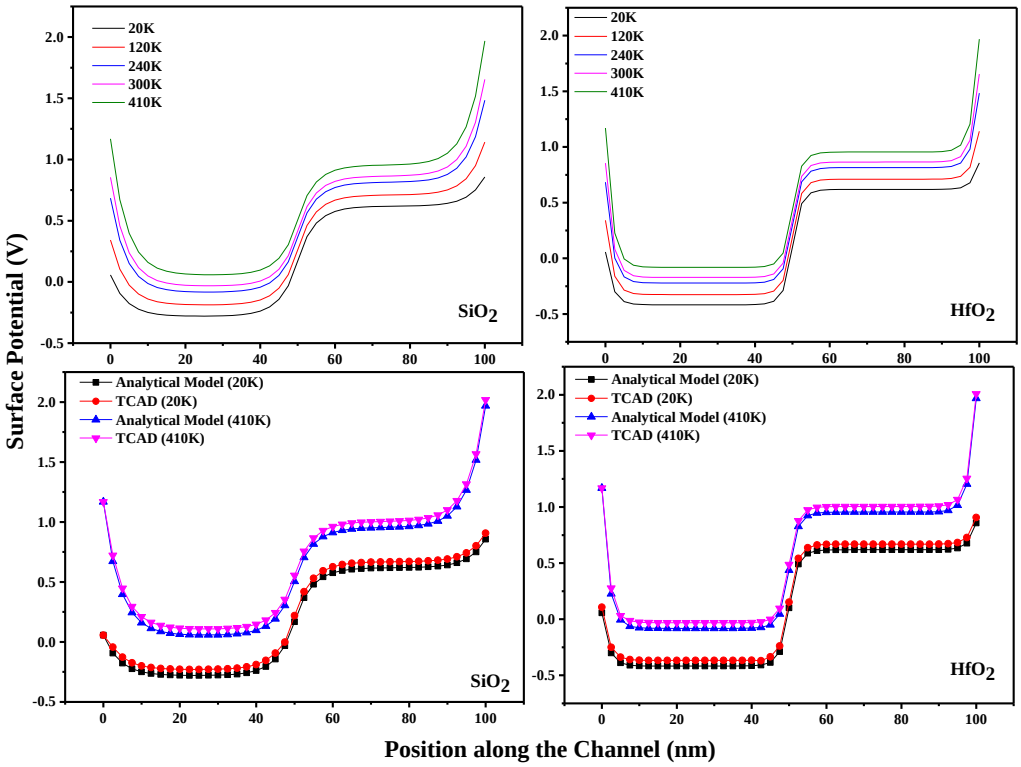

FIGURE 3.7. Change of surface potential with the channel position for different temperature

The variation of surface potential with normalized channel position for different combinations of channel length (L_1 and L_2) under different gate materials (M_1 and M_2) have been symbolized in Fig. 3.8. The total gate length is constant. Here

the different channel lengths under the two gate regions have been considered as (a) L_1:L_2=1:1, (b) L_1:L_2=1:2 and (c) L_1:L_2=2:1. The position of minimum surface potential always under L_1 and it is shifted towards the source as the gate length under M_1 reduces. For both cases, the surface potential of channel length ratio L_1:L_2=1:2 achieved the lowest value at the drain region, and L_1:L_2=2:1 achieved the highest value. It is mentioned in (Saxena et al., 2002) for smaller L_1/L_2 ratio the electrostatic potential increases with scaling down L_1. As a result, threshold voltage reduces and current increases. This type of structure is called asymmetric DMDG (ADMDG) structure. The analytical model prediction result exhibits good agreement with TCAD results as shown in the figure.

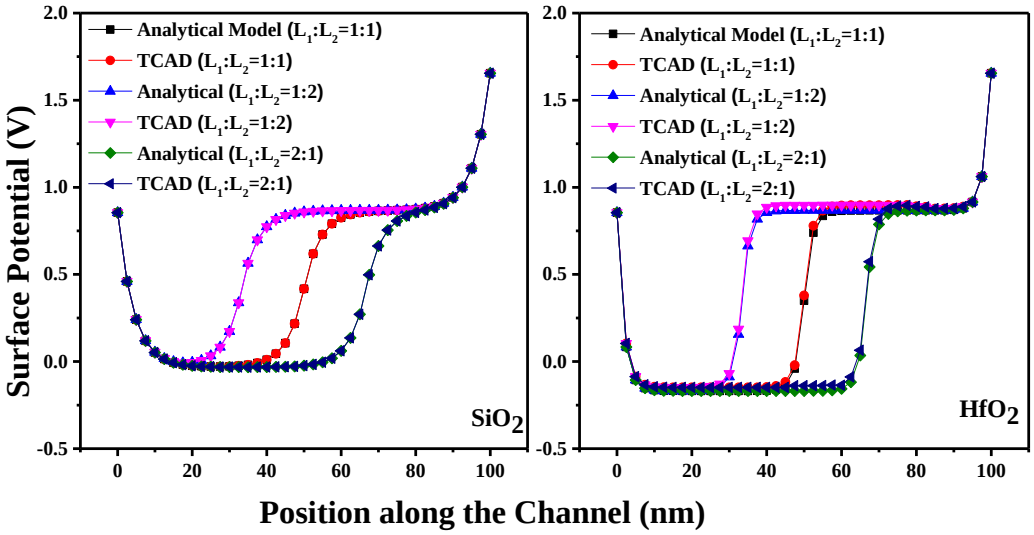

FIGURE 3.8. Surface potential with the channel position for different channel length ratio

Figure 3.9 shows the surface potential vs position along the channel, considering the interface charge that exists at the oxide-semiconductor interface. At the time of fabrication of oxide material upon the semiconductor surface, due to presence of two dissimilar materials, some amount of unwanted charges is generated between them and act as interface charge (Maity et al., 2014). Here, for both cases, the interface charge have been considered as $Q_0 = 1.6\times10^{-9} C/cm^2$ for simplicity. From the Fig. 3.10, it can be elaborated that when SiO_2 is used as the oxide material the incorporated interface charge increases the surface potential. But in the case of

high-k material, the interface charge has no distinguished effects in the device performance. From the above representation, it can be stated that when SiO_2 has been used as the gate oxide material the effective gate voltage increases as well as the surface potential. However for HfO_2 oxide material, the interface charge does not make any significant change. With the reduced oxide thickness value, the interface trap charge density increases, which upsurges in case of HfO_2. Increasing value in interface charge exposes that introducing high-k material in MOS structure decreases the interfacial attachment between semiconductor and insulator.

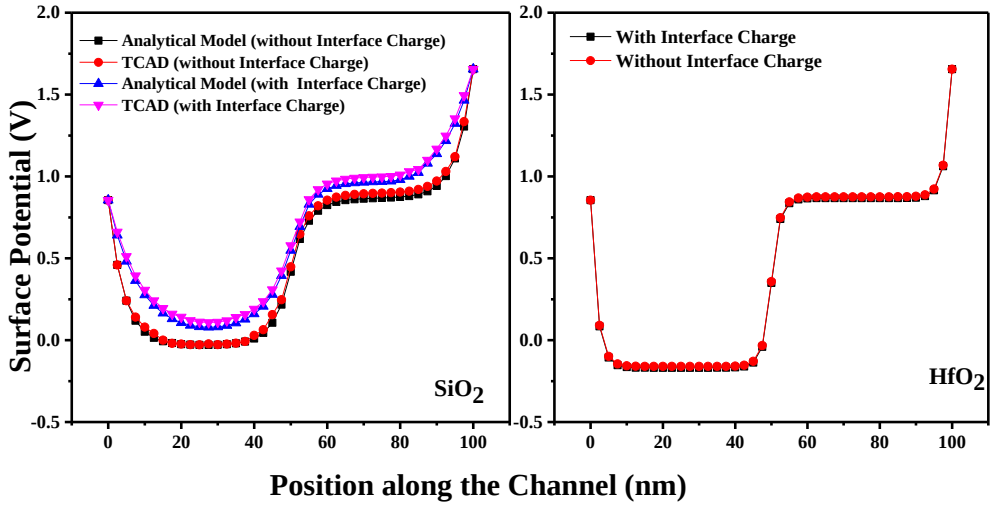

FIGURE 3.9. Surface potential with the channel position considering interface charge

Just like the surface potential electric field of the DMDG structure also shows step function because the electric field is generated from the surface potential. Figure 3.10 represents the electric field for two materials at different temperatures. It is depicted from the figure that, using high-k material the amplitude of the characteristics at the source side as well as drain side and at the middle of the channel is much more than using SiO_2. Apart from that, the average value of the electric field is almost near to zero through the channel. It can also be illustrated from the figure that it has no such significant effect at high and low temperatures for both cases. Only the peak value near the source and drain side of the characteristics increases using high-k material at high temperature.

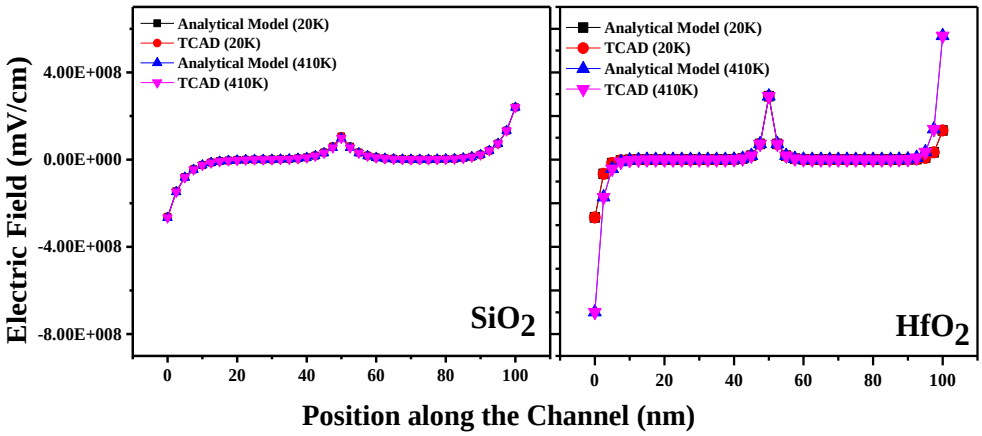

FIGURE 3.10. Comparison of electric field with channel position at different temperature

3.4. Summary

Surface potential is a basic and important characteristic of any amplifying device. All other essential characteristics parameters like electric field, threshold voltage and as well as drain current fully depend on it. Surface potential also changes with applied gate-source voltage. Depending on the potential difference, MOSFET changes its state from accumulation to strong inversion region and promotes itself to a very good and reliable amplifier. Due to the presence of different polysilicons (of different work functions) at the gate region, the step function generated at the surface potential characteristics make the DMDG structure a unique one. This nature reduces the peak value of the surface potential at the drain side. As a result, DIBL reduces. To minimize the gate tunneling affect the oxide thickness has to be increased without affecting the drain current. Again due to the small scale structure oxide thickness should be reduced. But using SiO_2, as an oxide material, has some limitations. Below 1 nm range, it would not work as an insulator and a huge amount of tunneling current flow through it. Considering all the above results it can be found that when all the other parameters are the same, the surface potential for the high-k material is lower than conventional oxide material. This statement leads to the conclusion that to achieve the equivalent value of surface potential the oxide material thickness in case of high-k material can be increased. It may help to overcome the tunnelling current problem to some extent. Using high-k dielectric material HfO_2 the oxide thickness

can be enhanced without affecting the surface potential hence the drain current. By changing the substrate doping concentration, temperature and gate-source voltage the surface potential also can be increased for the minimum oxide thickness. Also if we change some designing aspect of the device gate length structure then it will generate a better result. If surface potential decreases the threshold voltage also decreases, which leads to the flow of many unaccountable currents through the device structure. This unwanted current sometimes becomes so high that damages down the device structure. A good nature of the surface potential is also reflected in the electric field, threshold voltage as well as drain current. An increment of surface potential also helps to increase the threshold voltage. On the other hand using DMDG structure helps to decrease the other SCEs generated due to scaling down. It can be concluded that by using a DMDG structure with high-k material as a dielectric material all the problems normally generated for scaling down the structure can be eliminated.

CHAPTER

4

Surface Potential and Electric Field of GCDMDG

4.1. Introduction

In view of "Gate engineering" and "Gate material engineering", DG and DMG structures provide improved channel coverage (Frank et al., 2001; Moore, 1998; Nicollian et al., 1982; Orouji & Rahimian, 2012), which helps to reduce SCEs (Chaudhry & Kumar, 2004a; Garduño et al., 2011; Yeo et al., 2003; Young, 1989), increase punch through characteristics, and lower the capacitance created at junctions (Abd El Hamid et al., 2007; Balestra et al., 1987; Cerdeira et al., 2013; Maity et al., 2019). This type of design aids in improving carrier transport property efficiency (Chaudhry & Kumar, 2004b; Kumar & Chaudhry, 2004; Long et al., 1999; Pal & Sarkar, 2014; Saxena et al., 2002). When DG and DMG are combined, a DMDG SOI MOSFET structure is formed, which enhances the benefits of both (Reddy & Kumar, 2005). It helps to overcome the threshold voltage roll off problem that has been generated in other types of MOSFETs for less than 20 nm channel lengths and increases the drain breakdown voltage by decreasing the peak of the electric field near the drain side (Cerdeira et al., 2008). It also helps to reduce DIBL and drain conductance by declining the peak of the electric field near the drain side (Sharma et al., 2009).

In view of "Doping engineering" concept, the GC design is another adapted structure with an asymmetrically doped channel (Goel et al., 2016). Here the substrate is not uniformly doped. Comparing with the drain side, the substrate near the source side is fabricated with higher doping concentration. Consequently, the channel is

heavily doped near to the source region and moderately or lightly doped near to the drain region. This lateral asymmetric channel (LAC) helps to reduce the depletion width at the junction. The highly doped channel near the source side moderates the threshold voltage as well as DIBL effect. The lightly doped region near the drain end increases mobility and reduces the peak value of the surface potential along with the electric field. The GC structure gives excellent immunity to SCEs and boosts the on-off current ratio as a result of asymmetric doping nature. The pocket implantation techniques suppress the SCEs and improve circuit performance. It also helps to diminish the HCEs of the device and reduces the impact of ionization. Apart from all these advantages the GC design also produces a larger pilot current and rises transconductance in contrast with other uniformly doped planar structure (Kumar et al., 2016; Vadthiya et al., 2018).

If the DMDG device is asymmetrically doped instead of symmetrically doped, a GCDMDG structure can be created. It has already been reported that the GCDMDG structure increases drain current, peak transconductance and gives an outstanding cut off frequency at lower drain current. Apart from the gate and doping engineering concept, there are several other parameters also which have a huge impact on the device characteristics like temperature (Narang et al., 2013), interface charge (Maity et al., 2014; Suddapalli & Nistala, 2021), channel length ratio (Goel et al., 2016), etc. These parameters are also considered here for the comparative study between DMDG and GCDMDG structures. It has been established that all these parameters when simultaneously combine with the proposed structure increase the surface potential as well as electric field and decrease the leakage current.

It has also been observed that using high-k material the device performance will be better and reduce the SCEs for the small scale dimension. Among several high-k materials, HfO_2 has been chosen for some beneficial role. For the same value of surface potential, the thickness of the HfO_2 layer can be increased over the SiO_2 (Maity et al., 2017; Maity et al., 2011; Maity et al., 2016; Salmani-Jelodar et al., 2016). It can be calculated that using HfO_2 almost six times better performance can be achieved. Sometimes, to overcome the compatibility problems between Si substrate and high-k, the gate stack concept has to be incorporated. Surface potential and electric field of the GCDMDG MOSFET structure employing SiO_2 and HfO_2, which is obtained by

combining both DMG and GC engineering principles in the DG MOS devices, are detailed in this chapter. All the proposed characteristics of the structure have been related with similar results with uniform doping DMDG MOS structures. All the characteristics made from the analytical model are compared with TCAD simulation. Very good similarities can be found between them.

4.2. Analytical Model for Surface Potential of GCDMDG MOSFET

The surface potential distribution of the GCDMDG MOSFET structure can be described with the help of 2D Poisson's equation, the approximated vertical potential distribution with the help of the boundary conditions. Considering all the equations, the surface potential of the GCDMDG device can be solved out. The influence of the fixed insulator substrate interface charges on the channel's electrostatic potential was ignored during the modelling process.

Figure 4.1 shows a two-dimensional schematic illustration of a GCDMDG MOSFET. Doping concentration is different for two different zones (shown in figure with two different colour contrast) i.e. N_{a1} is considered as doping concentration of the substrate close by the source and N_{a2} is the doping concentration of the substrate near the drain region and the condition is $N_{a1} > N_{a2}$ (Chaudhry & Kumar, 2004b). The electronic charge is considered as q and the permittivity of Si is ε_{si}, the dimension of the device channel is L and T_{si} denotes the film thickness.

The 2D Poisson's equation depicted the potential distribution function of GCDMDG thin layer channel,

$$\frac{d^2\phi_{gc1}(x,y)}{dx^2} + \frac{d^2\phi_{gc1}(x,y)}{dy^2} = \frac{qN_{a1}}{\varepsilon_{si}} \qquad 0 \le x \le L_1, 0 \le y \le T_{si} \tag{4.1}$$

$$\frac{d^2\phi_{gc2}(x,y)}{dx^2} + \frac{d^2\phi_{gc2}(x,y)}{dy^2} = \frac{qN_{a2}}{\varepsilon_{si}} \qquad L_1 \le x \le L_2, 0 \le y \le T_{si} \tag{4.2}$$

The distribution of the potential $\phi_{gc}(x,y)$ is in the perpendicular (i.e in y) direction that can be calculated from the approximated form of a simple parabolic function. The expression for GCDMDG structure is

$$\phi_{gc}(x,y) = \phi_S(x) + a_{gc1}(x)\,y + a_{gc2}(x)\,y^2 \tag{4.3}$$

where, $\phi_S(x)$ describes the surface potential, $a_{gc1}(x)$ and $a_{gc2}(x)$ (mainly depending on x only) are the constants term. In DMDG SOI MOSFET configuration, the different gate materials (p^+ polysilicon and n^+ polysilicon) uses work functions ϕ_{M1} and ϕ_{M2} respectively and $\phi_{M1} > \phi_{M2}$. As a consequence, the calculated flat band voltages for the front gate material of the p^+ polysilicon $\left(V_{FB_d,fp}\right)$ and n^+ polysilicon $\left(V_{FB_d,fn}\right)$ are described in Eqn. 3.3,

$$V_{FB_{gc},fp} = \phi_{MS1} = \phi_{M1} - \phi_{si1} \quad \text{and}$$

$$V_{FB_{gc},fn} = \phi_{MS2} = \phi_{M2} - \phi_{si2} \tag{4.4}$$

where, ϕ_{si1} and ϕ_{si2} are the work functions of Si for two different doping regions. The expression is given by,

$$\phi_{si1} = X_{si} + \left(\frac{E_g}{2q}\right) + \phi_{F1} \tag{4.5a}$$

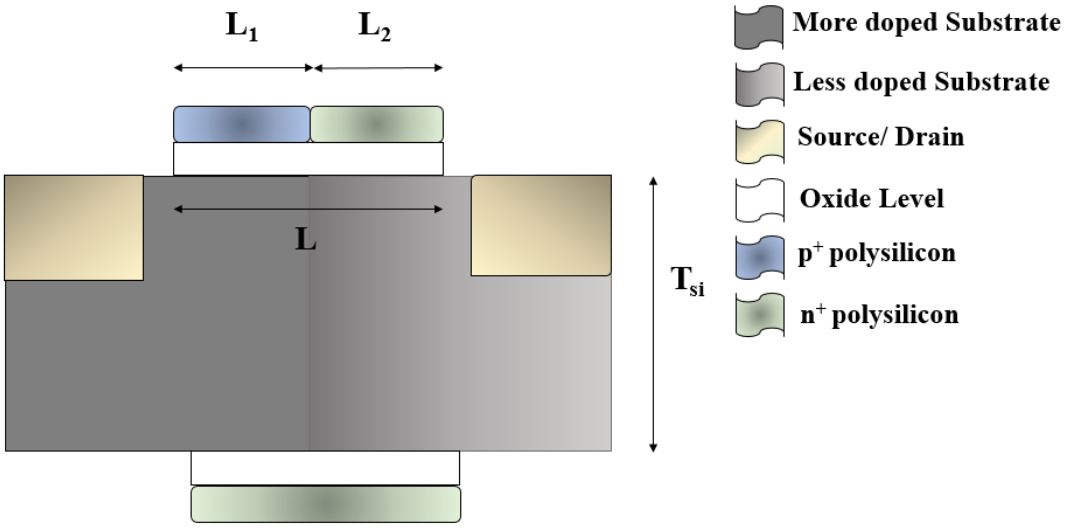

FIGURE 4.1. 2D Schematic view of the GCDMDG SOI MOSFET

$$\phi_{si2} = X_{si} + \left(\frac{E_g}{2q}\right) + \phi_{F2} \tag{4.5b}$$

Here, E_g is bandgap at 300K and ϕ_{F1} , ϕ_{F2} are the potentials function for the Fermi level for two different doping regions. The X_{si} defines the electron affinity of semiconductors. The expression can be written as,

$$\phi_{F_1} = V_T \ln\left(N_{a1}/n_i\right) \tag{4.6a}$$

and $$\phi_{F2} = V_T \ln\left(N_{a2}/n_i\right) \tag{4.6b}$$

Here, V_T is the thermal voltage explain in Eqn. 3.51a. n_i represents intrinsic carrier concentration and K defines the Boltzmann's constant. Surface potential under p^+ and n^+ polysilicons are explained as,

$$\phi_{gc1}(x,y) = \phi_{S1}(x) + a_{gc11}(x)y + a_{gc12}(x)y^2 \qquad 0 \le x \le L_1, 0 \le y \le T_{Si} \tag{4.7a}$$

$$\phi_{gc2}(x,y) = \phi_{S2}(x) + a_{gc21}(x)y + a_{gc22}(x)y^2 \quad L_1 \le x \le L_1 + L_2, 0 \le y \le T_{Si} \tag{4.7b}$$

where, $\phi_{S1}(x)$ and $\phi_{S2}(x)$ interpret the surface potential under p^+ polysilicon and n^+ polysilicon and $a_{gc11}(x), a_{gc12}(x), a_{gc21}(x), a_{gc22}(x)$ define arbitrary random constants depending on x . To solve the analytical model for the surface potential and electric field some boundary conditions (Eqn. 3.7-3.18) have to be considered.

From the boundary condition 5 (Eqn. 3.16), the surface potential at the source side can be explained as,

$$\phi_{gc1}(0,0) = \phi_{S1}(0) = V_{bi_1} \tag{4.8}$$

Built-in-potential for region 1 is

$$V_{bi_1} = (KT/q)\log\left(N_{a1}N_d/n_i^2\right) \tag{4.9a}$$

Built-in-potential for region 2 is

$$V_{bi_2} = (KT/q)\log\left(N_{a2}N_d/n_i^2\right) \tag{4.9b}$$

N_d is the source and drain doping concentration. From the boundary condition 6 (Eqn. 3.18), the surface potential at the drain side can be explained as,

$$\phi_2\left(L_1+L_2,0\right)=\phi_{s2}\left(L_1+L_2\right)=V_{bi_2}+V_{DS} \tag{4.10}$$

The t_{oxb} describes the width of the insulator used at the back gate, N_d demonstrates the doping concentration of source and drain region and V_{DS} defines the source-drain voltage (Vadthiya et al., 2018). For solving $a_{gc11}(x)$, $a_{gc12}(x)$ put $y=0$ in Eqn. 3.6,

$$\phi_{gc1}(x,y)=\phi_{S1}(x)+0+0 \tag{4.11}$$

Differentiating Eqn. 3.6a for GCDMDG with respect to y and put $y=0$,

$$\frac{d\phi_{gc1}(x,y)}{dy}|_{y=0}=0+a_{gc11}(x)+2a_{gc12}(x)y=a_{gc11}(x) \tag{4.12}$$

Comparing the Eqn. 4.12 with the first boundary condition, Eqn. 3.7, and simplifying it,

$$a_{gc11}(x)=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\phi_{S1}(x)-V_{GSf1}}{t_{ox}}\right) \tag{4.13}$$

Putting y=T_{si} in Eqn. 3.6a,

$$\phi_{gc1}(x,y)=\phi_{S1}(x)+a_{gc11}(x)T_{si}+a_{gc12}(x){T_{si}}^2 \tag{4.14}$$

At y=T_{si}, the back gate potential has to consider,

$$\phi_B(x,y)=\phi_{S1}(x)+a_{gc11}(x)T_{si}+a_{gc12}(x){T_{si}}^2 \tag{4.15}$$

Differentiating the Eqn. 4.15 with respect to y and comparing the equation with respect to Eqn. 3.10,

$$\frac{d\phi_B(x,y)}{dy}|_{y=T_{si}}=\frac{d\phi_{gc1}(x,y)}{dy}|_{y=T_{si}}=a_{gc11}(x)+2a_{gc12}(x)T_{si}=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{V_{GS,b}-\phi_B(x)}{t_{oxb}}\right)$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}}a_{gc11}(x)+\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc12}(x)T_{si}^2=V_{GS,b}-\phi_B(x) \tag{4.16}$$

Putting the value of $\phi_B(x)$ from Eqn. 4.15,

$$\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}}a_{gc11}(x)+\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{12}(x)T_{si}^2=V_{GS,b}-\left(\phi_{S1}(x)+a_{gc11}(x)T_{si}+a_{gc12}(x){T_{si}}^2\right)$$

$$\Rightarrow \frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc12}(x)T_{si}^2 = V_{GS,b} - \left(\phi_{S1}(x) + a_{gc11}(x)T_{si} + a_{gc12}(x)T_{si}^{\,2}\right) - \frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}}a_{gc11}(x) \quad (4.17)$$

Putting the value of $a_{gc11}(x)$ from Eqn. 4.13 in the Eqn. 4.17 and simplifying it,

$$\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc12}(x)T_{si}^2 = V_{GS,b} - \left\{\phi_{S1}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S1}(x) - V_{GSf}}{t_{ox}}\right)T_{si} + a_{gc12}(x)T_{si}^{\,2}\right\} - \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}}\left(\frac{\phi_{S}(x)_1 - V_{GSf}}{t_{ox}}\right)$$

$$\Rightarrow \frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc12}(x)T_{si}^2 = V_{GS,b} - \phi_{S1}(x)\left(1 + \frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right) + V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right) - a_{gc12}(x)T_{si}^2$$

$$\Rightarrow \frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc12}(x)T_{si}^2 + a_{gc12}(x)T_{si}^2 = V_{GS,b} - \phi_{S1}(x)\left(1 + \frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right) + V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)$$

$$\Rightarrow \left(2\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}} + 1\right)a_{gc12}(x)T_{si}^2 = V_{GS,b} - \phi_{S1}(x)\left(1 + \frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right) + V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)$$

$$\Rightarrow a_{gc12}(x) = \frac{V_{GS,b} - \phi_{S1}(x)\left(1 + \frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right) + V_{GSf1}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)}{\left(1 + 2\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}\right)T_{si}^2} \quad (4.18)$$

Considering, $c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $c_{oxb} = \frac{\varepsilon_{ox}}{t_{oxb}}$ and $c_{si} = \frac{\varepsilon_{si}}{T_{si}}$,

$$\Rightarrow a_{gc12}(x) = \frac{V_{GS,b} - \phi_{S1}(x)\left(1 + \frac{c_{ox}}{c_{si}} + \frac{c_{ox}}{c_{oxb}}\right) + V_{GSf1}\left(\frac{c_{ox}}{c_{si}} + \frac{c_{ox}}{c_{oxb}}\right)}{\left(1 + 2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (4.19)$$

Similarly, the constant terms $a_{gc21}(x)$, $a_{gc22}(x)$ can be solved, putting $y = 0$ in equation number 3.6b,

$$\phi_{gc2}(x,y) = \phi_{S2}(x) + 0 + 0$$

Differentiating Eqn. 3.6b with respect to y and putting $y = 0$,

$$\frac{d\phi_{gc2}(x,y)}{dy}|_{y=0} = 0 + a_{gc21}(x) + 2a_{gc22}(x)y = a_{gc21}(x)$$

Eqn. 4.18 is compared with the first boundary condition stated in Eqn. 3.8 and simplifying it,

$$a_{gc21}(x)=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\phi_{S2}(x)-V_{GSf2}}{t_{ox}}\right) \tag{4.20}$$

Putting $y=T_{si}$ in Eqn. 3.6b, the surface potential,

$$\phi_B(x,y)=\phi_{S2}(x)+a_{gc21}(x)T_{si}+a_{gc22}(x){T_{si}}^2$$

At $y=T_{si}$, the back gate potential has to be considered. Differentiating it with respect to y and comparing the equation with 2nd boundary condition given in Eqn. 3.11,

$$\frac{d\phi_{gc2}(x,y)}{dy}\Big|_{y=T_{si}}=\frac{d\phi_B(x,y)}{dy}\Big|_{y=T_{si}}=a_{gc21}(x)+2a_{gc22}(x)T_{si}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{V_{GS,b}-\phi_B(x)}{t_{oxb}}\right) \tag{4.21}$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}}a_{gc21}(x)+\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc22}(x)T_{si}^2=V_{GS,b}-\phi_B(x)$$

Putting the value of $\phi_B(x)$,

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}}a_{gc21}(x)+\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc22}(x)T_{si}^2=V_{GS,b}-\left(\phi_{S2}(x)+a_{gc21}(x)T_{si}+a_{gc22}(x){T_{si}}^2\right)$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc22}(x)T_{si}^2=V_{GS,b}-\left(\phi_{S2}(x)+a_{gc21}(x)T_{si}+a_{gc22}(x){T_{si}}^2\right)-\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}}a_{gc21}(x)$$

Putting the value of $a_{gc21}(x)$ from Eqn. 4.20 and simplifying it,

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc22}(x)T_{si}^2=V_{GS,b}-\left(\phi_{S2}(x)+\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\phi_{S2}(x)-V_{GSf2}}{t_{ox}}\right)T_{si}+a_{gc22}(x){T_{si}}^2\right)-\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}}\left(\frac{\phi_{S2}(x)-V_{GSf2}}{t_{ox}}\right)$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc22}(x)T_{si}^2=V_{GS,b}-\phi_{S2}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf2}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)-a_{gc22}(x)T_{si}^2$$

$$\Rightarrow\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}2a_{gc22}(x)T_{si}^2+a_{gc22}(x)T_{si}^2=V_{GS,b}-\phi_{S2}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf2}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)$$

$$\Rightarrow\left(2\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}+1\right)a_{gc22}(x)T_{si}^2=V_{GS,b}-\phi_{S2}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf2}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)$$

$$\Rightarrow a_{gc22}(x)=\frac{V_{GS,b}-\phi_{S2}(x)\left(1+\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)+V_{GSf2}\left(\frac{\varepsilon_{ox}T_{si}}{\varepsilon_{si}t_{ox}}+\frac{\varepsilon_{si}t_{oxb}\varepsilon_{ox}}{\varepsilon_{ox}\varepsilon_{si}t_{ox}}\right)}{\left(1+2\frac{\varepsilon_{si}t_{oxb}}{\varepsilon_{ox}T_{si}}\right)T_{si}^2} \tag{4.22}$$

Considering, $c_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$, $c_{oxb}=\frac{\varepsilon_{ox}}{t_{oxb}}$ and $c_{si}=\frac{\varepsilon_{si}}{T_{si}}$,

$$\Rightarrow a_{gc22}(x)=\frac{V_{GS,b}-\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)+V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \tag{4.23}$$

To calculate the surface potential under the p^+ polysilicon gate material for GCDMDG consider Eqn. 4.7a, $\phi_{gc1}(x,y)=\phi_{S1}(x)+a_{gc11}(x)y+a_{gc12}(x)y^2$. Putting the values of $a_{gc11}(x)$ and $a_{gc12}(x)$ from Eqn. 4.13 and 4.18,

$$\phi_{gc1}(x,y)=\phi_{S1}(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S1}(x)-V_{GSf1}}{t_{ox}}\right)y+\frac{V_{GS,b}-\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)+V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}y^2 \tag{4.24}$$

Differentiating the Eqn. 4.24 twice with respect to x,

$$\frac{d^2\phi_{gc1}(x,y)}{dx^2}=\frac{d^2\phi_{S1}(x)}{dx^2} \tag{4.25}$$

Differentiating the Eqn. 4.11 twice with respect to y,

$$\frac{d^2\phi_{gc1}(x,y)}{dy^2}=\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}+\frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \tag{4.26}$$

Putting the values of Eqn. 4.25 and 4.26 in the Poisson's equation, mentioned in Eqn. 4.1,

$$\frac{d^2\phi_{gc1}(x,y)}{dx^2}+\frac{d^2\phi_{gc1}(x,y)}{dy^2}=\frac{qN_{a1}}{\varepsilon_{si}}$$

$$\frac{d^2\phi_{S1}(x)}{dx^2}+\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}+\frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}=\frac{qN_{a1}}{\varepsilon_{si}}$$

$$\Rightarrow \frac{d^2\phi_{S1}(x)}{dx^2} - \frac{2\phi_{S1}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} = \frac{qN_{a1}}{\varepsilon_{si}} - \frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (4.27)$$

Putting,

$$\alpha = \frac{2\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \text{ and } \beta_{gc1} = \frac{qN_{a1}}{\varepsilon_{si}} - \frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \frac{2V_{GSf1}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (4.28)$$

Then,

$$\frac{d^2\phi_{S1}(x)}{dx^2} - \alpha\phi_{S1}(x) = \beta_{gc1} \quad (4.29)$$

To calculate the surface potential under the n^+ polysilicon gate material for GCDMDG consider Eqn. 4.7b, $\phi_{gc2}(x,y) = \phi_{S2}(x) + a_{gc21}(x)y + a_{gc22}(x)y^2$. Putting the values of $a_{gc21}(x)$ and $a_{gc22}(x)$ from Eqn. 4.19 and 4.23,

$$\phi_{gc2}(x,y) = \phi_{S2}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_{S2}(x)-V_{GSf2}}{t_{ox}}\right)y + \frac{V_{GS,b} - \phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right) + V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}y^2 \quad (4.30)$$

Differentiating Eqn. 4.30 twice with respect to x,

$$\frac{d^2\phi_{gc2}(x,y)}{dx^2} = \frac{d^2\phi_{S2}(x)}{dx^2} \quad (4.31)$$

Considering double derivatives of Eqn. 4.30 with respect to y,

$$\frac{d^2\phi_{gc2}(x,y)}{dy^2} = \frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} - \frac{2\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} + \frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (4.32)$$

Putting the values of Eqn. 4.31 and 4.32 in the Poisson's equation, mentioned in Eqn. 4.2,

$$\frac{d^2\phi_{gc2}(x,y)}{dx^2}+\frac{d^2\phi_{gc2}(x,y)}{dy^2}=\frac{qN_{a2}}{\varepsilon_{si}}$$

$$\Rightarrow \frac{d^2\phi_{S2}(x)}{dx^2}+\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}+\frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}=\frac{qN_{a2}}{\varepsilon_{si}}$$

$$\Rightarrow \frac{d^2\phi_{S2}(x)}{dx^2}-\frac{2\phi_{S2}(x)\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}=\frac{qN_{a2}}{\varepsilon_{si}}-\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (4.33)$$

Putting,

$$\alpha=\frac{2\left(1+\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \text{ and } \beta_{gc2}=\frac{qN_{a2}}{\varepsilon_{si}}-\frac{2V_{GS,b}}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2}-\frac{2V_{GSf2}\left(\frac{c_{ox}}{c_{si}}+\frac{c_{ox}}{c_{oxb}}\right)}{\left(1+2\frac{c_{si}}{c_{oxb}}\right)T_{si}^2} \quad (4.34)$$

Then,

$$\frac{d^2\phi_{S2}(x)}{dx^2}-\alpha\phi_{S2}(x)=\beta_{gc2} \quad (4.35)$$

4.2.1. Solution of Partial Differential Equation

From the Eqn. 4.29, $\frac{d^2\phi_{S1}(x)}{dx^2}-\alpha\phi_{S1}(x)=\beta_{gc1}$. Let $\phi_{S1}(x)=e^{mx}$, where $e^{mx}\neq 0$, so, the trial solution will be $\frac{d^2\phi_{S1}(x)}{dx^2}-\alpha\phi_{S1}(x)=0$. Now, $\phi_{S1}(x)=e^{mx}$, so, $\frac{d^2\phi_{S1}(x)}{dx^2}=m^2e^{mx}$. From the trial solution,

$$m^2e^{mx}-\alpha e^{mx}=0$$

$$\Rightarrow e^{mx}\left(m^2-\alpha\right)=0 \quad \text{as} \quad e^{mx}\neq 0$$

$$\Rightarrow \left(m^2-\alpha\right)=0$$

$$\Rightarrow m^2=\alpha$$

$$\Rightarrow m = \pm\sqrt{\alpha}$$

So, the roots are real and distinct. Now the C.F are

$$\text{C.F} \Rightarrow x_c = A_{gc}e^{\sqrt{\alpha}x} + B_{gc}e^{-\sqrt{\alpha}x} \tag{4.36}$$

Where, A_{gc} and B_{gc} are two arbitrary constants. P.I of the Eqn. 4.36 is

$$\text{P.I} = \frac{1}{D^2 - \alpha}\beta_{gc1} \tag{4.37}$$

[if, $\frac{d}{dx} = D$ and $\frac{d^2}{dx^2} = D^2$, then $\frac{d^2\phi_{S1}(x)}{dx^2} - \alpha\phi_{S1}(x) = \beta_{gc1}$ can be written as $\left(D^2 - \alpha\right)\phi_{S1}(x) = \beta_{gc1}$]

$$\Rightarrow \frac{1}{-\alpha\left(1 - \frac{D^2}{\alpha}\right)}\beta_{gc1}$$

$$= -\frac{1}{\alpha}\left(1 - \frac{D^2}{\alpha}\right)^{-1}\beta_{gc1}$$

$$= -\frac{1}{\alpha}\left(1 + \frac{D^2}{\alpha}\right)\beta_{gc1} \qquad \text{[Binomial expansion]}$$

$$= -\frac{\beta_{gc1}}{\alpha} \qquad \text{[Taking the derivatives]}$$

So, the complete equation will be $\phi_{S1}(x)$=C.F+P.I

$$\phi_{S1}(x) = A_{gc}e^{\sqrt{\alpha}x} + B_{gc}e^{-\sqrt{\alpha}x} - \frac{\beta_{gc1}}{\alpha}$$

$$\Rightarrow \phi_{S1}(x) = A_{gc}e^{\lambda x} + B_{gc}e^{-\lambda x} + \sigma_1 \quad [\text{putting } \sqrt{\alpha} = \lambda \text{ and } -\frac{\beta_{gc1}}{\alpha} = \sigma_1] \tag{4.38}$$

Similarly, $\phi_{S2}(x) = C_{gc}e^{\lambda(x-L_1)} + D_{gc}e^{-\lambda(x-L_1)} + \sigma_2$ [putting $-\frac{\beta_{gc2}}{\alpha} = \sigma_2$] (4.39)

From the boundary condition in Eqn. 3.14 for GCDMDG,

$$\phi_{gc1}(L_1, 0) = \phi_{gc2}(L_1, 0)$$

Putting the values in Eqn. 4.38 and 4.39,

$$A_{gc}e^{\lambda L_1} + B_{gc}e^{-\lambda L_1} + \sigma_1 = C_{gc}e^{\lambda(L_1 - L_1)} + D_{gc}e^{-\lambda(L_1 - L_1)} + \sigma_2$$

$$\Rightarrow A_{gc}e^{\lambda L_1} + B_{gc}e^{-\lambda L_1} + (\sigma_1 - \sigma_2) = C_{gc} + D_{gc} \tag{4.40}$$

From the boundary condition Eqn. 3.15,

$$\frac{d\phi_{gc1}(x,y)}{dx}|_{x=L_1} = \frac{d\phi_{gc2}(x,y)}{dx}|_{x=L_1}$$

Putting the values of $\phi_{S1}(x)$, $\phi_{S2}(x)$ in Eqn. 4.38 and 4.39 and consider the derivatives of the surface potentials,

$$\frac{d\phi_{S1}(x)}{dx}|_{x=L_1} = \lambda A_{gc} e^{\lambda L_1} - \lambda B_{gc} e^{-\lambda L_1}$$

$$\Rightarrow \frac{d\phi_{S1}(x)}{dx}|_{x=L_1} = \lambda\left(A_{gc} e^{\lambda L_1} - B_{gc} e^{-\lambda L_1}\right) \quad (4.41)$$

Similarly, $\frac{d\phi_{S2}(x)}{dx}|_{x=L_1} = \lambda C_{gc} e^{\lambda(L_1-L_1)} - \lambda D_{gc} e^{-\lambda(L_1-L_1)}$

$$\Rightarrow \frac{d\phi_{S2}(x)}{dx}|_{x=L_1} = \lambda\left(C_{gc} - D_{gc}\right) \quad (4.42)$$

According to boundary condition Eqn. 3.15,

$$\frac{d\phi_{S1}(x)}{dx}|_{x=L_1} = \frac{d\phi_{S2}(x)}{dx}|_{x=L_1} = \lambda\left(C_{gc} - D_{gc}\right) = \lambda(A_{gc} e^{\lambda L_1} - B_{gc} e^{-\lambda L_1})$$

$$\Rightarrow (C_{gc} - D_{gc}) = (A_{gc} e^{\lambda L_1} - B_{gc} e^{-\lambda L_1}) \quad (4.43)$$

Solving Eqn. 4.42 and 4.43 the final values of the constants are

$$C_{gc} = \left(A_{gc} e^{\lambda L_1} + \frac{\sigma_1 - \sigma_2}{2}\right) \quad (4.44)$$

And $D_{gc} = \left(B_{gc} e^{-\lambda L_1} + \frac{\sigma_1 - \sigma_2}{2}\right)$ (4.45)

Again from boundary conditions of Eqn. 3.16 and 3.18,

$$\phi_{gc1}(0,0) = \phi_{S1}(0) = V_{bi_1} \text{ and } \phi_{gc2}(L_1 + L_2, 0) = \phi_{S2}(L_1 + L_2) = V_{bi_2} + V_{DS} \quad (4.46)$$

Putting the values in equation,

$$\phi_{S1}(x) = A_{gc} e^{\lambda x} + B_{gc} e^{-\lambda x} + \sigma_1$$

$$\Rightarrow \phi_{S1}(0) = A_{gc} e^{\lambda 0} + B_{gc} e^{-\lambda 0} + \sigma_1$$

$$\Rightarrow \phi_{S1}(0) = A_{gc} + B_{gc} + \sigma_1 = V_{bi_1}$$

$$\Rightarrow B_{gc} = V_{bi_1} - A_{gc} - \sigma_1 \quad (4.47a)$$

$$\Rightarrow A_{gc} = V_{bi_1} - B_{gc} - \sigma_1 \quad (4.47b)$$

From another condition, Eqn. 3.18, putting the values,

$$\phi_{S2}(x) = C_{gc}e^{\lambda(x-L_1)} + D_{gc}e^{-\lambda(x-L_1)} + \sigma_2$$

$$\Rightarrow \phi_{S2}(L_1+L_2) = C_{gc}e^{\lambda(L_1+L_2-L_1)} + D_{gc}e^{-\lambda(L_1+L_2-L_1)} + \sigma_2 = V_{bi_2} + V_{DS}$$

$$\Rightarrow \phi_{S2}(L_1+L_2) = C_{gc}e^{\lambda(L_2)} + D_{gc}e^{-\lambda(L_2)} + \sigma_2 = V_{bi_2} + V_{DS}$$

Putting the values of C_{gc} and D_{gc} from Eqn. 4.44 and 4.45,

$$\phi_{S2}(L_1+L_2) = \left(A_{gc}e^{\lambda L_1} + \frac{\sigma_1-\sigma_2}{2}\right)e^{\lambda(L_2)} + \left(B_{gc}e^{-\lambda L_1} + \frac{\sigma_1-\sigma_2}{2}\right)e^{-\lambda(L_2)} + \sigma_2 = V_{bi_2} + V_{DS}$$

$$\Rightarrow A_{gc}e^{\lambda L_1}e^{\lambda(L_2)} + \frac{\sigma_1-\sigma_2}{2}e^{\lambda(L_2)} + Be^{-\lambda L_1}e^{-\lambda(L_2)} + \left(\frac{\sigma_1-\sigma_2}{2}\right)e^{-\lambda(L_2)} + \sigma_2 = V_{bi_2} + V_{DS}$$

$$\Rightarrow A_{gc}e^{\lambda L} + B_{gc}e^{-\lambda L} + \frac{\sigma_1-\sigma_2}{2}\left(e^{\lambda(L_2)} + e^{-\lambda(L_2)}\right) = V_{bi_2} + V_{DS} - \sigma_2$$

$$\Rightarrow A_{gc}e^{\lambda L} + B_{gc}e^{-\lambda L} + (\sigma_1-\sigma_2)\cosh(\lambda L_2) = V_{bi_2} + V_{DS} - \sigma_2 \quad (4.48)$$

Now put the value of B_{gc} from Eqn. 4.47b,

$$\Rightarrow A_{gc}e^{\lambda L} + \left(V_{bi_1} - A_{gc} - \sigma_1\right)e^{-\lambda L} + (\sigma_1-\sigma_2)\cosh(\lambda L_2) = V_{bi_2} + V_{DS} - \sigma_2 \quad (4.49)$$

$$\Rightarrow A_{gc}e^{\lambda L} - A_{gc}e^{-\lambda L} + \left(V_{bi_1} - \sigma_1\right)e^{-\lambda L} + (\sigma_1-\sigma_2)\cosh(\lambda L_2) = V_{bi_2} + V_{DS} - \sigma_2$$

$$\Rightarrow A_{gc} = \left\{\left(V_{bi_2} + V_{DS} - \sigma_2\right) - \left(V_{bi_1} - \sigma_1\right)e^{-\lambda L} - (\sigma_1-\sigma_2)\cosh(\lambda L_2)\right\}\frac{e^{-\lambda L}}{\left(1-e^{-2\lambda L}\right)} \quad (4.50)$$

Putting the value of A_{gc} from Eqn. 4.47b and 4.48,

$$A_{gc}e^{\lambda L} + B_{gc}e^{-\lambda L} + (\sigma_1-\sigma_2)\cosh(\lambda L_2) = V_{bi_2} + V_{DS} - \sigma_2$$

$$\Rightarrow \left(V_{bi_1} - B_{gc} - \sigma_1\right)e^{\lambda L} + B_{gc}e^{-\lambda L} + (\sigma_1-\sigma_2)\cosh(\lambda L_2) = V_{bi_2} + V_{DS} - \sigma_2$$

$$\Rightarrow \left(V_{bi_1} - \sigma_1\right)e^{\lambda L} - B_{gc}e^{\lambda L} + B_{gc}e^{-\lambda L} + (\sigma_1-\sigma_2)\cosh(\lambda L_2) = V_{bi_2} + V_{DS} - \sigma_2$$

$$\Rightarrow B_{gc}\left(e^{\lambda L} - e^{-\lambda L}\right) = \left(V_{bi_1} - \sigma_1\right)e^{\lambda L} - \left(V_{bi_2} + V_{DS} - \sigma_2\right) + (\sigma_1-\sigma_2)\cosh(\lambda L_2)$$

$$\Rightarrow B_{gc} = \left\{\left(V_{bi_1} - \sigma_1\right)e^{\lambda L} - \left(V_{bi_2} + V_{DS} - \sigma_2\right) + (\sigma_1-\sigma_2)\cosh(\lambda L_2)\right\}\frac{e^{-\lambda L}}{\left(1-e^{-2\lambda L}\right)} \quad (4.51)$$

The electric field can be found out from the derivative of surface potential expression. The electric fields for two different regions have been discussed in Chapter 3 (Eqn. 3.66a and 3.66b),

$$E_{gc1}(x)=\frac{d\phi_{S1}(x)}{dx}|_{y=0}=A_{gc}\lambda e^{\lambda x}-B_{gc}\lambda e^{-\lambda x},\ 0\le x\le L_1 \quad \text{under } M_1 \text{ and}$$

$$E_{gc2}(x)=\frac{d\phi_{S2}(x)}{dx}|_{y=0}=C_{gc}\lambda e^{\lambda(x-L_1)}-D_{gc}\lambda e^{-\lambda(x-L_1)},\ L_1\le x\le L \quad \text{under } M_2 \qquad (4.52)$$

If the temperature of the device is changed it affects its bandgap energy, doping concentrations, and thermal voltage. These constraints automatically change the surface potential and electric field. The effect of temperature on the model has been discussed in detail in Eqn. 3.59-3.62. That properties are also incorporated in the GCDMDG MOSFET structure and the changes are compared. The Si-HfO_2 interface introduces interface charge density that has been considered here. The respective model is described in Eqn. 3.63-3.65. For better compatibility gate stack concept has been introduced in the model (Eqn. 1.4).

4.3. Results and Discussions

To analyze the recommended analytical model for fully depleted GCDMDG MOSFET and the TCAD synthesis of the surface potential and electric field variation throughout the channel of the structure, different design parameter values have been considered (Table 4.1). All design parameters data, namely doping concentration for two regions, has been taken from (Goel et al. 2016; Reddy, 2005; Narang, 2013) and voltage dimension has been considered from (Contreras et al. 2010). In contrast to the DMDG structure with GCDMDG, the model for this case was developed from Table 3.1. The proposed structure has shown excellent conformity with the results of TCAD simulation.

Figure 4.2 represents the evaluation of surface potential in contrast with the position of the channel for GCDMDG device, using SiO_2 and HfO_2 as the oxide materials. It is found that like DMDG structure two separate lobes have been generated in the surface potential. Also, the two lobes are of two different values. As a result, a clear step like function has been formed. It also depicts that using high-k material, the value of the surface potential is lowered than using SiO_2 material. Not only that, but also the nature of the characteristics using high-k is more flattened than the material which is conventionally used, whereas the peak values at the drain side are found to be the same.

Table 4.1: Design Parameter Values for GCDMDG Potential

Sl. No.	Parameters	Values
1.	N_a - Uniform body doping concentration	1×10^{15} cm^{-3}
2.	N_{a1} - Doping concentration near source side	1×10^{17} cm^{-3}
3.	N_{a2} - Doping concentration near drain side	1×10^{16} cm^{-3}
4.	N_d - Source/ Drain doping concentration	5×10^{19} cm^{-3}
5.	L - Device channel length	100 nm
6.	L_1 - Gate length of M_1 p^+ Polysilicon	50 nm
7.	L_2 - Gate length of M_2 n^+ Polysilicon	50 nm
8.	T_{si} - Thickness of film	12 nm
9.	n_i - Intrinsic carrier concentration	1.5×10^{10} cm^{-3}
10.	t_{ox} - Gate oxide thickness	1 nm
11.	t_{oxb} - Back gate oxide thickness	1 nm
12.	V_{DS} - Drain source voltage	0.8 V
13.	V_{GS} - Gate source voltage	0.15 V
14.	α - Arbitrary Constant	4.73×10^{-4} eV/K
15.	β - Arbitrary Constant	636 K
16.	Q_0 - Interface charge	1.6×10^{-9} C/cm^2

It has been discussed in the previous chapter, that the step like function has been generated due to the presence of two different work functioned materials at the gate. The GCDMDG structure is comprised of DG and DMG structures. So the lower lobe is generated at the high work function material and the higher lobe is generated at the lower work function material. It has also been found that keeping the other parameters are same, the generated surface potential is lower using high-k material than SiO_2.

Thus, it can be concluded that for small dimensions using high-k in the device, better characteristics can be achieved which may help to overcome the short channel effects. Both DMDG SOI MOSFET and GCDMDG SOI MOSFET devices generate the step like surface potential characteristics due to different work function elements at the gate.

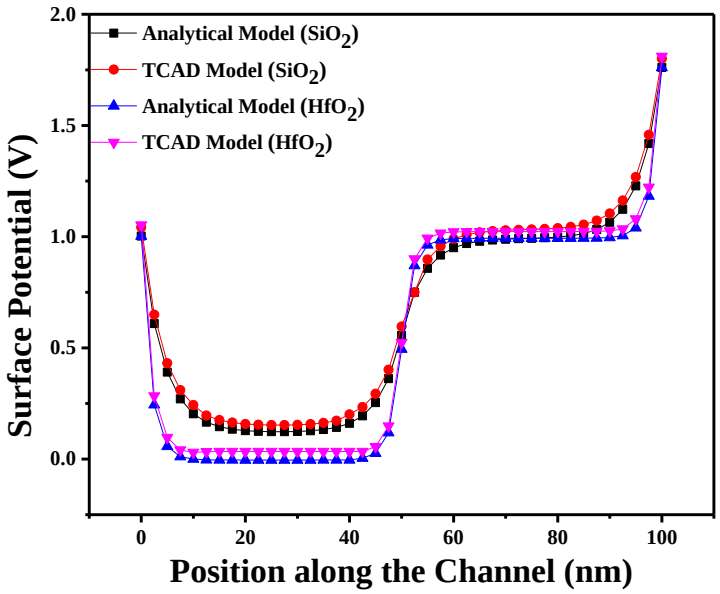

FIGURE 4.2. Change of surface potential with the channel position

Figure 4.3 signifies a comparative study of surface potential with different positions of the channel between (a) DMDG and (b) GCDMDG structures for identical parameters mainly with similar oxide thickness using conventional and high-k oxide materials SiO_2 and HfO_2. The generated value of the surface potential is higher for graded channel DMDG structure over uniform doping DMDG structure. It is also revealed from the figure that the lowest value of the surface potential is closer to the source side for both DMDG and GCDMDG structures. In accordance with GCDMDG structure the surface potential rises because of different doping concentrations present at the substrate region. It is found that the GCDMDG structure introduces the highest value of surface potential over others (Goel et al., 2016). It helps to produce the highest threshold voltage and reduces the unwanted current that is usually generated due to SCE. It is clearly evident from the results obtained that using high-k material the surface potential becomes negative for DMDG structure. The negative value of the

surface potential may create a negative threshold voltage which will change the device characteristics. GCDMDG's structural properties help to modify it. The lowest value of the surface potential near the source side provides better screening of the channel over the drain to source voltage. The surface potential generated using high-k materials like HfO_2 is smaller than SiO_2. So, there will be a choice to enhance the oxide thickness value using HfO_2 to produce a similar surface potential like SiO_2. Using of GCDMDG structure, a better device performance can be achieved

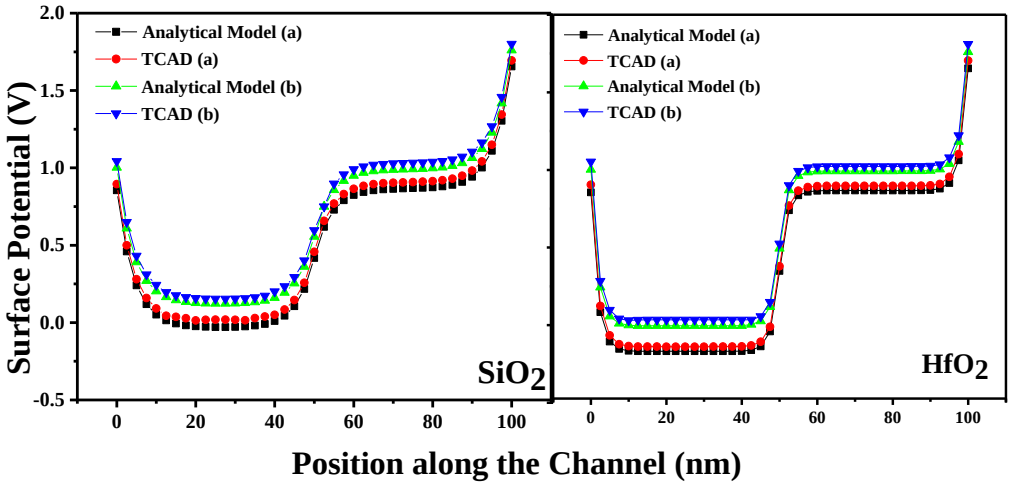

FIGURE 4.3. Change of surface potential with the channel position

As discussed in Chapter 3, with the change of temperature, the values of some essential parameters integrated into the surface potential are changed. These changes have an enormous impact on surface potential. Fig. 4.4 represents the change of surface potential with the position along with the graded channel DMDG structure at different temperatures. With increasing temperature, the surface potential goes up irrespective of the position along the channel as well as oxide materials. Using the boundary conditions and other relative expressions with bandgap energy, carrier concentration, thermal voltage, etc. that are required to construct the surface potential expressions are also changed with temperature. As a result, the surface potential also increases. But in the case of high-k material the increment is lesser than using SiO_2 keeping other parameters same. For both the devices, i.e. DMDG and GCDMDG structure, the surface potential increases with the increment of temperature. At very high temperature (Fig. 4.5) (near about 410k) the surface potential of the GCDMDG

structure increases more than DMDG, whereas at low temperature the difference between them is negligible. Thus, it is evident that with the increment of temperature the difference becomes prominent.

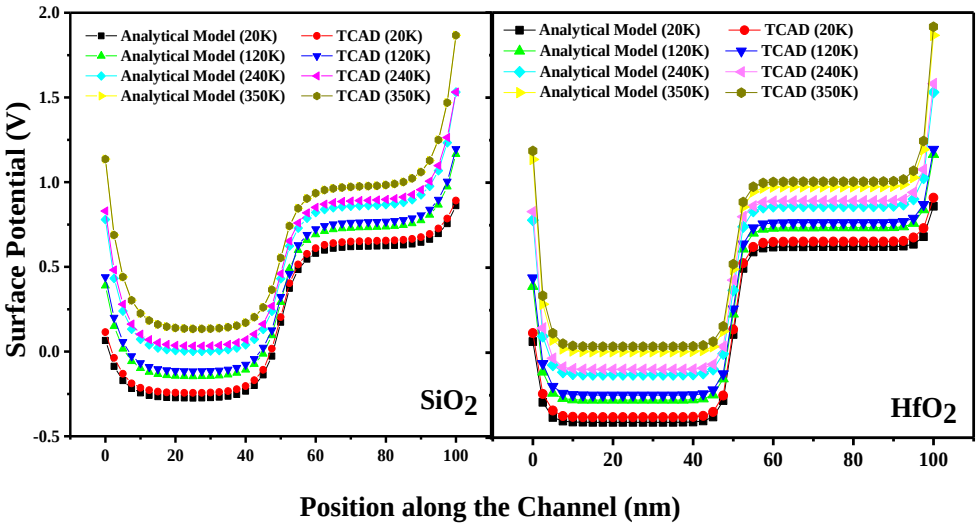

FIGURE 4.4. Surface potential with position along the channel for GCDMDG at different temperatures

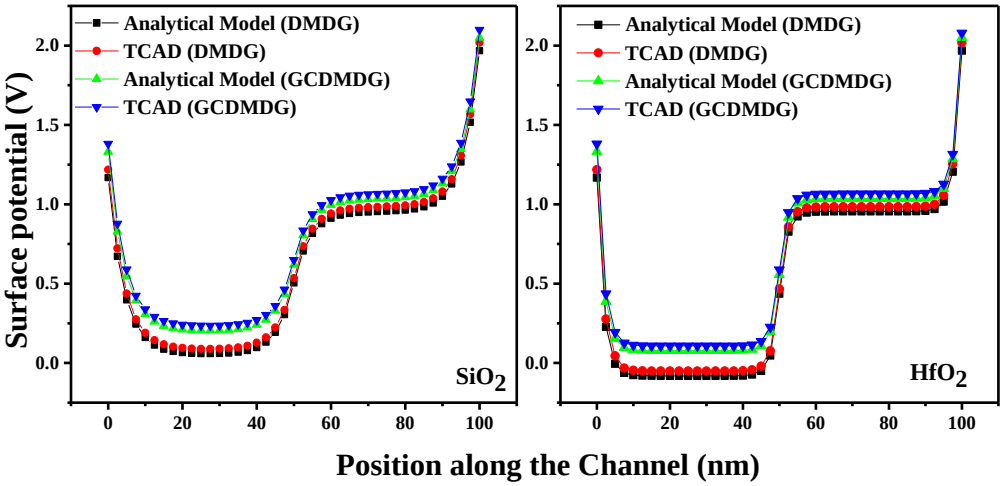

FIGURE 4.5. Comparison of surface potential with position along the channel for high temperature (410K)

Oxide thickness is an important parameter to control the SCEs. In the small scale dimension, the thickness of the oxide level is smaller and could not behave like an insulator. As a result of SCE increases which is evident from Fig. 4.6. Again with decreasing value of oxide thickness the surface potential with respect to position across

the channel also decreases. This particular nature of the surface potential helps to generate a low value of threshold voltage. Low threshold voltage increases unwanted current which is generated due to SCEs. Using high-k material, the generated surface

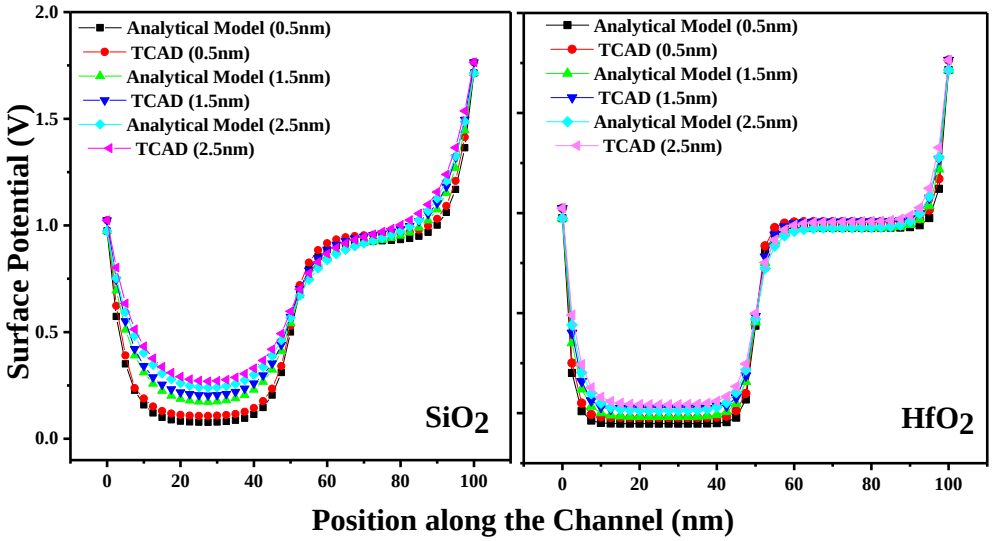

FIGURE 4.6. Development of surface potential with position of the channel for different oxide thickness

potential is lower compared to SiO_2. So to produce the same surface potential, the oxide thickness can be increased using high-k and minimize the SCE problems.

The gate voltage is a vital factor for any device performance. By applying the proper gate voltage the device changes its mode from accumulation to the inversion region. The gate voltage also helps in channel formation at the inversion region. It supports to increase the amount of drain current flow through the channel before punch through. It is observed from Fig. 4.7 that with increasing gate voltage the potential increases. With the applied gate voltage a large number of negative carriers are induced at the channel region. The applied voltage and charged particles increase the potential difference between them.

The surface potential characteristics with position along the channel for different control (L_1) to screen gate length (L_2) ratio is represented in the Fig. 4.8. The source to channel barrier height changes with the increasing ratio of L_1 and L_2. It can also be stated that the minimum value of the surface potential is shifted with them irrespective of the oxide material. On the other hand, the peak value at the drain side is decreased

with the decreasing ratio. Thus, it can be concluded from the illustration that with the shifting of minimum surface potential, the threshold voltage is also shifted with an increasing ratio of control to screen gate ratio. Shifting of threshold voltage towards drain side may reveal the optimizing threshold voltage roll off whereas the DIBL effects can be reduced with decreasing length ratio (Goel et al., 2016).

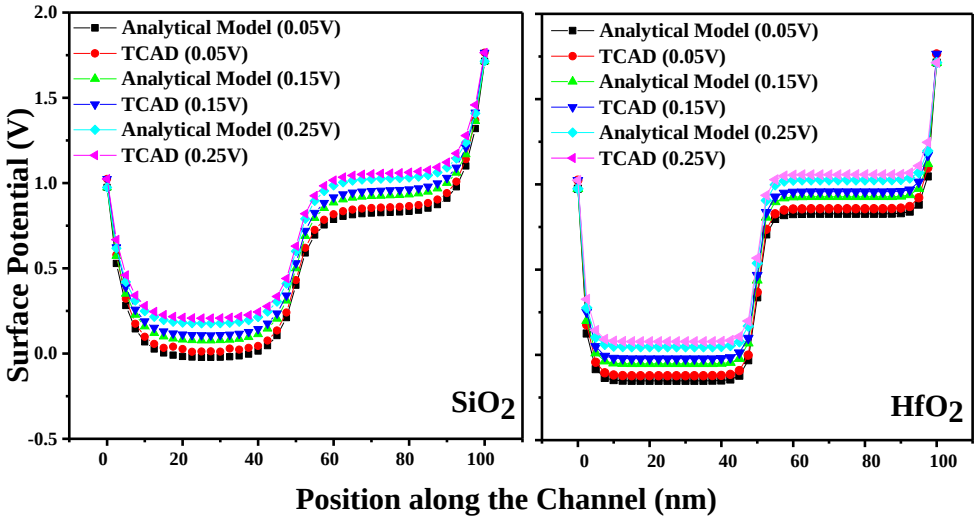

FIGURE 4.7. Surface potential characteristics with position along the channel for different gate source voltage

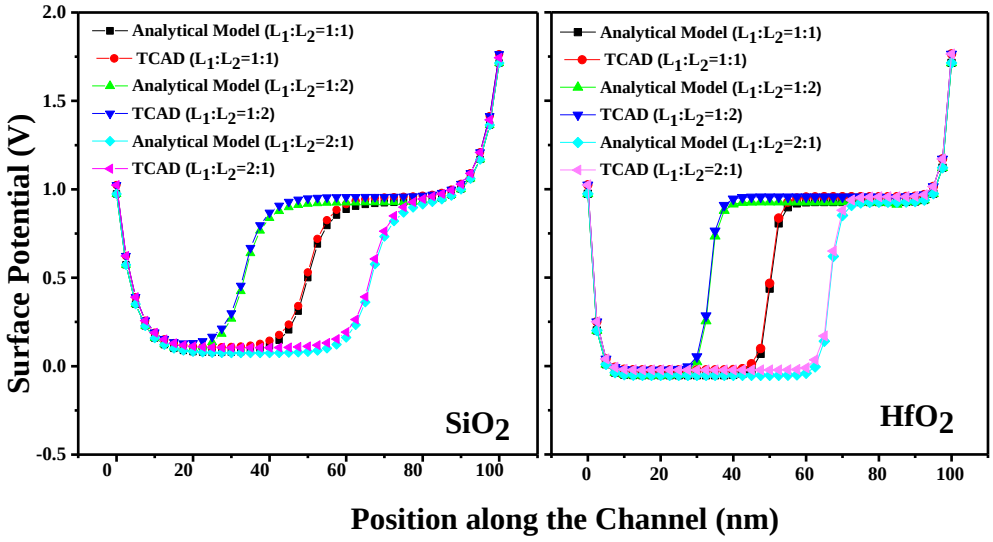

Figure 4.8. Surface potential characteristics with position along the channel for different channel length ratio

The oxide layer over the Si substrate of the device generates a Si-SiO_2 interface. This type of interface also generates some interface charge, in between them at the time of fabrication. Interface charge has a lot of influence over the device performance depicted in Fig. 4.9. In view of the effect, the surface potential characteristics have been compared in between the two device structures. For simplicity, only the positive value of interface charge has been considered here. Figure 4.9 illustrates that the surface potential increases when the interface charges are incorporated in the device structure for both oxide materials. According to Suddapalli and Nistala (Suddapalli & Nistala, 2021), with the increasing surface potential of GCDMDG structure for the positive value of the interface charge, the minimum value of the surface potential also increases. As a consequence, the roll off nature of the threshold voltage decreases. Sometimes the minimum central potential value shifts to the drain side which helps to minimize the DIBL effect.

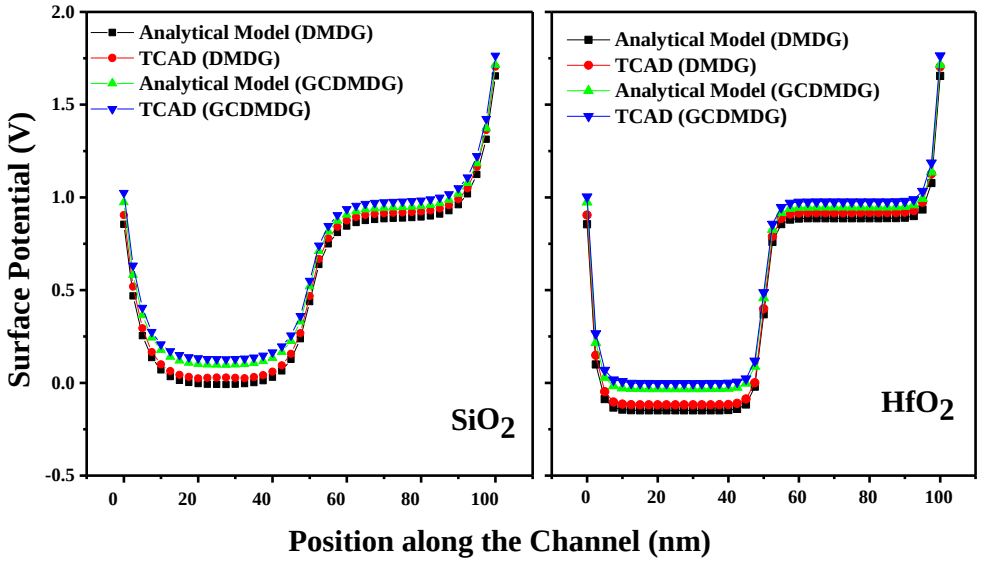

FIGURE 4.9. Surface potential with position along the channel including interface charge

The variation of the electric field with position along the channel for the GCDMDG structure has been illustrated in Fig. 4.10. The generated characteristics show the step function irrespective of the oxide material. It is revealed that the average

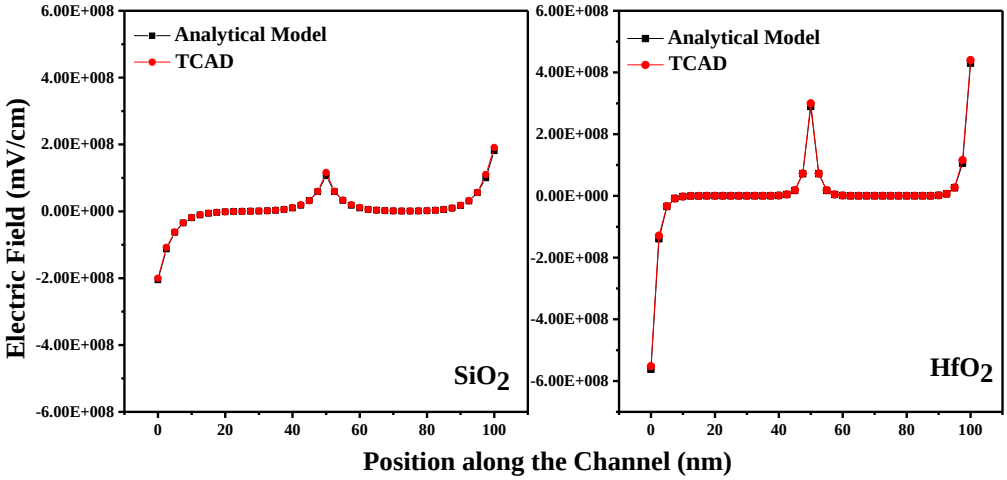

Figure 4.10. The electric field with position along the channel for GCDMDG

electric field is almost zero throughout the channel except for adjacent to the source and drain channel junction. However, the magnitude of the electric field increases with the high-k material. Normally the electric field is generated from the surface potential. So the step like function is produced due to the presence of two different materials with different work functions at the gate (Goel et al., 2016; Kumar & Chaudhry, 2004). Comparing with the electric field of the DMDG structure (Chapter 3), the GCDMDG structure does not show any significant change. At high temperature, the magnitude of the field becomes higher at the vicinity of the drain channel junction and lower at the source-channel junction than low temperature but the average value is constant at zero level, which has been observed in Fig. 4.11.

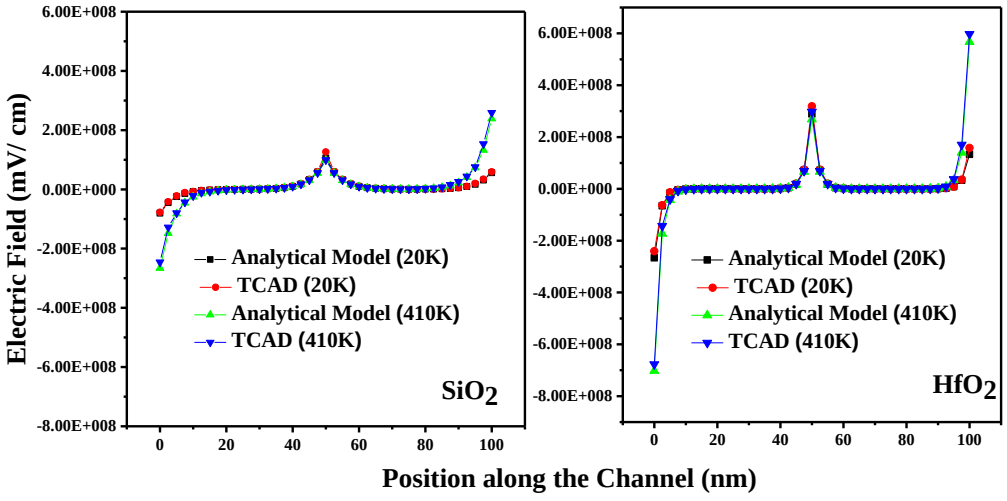

FIGURE 4.11. The electric field with position along the channel for different temperature of GCDMDG structure

4.4. Summary

Scaling down the device has the challenge to shrink several parameters of it. It introduces some complications in the device. Reduction of the width of the gate oxide increases the gate tunneling effect. To overcome such type of difficulties, the effective oxide thickness should be improved without converting the device dimension. Using SiO_2 material oxide interface, the device has some limitations. In accordance with HfO_2, the oxide thickness can be improved of the DMDG structure without inducing the surface potential. Using different doping concentrations at substrate the graded channel DMDG structure can be formed. At different temperatures, the surface potential for the GCDMDG structure can also be increased for the minimum thickness value of the oxide level. It has no such effect on the electric field of DMDG structure. Comparing to the SMDG structure, in the DMDG and GCDMDG structures, the electric field decreases at the drain side which helps to generate fewer amount of hot carriers in the channel and reduces the impact ionization. Thus, the GCDMDG structure provides maximum advantage over the DMDG structure as it improves the short channel immunity, increases the controllability of the gate, carrier transportability in addition with reducing the hot carrier movements. From the figures, it can be concluded that the highest source-channel potential barrier (i.e., large threshold voltage) among DMDG, SMDG, and GCDMDG structures can be achieved only in the GCDMDG structure. It reduces the SCEs that have been generated due to the scaling of the device structure. Also by using GCDMDG structure HCEs, DIBL effects can be decreased. Among all the three MOSFET devices under study, GCDMDG MOSFET has the highest immunity to SCEs and related HCEs. Thus, most of the difficulties that are normally generated due to the scaling down of the device can be eliminated if the GCDMDG structure combines with a high-k material.

CHAPTER

5

Threshold Voltage

5.1. Introduction

The threshold voltage is a very important parameter for any device. It is the minimum value of the gate to source voltage of the MOSFET that is needed to create a conducting path between the source and drain terminals (Neamen, 1992; Nicollian et al., 1982). It is also an important scaling factor to maintain power efficiency at which the device turns on and starts to conduct. When the gate voltage is above the threshold voltage, the "enhancement-mode" transistor is turned on. Sufficient amount of charge particles accumulate at the channel that has been generated at the oxide silicon interface and they start to diffuse from source to drain (Cerdeira et al., 2008; A. Cerdeira et al., 2008; Chiang, 2016; Francis et al., 1994; Maity et al., 2015; Suzuki et al., 1995; Tsormpatzoglou et al., 2007). On account of applied bias between source and drain the charged particles move in specific directions and current starts to flow. In this chapter, the threshold voltage for DMDG and GCDMDG structures has been established.

DMDG (Kumar & Chaudhry, 2004; Kumar & Reddy, 2004; Kumar et al., 2016; Narendar & Girdhardas, 2018) architecture, where the potential profile of the surface region is modified to enhance the efficiency of electron transport, improves the transconductance and drop down the drain conductance. In the DMDG structure (Chaudhry & Kumar, 2004b; Chen & Kuo, 1996; Goel et al., 2016; Jin et al., 2010; N P Maity et al., 2019; Noor et al., 2016; Reddy & Kumar, 2005; Schaller, 2004) there are two threshold voltages for two different gate materials (p^+ and n^+ polysilicon) (Kaur et al., 2008; Maity et al., 2017; Maity et al., 2018; N. Maity, R. Maity, & S. Baishya,

2019; N. Maity, R. Maity, S. Maity, et al., 2019; Maity et al., 2011; Maity et al., 2016; Narendar & Girdhardas, 2018). One of them is dependent and the other one is independent with several device parameters (oxide thickness, channel length, temperature, etc.). Threshold voltage can also be calculated from a minimum value of the surface potential of the device. The minimum surface potential will be generated under the high work functioned gate region. As p^+ polysilicon has a higher work function than n^+ polysilicon so the minimum value of surface potential lies under p^+ polysilicon region, hence the threshold voltage. The threshold voltage that has been generated for n^+ polysilicon gate material has a higher value and is independent. The lower one varies with the several device constraints and it is considered as the prime threshold voltage for DMDG device.

In GCDMDG structure, due to the dual-material gate, two threshold voltages are present (Kaur et al., 2008). These values are higher than DMDG. In this structure the threshold voltage decreases at a very small value of channel length (10 nm), and increases several SCEs. These problems can be overcome using GCDMDG structure (Narendar & Girdhardas, 2018). The threshold voltages remain almost constant with the channel length (N. Maity, R. Maity, & S. Baishya, 2019) and no rolling off nature can be seen. The model has been established by varying several criteria like channel length, film thickness, oxide thickness, temperature change, work function difference and drain source voltage, so that a clear reflection can be seen how the threshold voltage (Suzuki & Sugii, 1995) changes with several parameters. In this chapter, the DIBL(Khan et al., 2008) and subthreshold swing (SS) (Abd El Hamid et al., 2007; Tosaka et al., 1994) have also been estimated for the device structure. Better performance can be seen using high-k material (Chaudhry & Kumar, 2004a; Maity et al., 2018; Niladri Pratap Maity et al., 2019; Salmani-Jelodar et al., 2016). To remove the interface charge, the gate stack concept has also been incorporated here (Maity et al., 2020; Maity et al., 2016). A very thin SiO_2 layer has been established below the high-k material so that Si-SiO_2 bonding is very good and generates a minimum interface charge. In the first part, the threshold voltage of the DMDG structure has been established and discussed its variations with several factors.

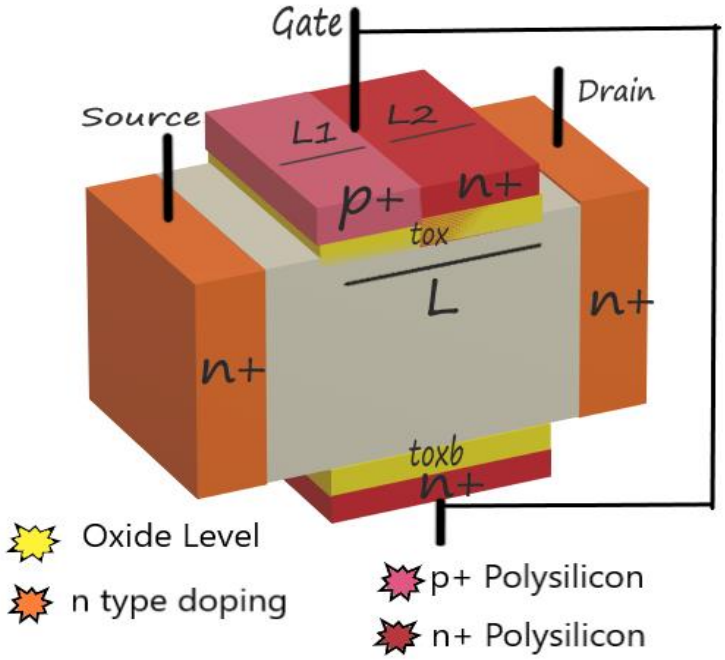

FIGURE 5.1. 3D representation of an asymmetric SOI DMDG structure

5.2. Analytical Model of Threshold Voltage for DMDG MOSFET

In SOI DMDG structure (Fig. 5.1), p^+ and n^+ polysilicon have been used at the top gate and n^+ polysilicon is used at the back gate. To generate a simplified analytical model, this structure can be considered as two DG structures. One structure is with p^+ polysilicon at the top gate and n^+ polysilicon at the bottom gate and another structure is with n^+ and n^+ polysilicon at the top and bottom gate, respectively (illustrated in Fig. 5.2). Threshold voltage V_{th} can be defined by the interaction between two gates. This type of DMDG structure generates two threshold voltages for two different gate materials, V_{th_1} and V_{th_2} respectively.

V_{th_1} generated for p^+-n^+ DG MOSFET and V_{th_2} is generated for n^+-n^+ MOSFET. The threshold voltage can be defined by the work function of the gate materials. As the work function of the p^+ polysilicon is higher than n^+, so the minimum value of the surface potential lies under the p^+ polysilicon region. The threshold voltage is very much depends on the minimum value of the surface potential so V_{th_1} has a smaller value than V_{th_2}, whereas the resultant threshold voltage of the device depends on the

combination of these two values. V_{th_1} can vary with t_{ox} and T_{si} of the device but V_{th_2} is insensitive to these parameters and it has a constant value of 1V.

Same t_{ox} applied for both gates, the channel doping concentration N_a is constant throughout the channel and the same gate source voltage applied for both the gates. Researcher Suzuki has explained about threshold voltage in DG MOSFET (Khan et al., 2008) in which the potential distribution in the subthreshold region is almost constant and it is shifted with the applied gate voltage.

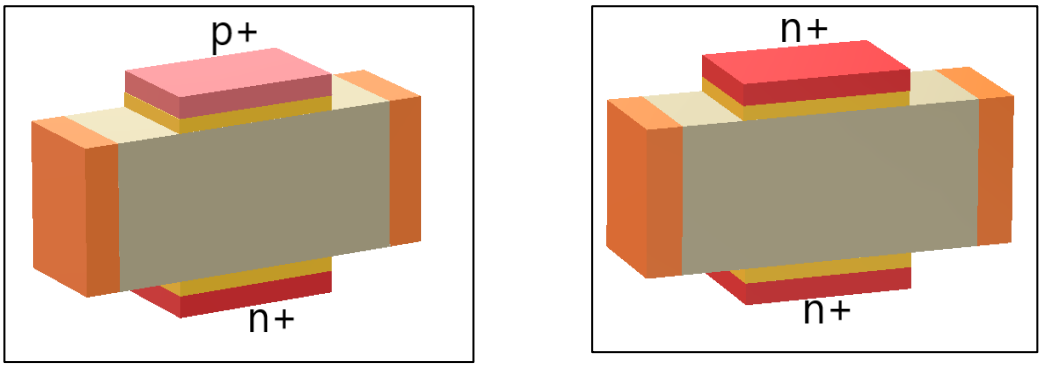

FIGURE 5.2. Representation of two double gate structures of DMDG

At first, the inversion layer is formed below the n^+ polysilicon gate of the p^+-n^+ double gate structure and the potential distribution changes linearly to fix the surface potential. After that, the inversion layer is generated below the p^+ polysilicon gate. So, this structure has two different threshold voltages concerning two different polysilicon materials. The threshold voltage of n^+-n^+ double gate SOI MOSFET (the value of threshold voltage generated due to front gate with n^+ polysilicon and back gate with n^+ polysilicon) (Reddy & Kumar, 2005) is,

$$V_{th}\left(n^+ - n^+\right) = V_{FB,fn} + 2\phi_F + \frac{Q_{si}}{2}\left\{1+\left(V_T\frac{4c_{si}}{Q_{si}}\right)\right\}\left\{\frac{1}{4c_{si}}+\frac{1}{c_{ox}}\right\} + V_T \ln\left(V_T\frac{4c_{si}}{Q_{si}}\right) \qquad (5.1)$$

where, thermal voltage, the Fermi potential expressed in Eqn. 3.5, $\phi_F = V_T \ln\left(\frac{N_a}{n_i}\right)$,

n_i - intrinsic carrier concentration. The flat band voltage of n^+ polysilicon can be expressed as,

$$V_{FB,fn} = V_T \ln\left(\frac{N_{n^+ poly}}{N_a}\right) \tag{5.2}$$

where $N_{n^+ poly}$ is the doping concentration of n^+ polysilicon. The flat band voltage also can be expressed as Eqn. 3.3 , $V_{FB,fn} = \phi_{MS2} = \phi_{M2} - \phi_{si}$

The space charge/unit area in the case of semiconductors is,

$$Q_{si} = qN_aT_{si} \qquad q \text{ - electronic charge,} \tag{5.3}$$

Considering the body effect, Eqn. 5.3 can be expressed as,

$$Q_{si} = \sqrt{\{2q\varepsilon_{si}N_a(2\phi_{si} + V_{SB})\}} \tag{5.4}$$

where, ϕ_{si} is the work function of silicon, describe in Eqn. 3.5, $\phi_{si} = X_{si} + \left(\frac{E_g}{2q}\right) + \phi_F$

and V_{SB} is the body bias.

Considering, $c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $c_{si} = \frac{\varepsilon_{si}}{T_{si}}$, For simplification, the gate oxide thickness is multiplied by a factor γ, where γ is the fraction of the permittivity constant of Si to the SiO_2.

$$\gamma = \frac{\varepsilon_{si}}{\varepsilon_{ox}} = 3 \quad \text{(Considered here).} \tag{5.5}$$

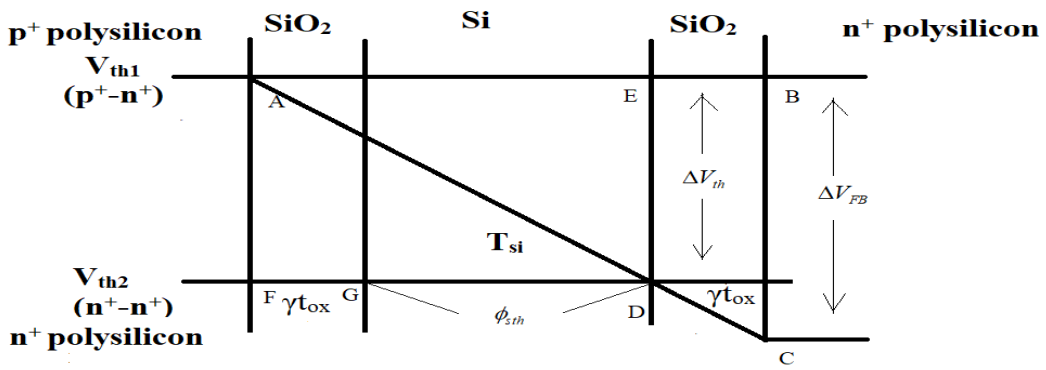

FIGURE 5.3. The schematic diagram for the potential distribution of DMDG

Following the method of Suzuki (Suzuki & Sugii, 1995; Suzuki et al., 1995) with little modification, the model of the threshold voltage for the DMDG structure, the potential distribution with respect to gate voltage at the several sections of the device is derived (Fig. 5.3). Based on the schematic representation, the analytical model of V_{th} for the device can be derived geometrically. The potential distribution representation (Fig. 5.3) is generated when the channel has been induced below the n^+ polysilicon. The potential distribution is constant for the entire channel region under the (n^+-n^+) double gate MOSFET, and the device is switched on when,

$$\phi_{sth} = V_{th_2} - V_{FB,fn} \tag{5.6}$$

The potential distribution under the (p^+-n^+) double gate MOSFET produces a gradient nature due to the difference in flat band voltage (Fig. 5.3). Also, the distribution shifted parallel with the applied gate voltage. The threshold voltage for p^+-n^+ DG SOI MOSFET can be calculated from the similar triangle ABC and AED of Fig. 5.3.

$$\begin{aligned} V_{th_1} &= V_{th}\left(n^+ - n^+\right) \times \left\{ \frac{\left(\gamma t_{ox} + T_{si}\right)}{\left(\gamma t_{ox} + \gamma t_{oxb} + T_{si}\right)} \right\} \times \Delta V_{FB} \\ &= V_{FB,fn} + 2\phi_F + \frac{Q_{si}}{2} \times \left\{ 1 + \left(V_T \times \frac{4c_{si}}{Q_{si}} \right) \right\} \times \left\{ \frac{1}{4c_{si}} + \frac{1}{c_{ox}} \right\} + V_T \times \ln\left(V_T \times \frac{4c_{si}}{Q_{si}} \right) - \left\{ \frac{\left(\gamma t_{ox} + T_{si}\right)}{\left(\gamma t_{ox} + \gamma t_{oxb} + T_{si}\right)} \right\} \times \Delta V_{FB} \end{aligned} \tag{5.7}$$

As the gate voltage increases the line AD changes its position and overlaps with FD. By this time the inversion layer is completely formed below the p^+ polysilicon gate and that is similar to,

$$V_{th_2} = V_{th}\left(n^+ - n^+\right) = V_{FB,fn} + 2\phi_F + \frac{Q_{si}}{2}\left\{ 1 + \left(V_T \frac{4c_{si}}{Q_{si}} \right) \right\}\left\{ \frac{1}{4c_{si}} + \frac{1}{c_{ox}} \right\} + V_T \ln\left(V_T \frac{4c_{si}}{Q_{si}} \right) \tag{5.8}$$

V_{th_1} mainly depends on t_{ox} and T_{si} because only these two parameters are connected with the gates. For $\left(t_{ox}/T_{si}\right) = 0.17$ the value of $V_{th_1} = 0.2$V. But $V_{th}\left(n^+ - n^+\right)$ and ΔV_{FB} are independent parameters and not related with t_{ox} and T_{si}. Both the channels take part in conduction when the gate voltage becomes higher than V_{th_2}. Now, $\left(\Delta V_{FB} = V_{FB,fp} - V_{FB,bn}\right)$ is the variation between flat band voltages and generates at front and back gates. Due to the SCE, the threshold voltage is shifted by ΔV_{th} amount for DMDG SOI MOSFET,

$$\Delta V_{th} = 2\sqrt{\eta_s \eta_{L_1}} e^{-\xi} \phi_{sth} \tag{5.9}$$

where,

$$\eta_s = V_{bi} - V_{Gs,f1} + \left\{ \Delta V_{FB} \left(2\left(1 + \frac{T_{si}}{2\gamma t_{ox}} \right) \right)^{-1} \right\} \tag{5.10}$$

$$\eta_{L_1} = \frac{1}{2} \left\{ \frac{\left(V_{bi} + V_{DS} - V_{Gs,f2} \right) Sinh\left(\frac{L_1}{\chi} \right) + \eta_s Sinh\left(\frac{L_2}{\chi} \right)}{Cosh\left(\frac{L_1}{\chi} \right) Sinh\left(\frac{L_2}{\chi} \right) + Sinh\left(\frac{L_1}{\chi} \right) Cosh(\frac{L_2}{\chi})} \right\} \tag{5.11}$$

$$\chi = T_{Si} \sqrt{\left(1 + \frac{2C_{si}}{C_{air}} \right) \left\{ 2\left(1 + \frac{C_{ox}}{C_{air}} + \frac{C_{ox}}{C_{si}} \right) \right\}^{-1}} \tag{5.12}$$

`

$$\xi = \frac{L_1}{\sqrt{2\left(\gamma T_{Si} t_{ox} \right)}} \tag{5.13}$$

Finally, the threshold voltage expression for DMDG SOI MOSFET is,

$$V_{th} = V_{thi} - \theta \Delta V_{th} \tag{5.14}$$

where i=1 or 2 , $\rho = k^{'} L_1 - 2.25$ and $k^{'} = 185 / \mu m$ and

$$\theta = 1 - \left\{ \frac{\left(L_1 - L_2 \right)}{\rho L_1} \right\} \tag{5.15}$$

But, when, $L_1 = L_2$ then $\theta = 1$.

The DIBL for the DMDG MOSFET structure can be defined as the difference in threshold voltages when the drain voltage is increased from the linear region to the saturation region (Lee et al., 2010).

$$\text{DIBL} = \text{V}_{\text{th}} \left(\text{V}_{\text{DS}} = 0.05\text{V} \right) - \text{V}_{\text{th}} \left(\text{V}_{\text{DS}} = 1\text{V} \right) \tag{5.16}$$

Subthreshold swing (S) is a specific quality of the device. It is the transformation of gate terminal voltage required for modification of one decade of subthreshold drain terminal current. In this case, the subthreshold swing of the device structure can be defined as (Tosaka et al., 1994),

$$\text{S} = \frac{\text{V}_{\text{t}} \ln 10}{\left\{ 1 - 2\exp\left(-\rho \right) \right\}} \tag{5.17}$$

$$\rho = \frac{L_1 + L_2}{2\sqrt{\left[\left(\frac{\gamma}{2}\right)\times\left\{1+\left(\frac{T_{si}}{4t_{ox}\gamma}\right)\right\}T_{si}t_{ox}\right]}} \tag{5.18}$$

In previous chapters, it has been discussed that with the change in temperature, the bandgap energy, carrier concentration and thermal voltage of the semiconductor change their values accordingly (Eqn. 3.59 to 3.62). The temperature effect also has been incorporated in the threshold voltage expression. A comparative study has been made in between SiO_2 and high-k material HfO_2 for all the characteristics. Using high-k material directly will generate some other difficulties which have already discussed earlier. To overcome it, the gate stack concept has been introduced in the design (Eqn. 1.4).

5.3. Analytical Model for Threshold Voltage of GCDMDG MOSFET

The 3D view of the asymmetric SOI GCDMDG structure is represented in Fig. 5.4. The doping concentration of the semiconductor substrate (N_a) is not constant here. It gradually changes from source to drain side. In graded channel structure the higher concentration region (N_{a1}) is present near the source side and the lower concentration region (N_{a2}) is present near the drain side. Similar to DMDG structure p^+ - n^+ polysilicon combinations have been used at the front gate and only n^+ polysilicon is used at the back gate. Due to the presence of two different work function materials, two different threshold voltages have been generated, those are V_{GC,th_1} and V_{GC,th_2} respectively. V_{GC,th_1} mainly depends on oxide width below the gate t_{ox} and (T_{si}) but V_{GC,th_2} is insensitive to these parameters. Normally V_{GC,th_1} is considered as the working threshold voltage for the device.

The minimum surface potential will be generated under the p^+ polysilicon as the work function is higher than n^+ polysilicon and also the higher work functioned polysilicon is at the top of the higher concentrate region. The threshold voltage mainly depends on the minimum surface potential. Oxide thicknesses are the same and the same voltages at both gate-source junctions have been applied. To estimate the

threshold voltage, the surface potential of GCDMDG structure has to be considered. Using the 2D Poisson's equation described in (Eqn. 4.1 and 4.2), vertical potential distribution (Eqn. 4.7a and 4.7b) and boundary conditions (Eqn. 3.7 - 3.18) the analytical model of the surface potential distribution is discussed in Chapter 4 (Eqn. 4.11- 4.51).

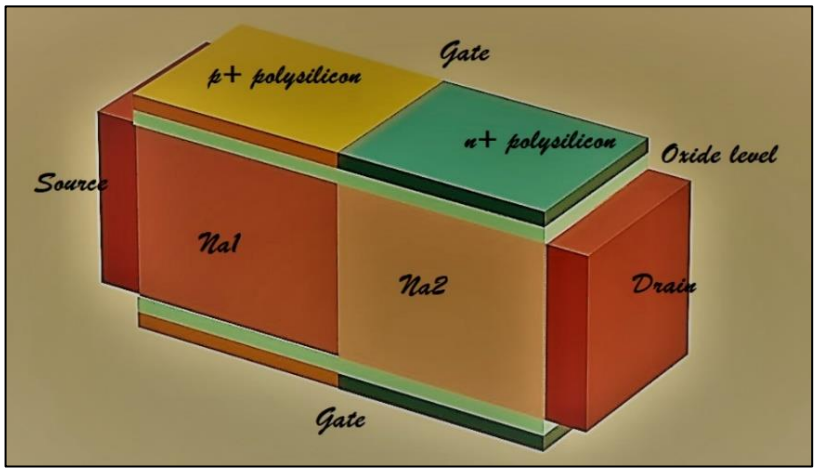

FIGURE 5.4. 3D representation of SOI GCDMDG

Minimum surface potential value being applied to compute the threshold voltage, because at this condition the minimum surface potential is equal to twice the bulk potential (Goel et al., 2016).

$$\phi_S\left(x_{\min}\right) = 2\phi_F \tag{5.19}$$

The minimum surface potential of the front channel can be calculated from $\phi_{S1}(x)$ and $\phi_{S2}(x)$, from Eqn. 4.38,

$$\phi_{S1}(x) = A_{gc}e^{\lambda x} + B_{gc}e^{-\lambda x} + \sigma_1$$

Considering the derivative of the surface potential for minimum value,

$$\Rightarrow \frac{d\phi_{S1}(x)}{dx}|_{x_{\min}} = A_{gc}\lambda e^{\lambda x} - B_{gc}\lambda e^{-\lambda x} = 0$$

$$\Rightarrow A_{gc}\lambda e^{\lambda x_{\min}} = B_{gc}\lambda e^{-\lambda x_{\min}}$$

$$\Rightarrow A_{gc}e^{\lambda x_{\min}} = B_{gc}e^{-\lambda x_{\min}}$$

$$\Rightarrow \frac{B_{gc}}{A_{gc}} = \frac{e^{\lambda x_{\min}}}{e^{-\lambda x_{\min}}} = e^{(\lambda+\lambda)x_{\min}}$$

$$\Rightarrow \frac{B_{gc}}{A_{gc}} = e^{(2\lambda)x_{\min}} \tag{5.20}$$

Considering the logarithmic value of both sides of Eqn. 5.20,

$$\Rightarrow \ln\frac{B_{gc}}{A_{gc}} = \ln\left(\exp 2\lambda x_{\min}\right)$$

$$\Rightarrow \ln\frac{B_{gc}}{A_{gc}} = 2\lambda x_{\min}$$

$$\Rightarrow x_{\min} = \frac{1}{2\lambda}\ln\frac{B_{gc}}{A_{gc}} \tag{5.21}$$

Putting the value of $x_{\min}$ from Eqn. 5.21 in Eqn. 4.38 of $\phi_{S1}(x)$,

$$\Rightarrow \phi_{S1}(x) = A_{gc}e^{\lambda\left(\frac{1}{2\lambda}\ln\frac{B_{gc}}{A_{gc}}\right)} + B_{gc}e^{-\lambda\left(\frac{1}{2\lambda}\ln\frac{B_{gc}}{A_{gc}}\right)} + \sigma_1$$

$$\Rightarrow \phi_{S1}(x) = A_{gc}e^{\left(\ln\sqrt{\frac{B_{gc}}{A_{gc}}}\right)} + B_{gc}e^{\left(\ln\sqrt{\frac{A_{gc}}{B_{gc}}}\right)} + \sigma_1$$

$$\Rightarrow \phi_{S1}(x) = A_{gc}\sqrt{\frac{B_{gc}}{A_{gc}}} + B\sqrt{\frac{A_{gc}}{B_{gc}}} + \sigma_1$$

$$\Rightarrow \phi_{S1}(x) = \sqrt{A_{gc}B_{gc}} + \sqrt{A_{gc}B_{gc}} + \sigma_1$$

$$\Rightarrow \phi_{S1}(x_{\min}) = 2\sqrt{A_{gc}B_{gc}} + \sigma_1 \tag{5.22}$$

Similarly, from Eqn. 4.39

$$\phi_{S2}(x) = C_{gc}e^{\lambda(x-L_1)} + D_{gc}e^{-\lambda(x-L_1)} + \sigma_2$$

Considering the derivative of the surface potential for minimum value,

$$\frac{d\phi_{S2}(x)}{dx}\Big|_{x_{\min}} = C_{gc}\lambda e^{\lambda(x-L_1)} - D_{gc}\lambda e^{-\lambda(x-L_1)} = 0$$

$$\Rightarrow C_{gc}\lambda e^{\lambda(x_{\min}-L_1)} = D_{gc}\lambda e^{-\lambda(x_{\min}-L_1)}$$

$$\Rightarrow C_{gc}e^{\lambda(x_{\min}-L_1)} = D_{gc}e^{-\lambda(x_{\min}-L_1)}$$

$$\Rightarrow \frac{D_{gc}}{C_{gc}} = \exp 2\lambda\left(x_{\min} - L_1\right) \tag{5.23}$$

Considering the logarithmic value of both sides of Eqn. 5.23,

$$\ln\frac{D_{gc}}{C_{gc}} = \ln\left(\exp 2\lambda\left(x_{\min} - L_1\right)\right)$$

$$\Rightarrow \ln\frac{D_{gc}}{C_{gc}} = 2\lambda\left(x_{\min} - L_1\right)$$

$$\Rightarrow \left(x_{\min} - L_1\right) = \frac{1}{2\lambda}\ln\frac{D_{gc}}{C_{gc}}$$

$$\Rightarrow x_{\min} = \frac{1}{2\lambda}\ln\frac{D_{gc}}{C_{gc}} + L_1 \tag{5.24}$$

Putting the value of $x_{\min}$ from Eqn. 5.24 in Eqn. 4.39 of $\phi_{S2}(x)$,

$$\phi_{S2}(x) = C_{gc}e^{\lambda\left(\frac{1}{2\lambda}\ln\frac{D_{gc}}{C_{gc}}+L_1-L_1\right)} + D_{gc}e^{-\lambda\left(\frac{1}{2\lambda}\ln\frac{D_{gc}}{C_{gc}}+L_1-L_1\right)} + \sigma_2$$

$$\Rightarrow \phi_{S2}(x) = C_{gc}e^{\left(\frac{1}{2}\ln\frac{D_{gc}}{C_{gc}}\right)} + D_{gc}e^{-\left(\frac{1}{2}\ln\frac{D_{gc}}{C_{gc}}\right)} + \sigma_2$$

$$\Rightarrow \phi_{S2}(x) = C_{gc}\sqrt{\frac{D_{gc}}{C_{gc}}} + D_{gc}\sqrt{\frac{C_{gc}}{D_{gc}}} + \sigma_2$$

$$\Rightarrow \phi_{S2}(x) = \sqrt{C_{gc}D_{gc}} + \sqrt{C_{gc}D_{gc}} + \sigma_2$$

$$\Rightarrow \phi_{S2}(x_{\min}) = 2\sqrt{C_{gc}D_{gc}} + \sigma_2 \tag{5.25}$$

Now, the minimum surface potential can be calculated as,

$$\phi_S\left(x_{\min}\right)=\min\left(\phi_{S1}\left(x_{\min}\right),\phi_{S2}\left(x_{\min}\right)\right) \tag{5.26}$$

Minimum surface potential is generated at the high work function polysilicon material. So, $\phi_{S1}\left(x_{\min}\right)$ has the lowest value. Now, at threshold voltage condition described in Eqn. 5.19

$$\phi_{S1}\left(x_{\min}\right)=2\phi_{F1}$$

Putting all the values from Eqn. 5.22 and Eqn. 4.6a,

$$\phi_{S1}\left(x_{\min}\right)=2\phi_{F1}=2V_T\ln\left(\frac{N_{a1}}{n_i}\right)$$

$$\Rightarrow 2\sqrt{A_{gc}B_{gc}}+\sigma_1=2\frac{KT}{q}\ln\left(\frac{N_{a1}}{n_i}\right)$$

$$\Rightarrow \sigma_{_1}=2\frac{KT}{q}\ln\left(\frac{N_{a1}}{n_i}\right)-2\sqrt{A_{gc}B_{gc}}$$

$$\Rightarrow -\frac{\beta_{gc1}}{\alpha}=2\phi_{F1}-2\sqrt{A_{gc}B_{gc}} \quad \text{[Putting the value of } \sigma_1 \text{ from Eqn. 4.38]}$$

$$\Rightarrow \frac{\beta_{gc1}}{\alpha}=2\left(\sqrt{A_{gc}B_{gc}}-\phi_{F1}\right)$$

Putting the values from Eqn. 4.28

$$\frac{\beta_{gc1}}{\alpha}=\frac{-2\left(\frac{c_{ox}}{T_{si}\varepsilon_{si}}\right)\left(V_{GS,f1}-\frac{qN_{a1}T_{si}}{2c_{ox}}\right)}{2\left(\frac{c_{ox}}{T_{si}\varepsilon_{si}}\right)}=2\left(\sqrt{A_{gc}B_{gc}}-\phi_{F1}\right)$$

After solving this, the gate voltage will be,

$$V_{GS}=2\phi_{F1}-2\sqrt{\left(A_{gc}B_{gc}\right)}+V_{FB,fp}+\frac{qN_{a1}T_{si}}{c_{ox}}$$

This gate voltage is equal to the threshold voltage. So,

$$V_{GC,th_1} = V_{GS} = 2\phi_{F1} - 2\sqrt{\left(A_{gc}B_{gc}\right)} + V_{FB,fp} + \frac{qN_{a1}T_{si}}{c_{ox}} \tag{5.27}$$

where, V_{GC,th_1} is the Threshold Voltage of the device. Like the DMDG, the temperature effect (Eqn. 3.59 and 3.62) on threshold voltage is also studied in the GCDMDG structure. All the characteristics have been considered for the comparative study with SiO_2, high-k material and gate stack concept (Eqn. 1.4).

5.4 Results and Discussions

Table 5.1. Design parameters to evaluate Threshold Voltage

Sl. No.	Parameters	Values
1.	N_a -Uniform body doping concentration	10^{15} cm^{-3}
2.	N_{a1} - Substrate doping concentration near the source	10^{16} cm^{-3}
3.	N_{a2} - Substrate doping concentration near the drain	10^{15} cm^{-3}
4.	N_d - Source/ Drain doping concentration	5×10^{19} cm^{-3}
5.	T_{si} - Thickness of film	12 nm
6.	L - Device channel length (for DMDG model)	40 nm
7.	L_1 - Gate length of M_1 p^+ Polysilicon (for DMDG model)	20 nm
8.	L_2 - Gate length of M_2 n^+ Polysilicon (for DMDG model)	20 nm
9.	L - Device channel length (for GCDMDG model)	100 nm
10.	L_1 - Gate length of M_1 p^+ Polysilicon (for GCDMDG model)	50 nm
11.	L_2 - Gate length of M_2 n^+ Polysilicon (for GCDMDG model)	50 nm
12.	n_i - Intrinsic carrier concentration	1.5×10^{10} cm^{-3}
13.	t_{ox} - Gate oxide thickness	2 nm
14.	t_{oxb} - Back gate oxide thickness	2 nm
15.	V_{DS} - Drain source voltage	0.5 V
16.	V_{GS} - Gate source voltage	0.5 V
17.	V_{SB} - Body bias	-1V

The characteristics generated from the analytical model of the threshold voltage of DMDG structure using SiO_2 and HfO_2 have been compared in this section. All the design parameters that have been considered to construct the threshold voltage have been listed in Table 5.1. For uniform doped and graded doped DMDG, the design

parameters mentioned in table 5.1 are essential for determining the threshold voltage. All of the information was gathered mostly from (Chiang, 2009; Goel, 2016; Suzuki, 1995; Suzuki, 1996; Chaudhry & Kumar, 2004) and other sources. The experimental value of threshold voltage data for uniformly doped DMDG structure can be compared to the generated value using these limitations (Bhattacherjee, 2017). The predicted analytical value of subthreshold swing is likewise equivalent to the experimental result of (Lolivier, 2004). All the analytical results are portraying outstanding agreement with TCAD results.

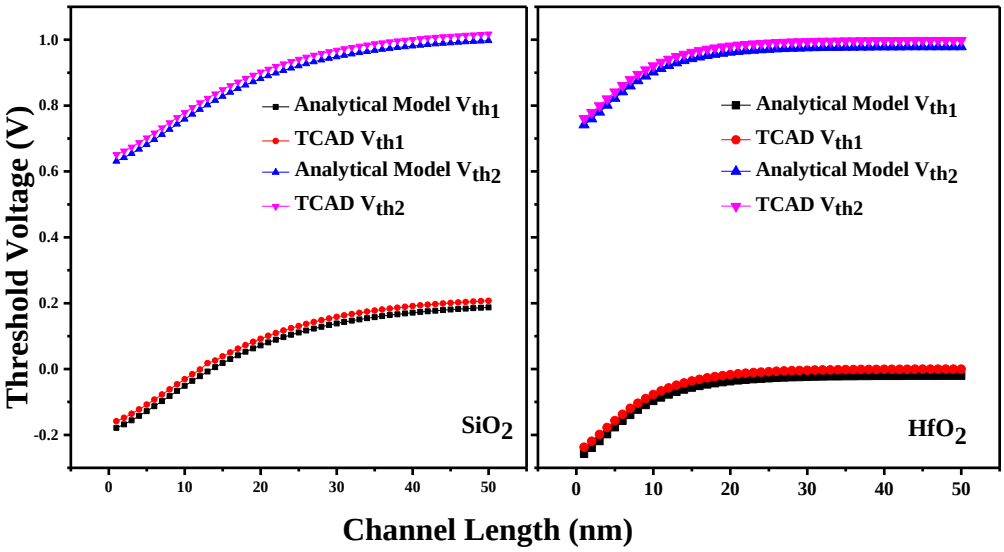

FIGURE 5.5 Threshold voltage with channel position

As per the analytical model prediction, the DMDG structure has two different threshold voltages. These were generated due to the presence of two different work functioned materials at the front gate as well as at the back gate terminals. The prediction is illustrated in Fig. 5.5, which shows a comparative study of the threshold voltage using SiO_2 and HfO_2 materials. It is observed that the threshold voltage is almost constant with respect to the channel length but at short channel length it decreases. This decreasing nature is called the threshold voltage roll off. Two threshold voltages are V_{th_1} and V_{th_2} where V_{th_1} is 0.2V and V_{th_2} is 1.0V approximately using SiO_2. But due to roll off, these values go down to -0.2V and 0.65V, respectively. Using high-

k material, the values of V_{th_1} and V_{th_2} are 0V and 1.0V approximately. At small scale channel length, these values go to -0.3V and 0.75V. For both the cases V_{th_1} vary with t_{ox}, T_{si}, etc, but V_{th_2} do not change their values at all. Rolling off nature triggers on the device at very low voltage in case of a small scale dimension. It is detected that the rolling off nature has been generated below 13 nm channel length using high-k material, whereas in the case of SiO_2 it has initiated approximately below 22 nm channel length. The rolling off nature is also negligible in high-k than using SiO_2. So, it can be predicted from the figure that in case of downscaling the device structure the rolling off problem of the threshold voltage may be overcomed using high-k material.

Figure 5.6 represents the comparative study of V_{th_1} with respect to the channel length using SiO_2, HfO_2, silicon on nothing (SON) and gate stack (GS) as the insulator medium simultaneously. Using SiO_2 the threshold voltage remains almost constant value 0.2V up to 20 nm channel length, after that it is rolling off to -0.2V (approx.). But using HfO_2 the threshold voltage is constant up to 10 nm channel length to the value -0.05V, after that it is rolling down. Similar features can be observed for the gate stack. SON means no dielectric material physically presents just above the semiconductor substrate. The absence of material is filled with air. So practically in the SON concept, air is acting as a dielectric medium. The threshold voltage is comparatively high for the SON structure and rolling off nature is also high. From 40-45 nm channel length it is declining. Thus, this concept is not feasible for downscaling the device structure. It is cleared that, though the threshold voltage is smaller than SiO_2, HfO_2 will be a better candidate for the rolling off nature at downscaling the device. Using high-k material as a dielectric medium the device can be triggered at very low voltage but it may protect the flow of unwanted leakage current that has been generated for the small scale dimension because its rolling off nature is also smaller than other competitors. But to avoid compatibility problem it is better to use gate stack structure as both of them has given similar nature. It can reduce SCEs as well as bear the same performance.

The threshold voltage increases with the decreasing value of film thickness for both SiO_2 and HfO_2 (Fig. 5.7.). It depicts that for a fixed channel length (L), with the

increment of film thickness, L/T_{si} ratio decreases. Consequently, threshold voltage reduces. But the nature of the characteristics is dissimilar for different dielectric materials. Using high-k material the threshold voltage remains almost constant up to 20 nm of film thickness, after that it increases and goes to 0.3V (approx.), but using SiO_2 the threshold voltage increases from 50 nm film thickness and goes to as high as 0.6V. So, it can be depicted that when the dimension is scaling down, using high-k the increased threshold voltage prevents the flow of unwanted leakage current and removes SCEs. On the other hand, the threshold voltage is not as high as the conventional one that delays the system.

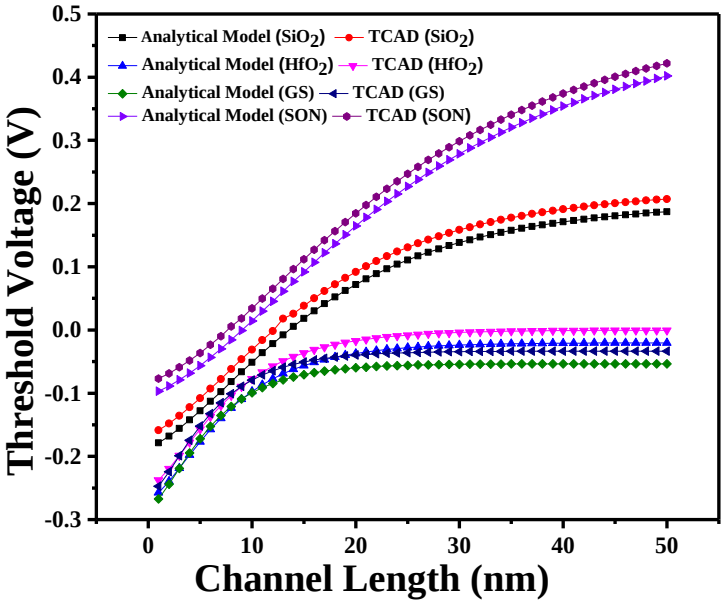

FIGURE 5.6. Threshold voltage with respect to channel length for different materials SiO_2, HfO_2, gate stack and SON

Earlier it has been discussed (Chapter 3) that with the variation of temperature the device parameters change their values. Bandgap energy, carrier concentration, thermal voltage and their corresponding relations have significant effects on temperature. Consequently, it also affects the threshold voltage (Fig. 5.8). Initially, threshold voltage decreases with the increasing value of temperature and after a certain temperature, it increases. It is perceived from the figure that at a very low temperature

(0K) the threshold voltage goes to 0.2V using SiO_2 material, it decreases to 0V at 150K temperature and after that, it increases upto 0.5V at a very high temperature (550K).

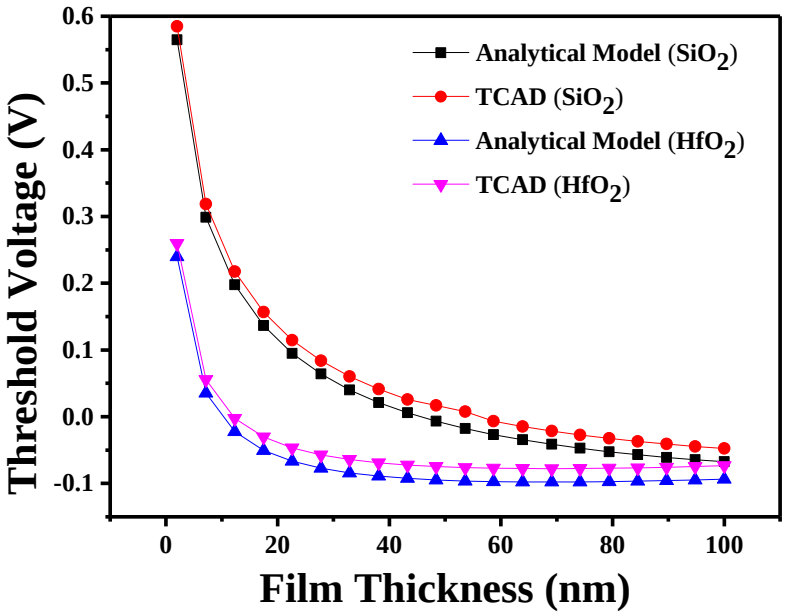

FIGURE. 5.7. Threshold voltage with film thickness

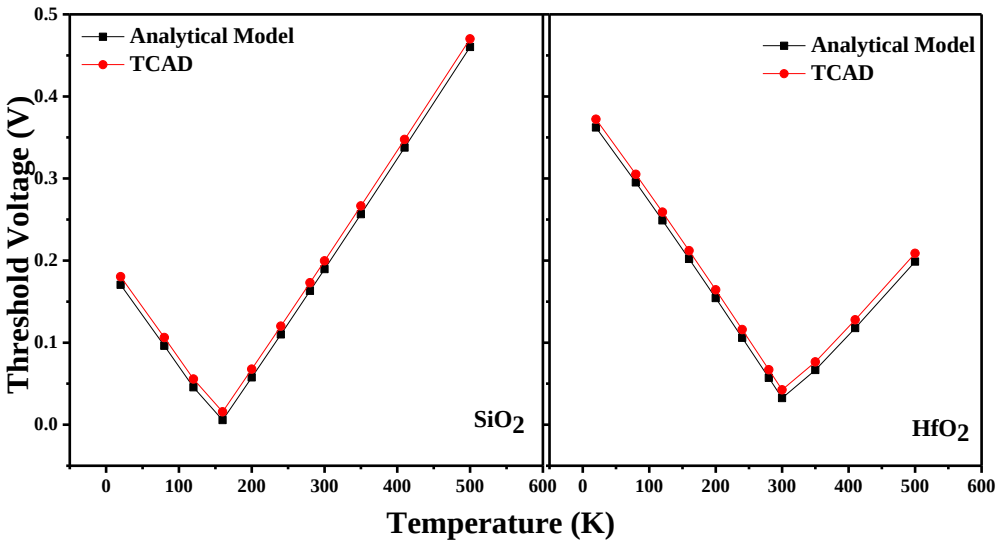

FIGURE. 5.8. Threshold voltage with temperature

On the other hand, in the case of HfO_2, the threshold voltage is at about 0.38V at 0K temperature. A minimum value of threshold voltage is generated at about 300K after that it increases and reaches up to 0.2V at 500K. In the case of high-k material, the minimum threshold voltage value is produced near to the room temperature. If the

temperature increases or decreases from this value the threshold voltage increases. It may help to protect the flow of unwanted current which is generated due to the low value of threshold voltage. For SiO_2 this phenomenon has occurred at a very low temperature (150K).

The thickness of the oxide level reduces with scaling down of device. Sometimes the oxide level won't be able to operate as the insulator medium with the reduced value. Threshold voltage also decreases with decreasing value of oxide thickness (Fig. 5.9). Thus, it can be said that at a small scale dimension the device can be activated at comparatively low gate voltage and it enhances the unwanted current as well as introduces SCEs. But from the figure, it can be stated that using high-k material the decreasing nature is quite low than using SiO_2. Using SiO_2, the threshold voltage reduces from 0.3V to -0.05V but using HfO_2 the threshold voltage remains almost same. So, it can be depicted that using high-k material the reduction of threshold voltage with the decreasing oxide thickness can be overcome and hence the unwanted current.

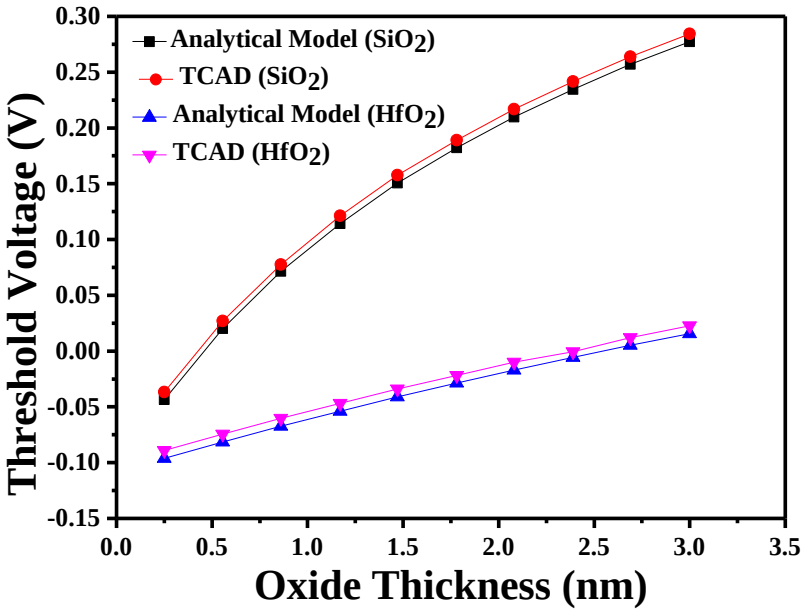

FIGURE. 5.9. Threshold voltage with oxide thickness

Figure 5.10 represents that threshold voltage variation with the substrate doping concentration. Like oxide thickness, the threshold voltage also decreases with the decreasing body doping concentration. It can be illustrated from the analytical model that, body or substrate doping concentration is an important parameter for threshold voltage modeling. The decreasing concentration value also affects the Fermi potential value as well as the flat band voltage of the semiconductor. Also the variation in substrate concentration changes the charge concentration that has accumulated below the oxide surface and formed the channel. These will reduce the threshold voltage and helps to increase unwanted small geometry effects. It can also be identified from the Fig. 5.10 that using high-k material, the decreasing nature is smaller than SiO_2. Using high-k material the oxide level may protect the device from the unwanted SCEs.

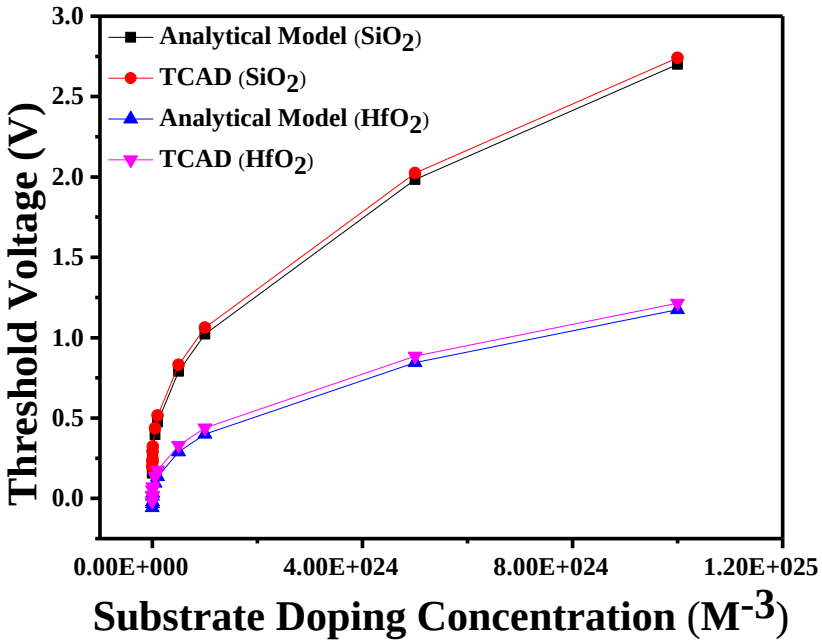

FIGURE. 5.10. Comparison of threshold voltage with substrate doping concentration

Threshold voltage also varies with the work function difference of the gate materials (Fig. 5.11). p^+ and n^+ polysilicon materials with different work functions have been used at the gate. This is the reason for step function in surface potential and electric field as well as the dual-threshold voltage of the device. So the work function is a vital parameter to determine the threshold voltage. The difference between the values of two work functions of the polysilicon is represented as work function

difference. For a fixed gate length ratio $L_1 : L_2$ = 1:1, the work function value of the 2nd polysilicon (n^+) material is kept at ϕ_{M2} = 4.17 eV and the work function value of the 1st polysilicon (p^+) is changed. The difference between them is called "changing work function" and represented as ΔW. The threshold voltage increases with the increment of ΔW (Kumar & Reddy, 2004). The increasing rate is higher in the case of SiO_2 material than HfO_2. With a very high value of ΔW, the threshold voltage is also very high using SiO_2 material, which again helps to decrease the on (I_{on}) and off (I_{off}) current (Reddy & Kumar, 2005). On other aspects, it is observed that with ΔW the threshold voltage using high-k material is almost negligible. This factor helps to overcome the SCEs.

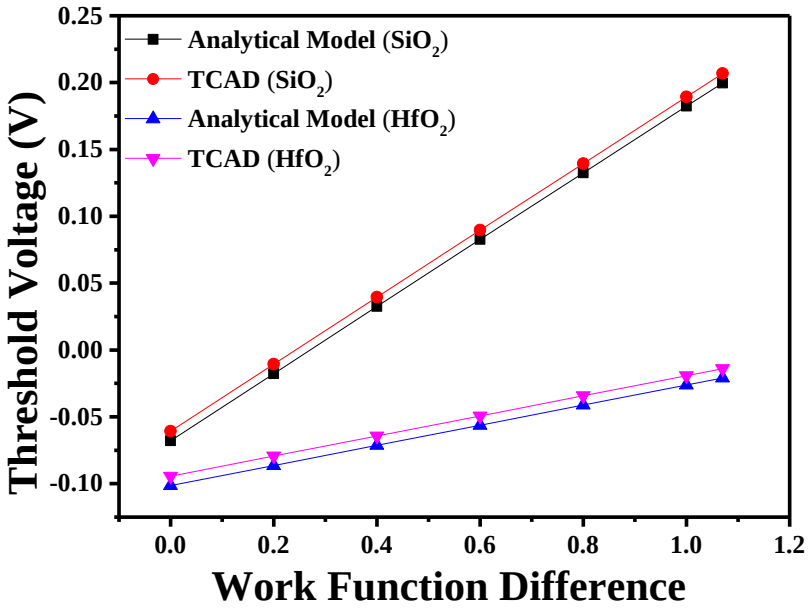

FIGURE 5.11. Relation of threshold voltage with ΔW

As the threshold voltage is a function of gate voltage, the drain voltage has no such significant effect on it. It can be explained from Fig. 5.12 that, threshold voltage slightly decreases with drain voltage. With the increasing value of drain voltage the p-n junction depletion region changes its formation and will affect the weak inversion mode. For that channel formation is delayed and as a result threshold voltage decreases its value. From Fig. 5.12, it can be depicted that using high-k material the decreasing value of the threshold voltage is so small that it has to be represented in exponential

order. So it can be said that using high-k, the drain voltage influence on threshold voltage can be removed.

DIBL for the structure is illustrated for both the oxide materials (Fig. 5.13) with gate length. Its value is 0.4 mV for 100 nm channel length and 7.3 mV for 60 nm channel length for SiO_2 oxide material but DIBL for HfO_2 is 1.5×10^{-7} V for 100 nm channel length and 0.06 mV for 60 nm. Therefore, it can be mentioned that DIBL intensifies with declining channel length but its value is smaller in the case of HfO_2 material than SiO_2 oxide material for the same channel length. That is the significant advantage of using high-k dielectric material. DIBL is decreasing means it will also reduce the SCEs. Also, it can be concluded that the enhancement of DIBL with the declining channel length increases the SCEs. Drain voltage reduces the barrier between the depletion region and that helps to enhance the free charged particle to flow through the channel, this will increase the unwanted current flow mechanism and decrease the threshold voltage. As a result the device temperature increases. From the above characteristics, it can be declared that using high-k as an oxide material in the device will be a better option to remove the SCEs in the small scale geometry.

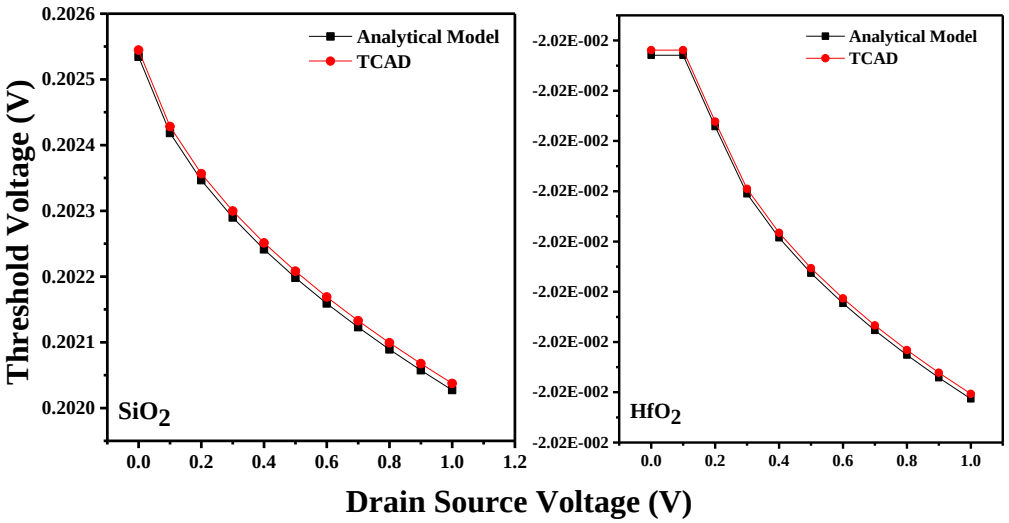

FIGURE 5.12. Threshold voltage with drain-source voltage

When the gate voltage is below the threshold voltage, the minority careers start accumulating just below the oxide semiconductor interface. This phenomenon is called weak inversion mode. The device is considered as “OFF” state because the threshold voltage has not been reached. At this stage, a small amount of current will flow through

the channel that has been generated by weak inversion mode. As the current flows before reaching the threshold voltage, the current is called 'subthreshold current'. This current is not desirable in a digital circuit, because at the OFF state this tends to enhance the flow of leakage current. This characteristic can be measured by the slope of the curve of the logarithmic value of the current vs gate voltage. With the help of the approximations (Eqn. 5.17), it can be estimated that the value of subthreshold swing for the DMDG structure is S = 59.8 mV/dec for 60 nm of channel length with HfO_2 (ideal value is 60 mV/dec at 300K) as shown in Fig. 5.14. Whereas at the same channel length S = 61.6 mV/dec for SiO_2. It is supposed that when the channel length is decreasing subthreshold swing is increasing owing to SCEs.

It can be depicted from the figure that using high-k material the subthreshold swing remains almost constant up to 25 nm channel length (in case of SiO_2 it is up to 35 nm only) and the increment of it with decreasing channel length is much lesser than SiO_2. Moreover, Fig. 5.15 also represents that with high-k material the swing maintains a constant value with the decreasing oxide thickness than SiO_2. Though when SiO_2 as the oxide material is considered, the subthreshold swing enhances significantly with increasing oxide thickness.

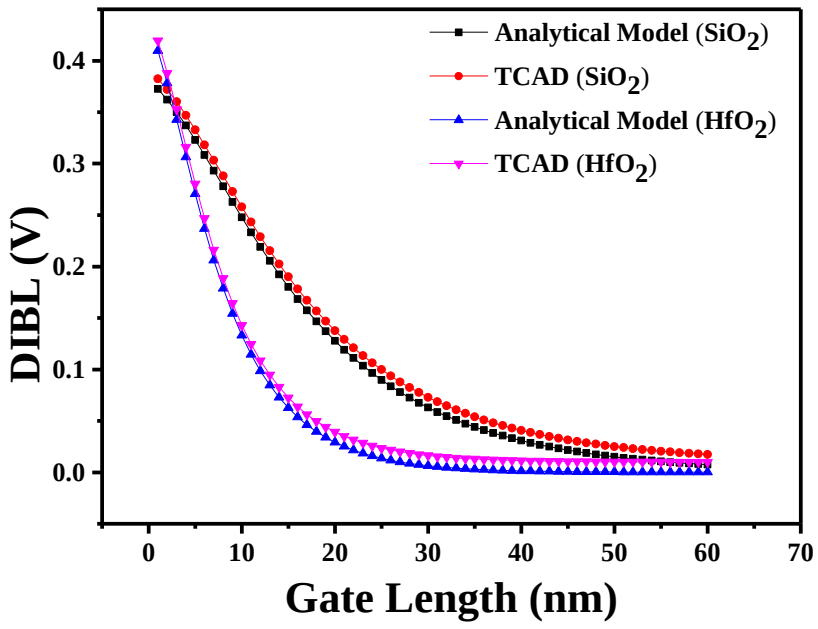

FIGURE 5.13. DIBL with channel length

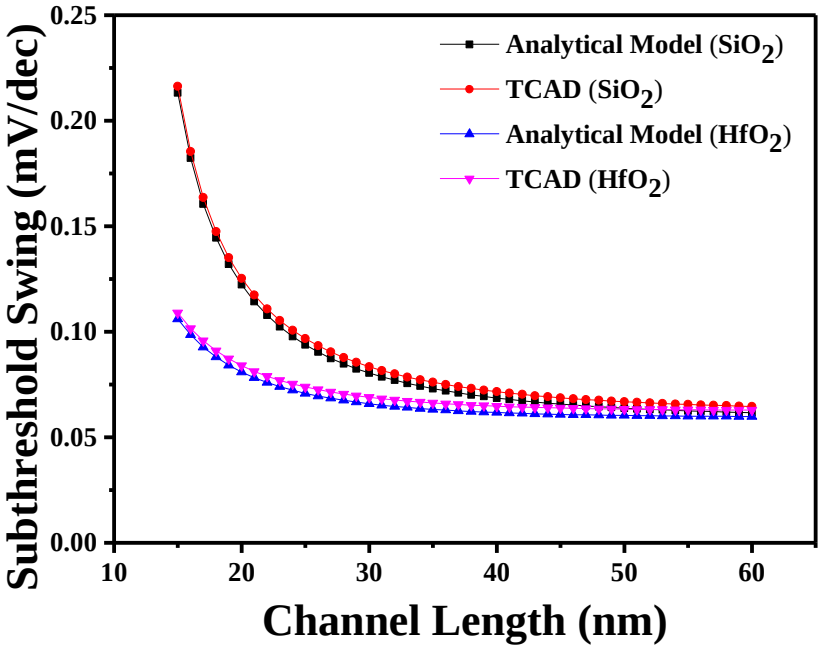

FIGURE 5.14. Subthreshold swing with channel length

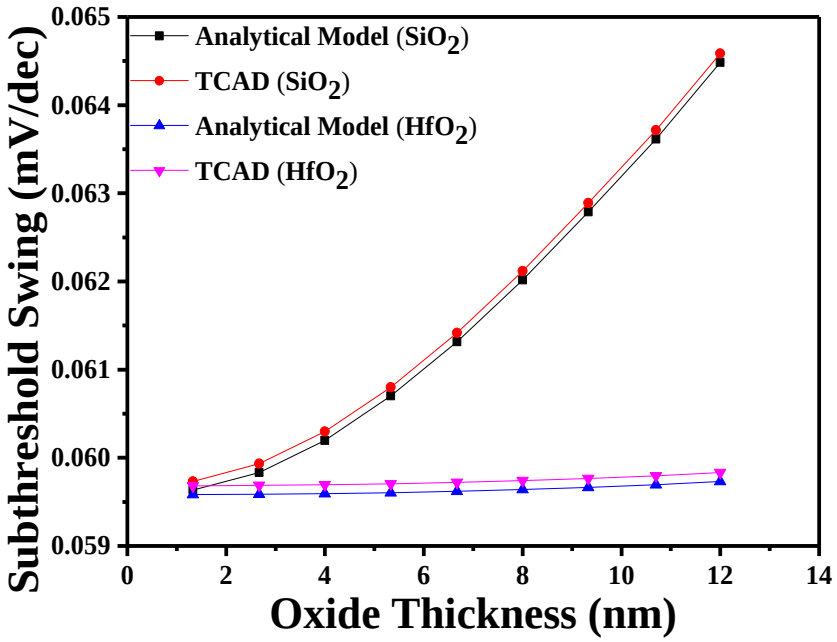

FIGURE 5.15. Subthreshold swing with oxide thickness

Increasing subthreshold swing decreases mobility. Figure 5.16 shows the variation of subthreshold swing with film thickness. Here it is increased with increasing value of film thickness for both cases. But the nature of the representation

using SiO_2 is stiffer than high-k. Therefore, it is observed that the switching characteristics of the DMDG structure are worsened significantly with lowering channel length, oxide thickness and film thickness.

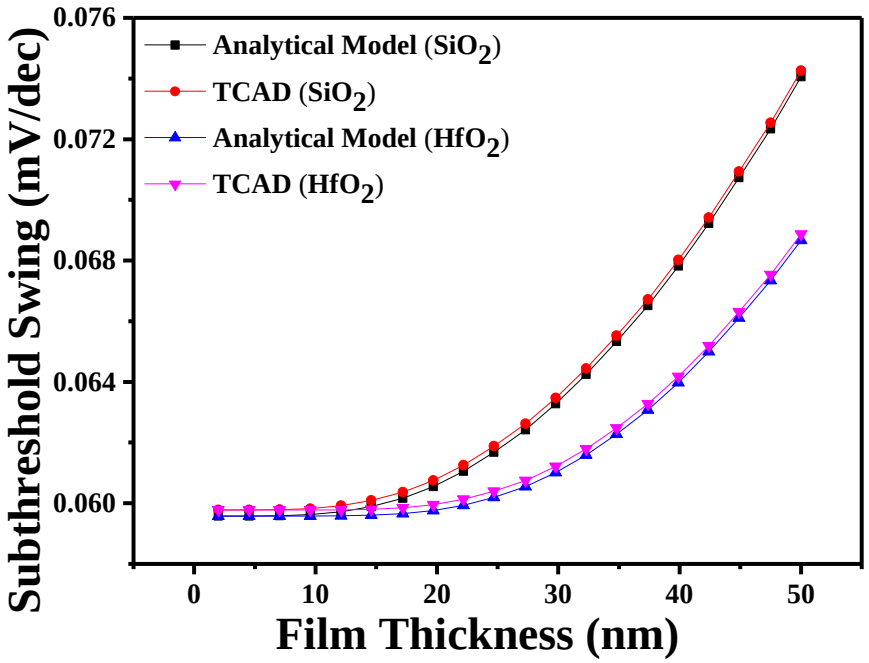

FIGURE 5.16. Subthreshold swing with film thickness

The characteristics generated from the analytical model of threshold voltage for GCDMDG structure using SiO_2 and HfO_2 are compared in next section. All the design parameters that have been considered to construct the threshold voltage have been listed in Table 5.1 All the analytical results are portraying outstanding agreement with TCAD results

The changes of threshold voltage with channel length for GCDMDG structure are represented in Fig. 5.17. It can be depicted from the figure that, irrespective of the oxide material used as the dielectric constant, the threshold voltage value for the GCDMDG structure is almost the same and it is at about 0.97V. It can be described that the threshold voltage varies so slightly that it can be said, it remains almost constant with the decrement of channel length. Whereas the decreasing nature is more flatted using high-k material, and stiffened in the case of SiO_2 material. It can be indicated that using the graded nature of doping concentration of the substrate, the roll

off factor of the threshold voltage with small scale dimension can be minimized and using high-k material better result is obtained.

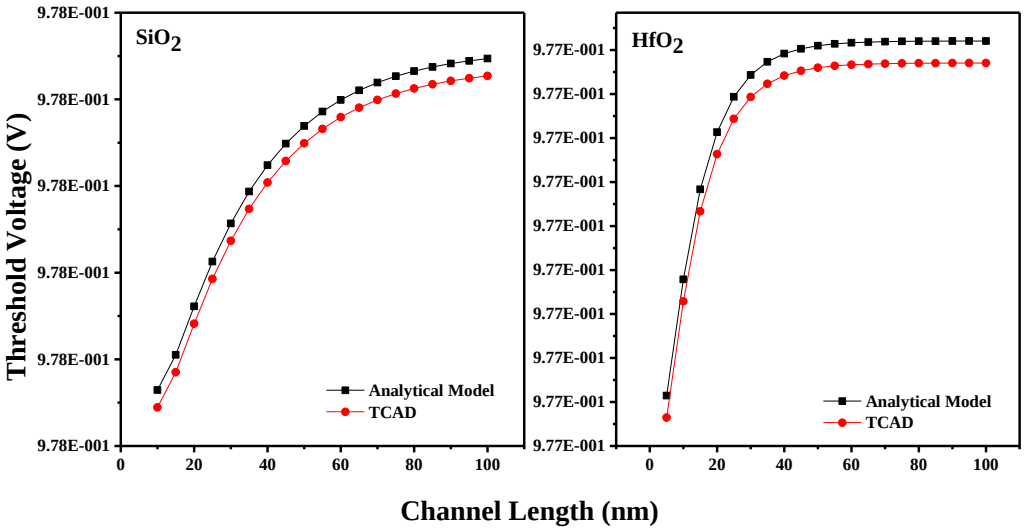

FIGURE 5.17. Threshold voltage with Channel length GCDMDG structure

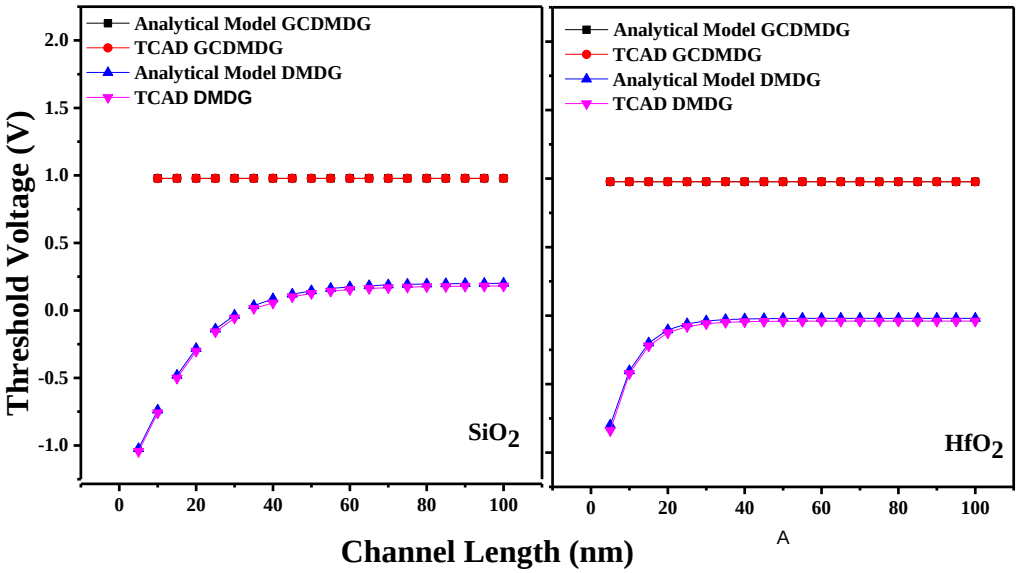

FIGURE 5.18. Threshold voltage for different device structure

Figure 5.18 illustrated the comparative study of threshold voltage for two different structures DMDG and GCDMDG. The figure has clearly shown that the threshold voltage of the GCDMDG structure is much higher than the DMDG structure

and it is almost constant. The threshold voltage of the DMDG structure present the rolling off nature. It is also verified that the surface potential value of GCDMDG structure is higher than DMDG structure (Fig. 4.3). As the threshold voltage depends on the minimum value of the surface potential so it is higher in the case of GCDMDG structure. It can also be seen that by using high-k material the threshold voltage value is almost same with SiO_2 in GCDMDG, but in DMDG structure these two values are found different.

In GCDMDG structure, the substrate doping concentration has been changed gradually which has a great influence on the threshold voltage. The threshold voltage increases with the increasing value of doping concentration (Fig. 5.19). Here the doping concentration near the source side has been changed, keeping the concentration constant near to the drain side. This is due to higher concentration and presence of higher work function gate material the threshold voltage primarily is generated at this region. The change of threshold voltage with change in substrate doping concentration near source region has been considered here. It can be illustrated that using SiO_2 material the increment is very stiff whereas using high-k material and gate stack the threshold voltage increases slightly with the substrate doping concentration.

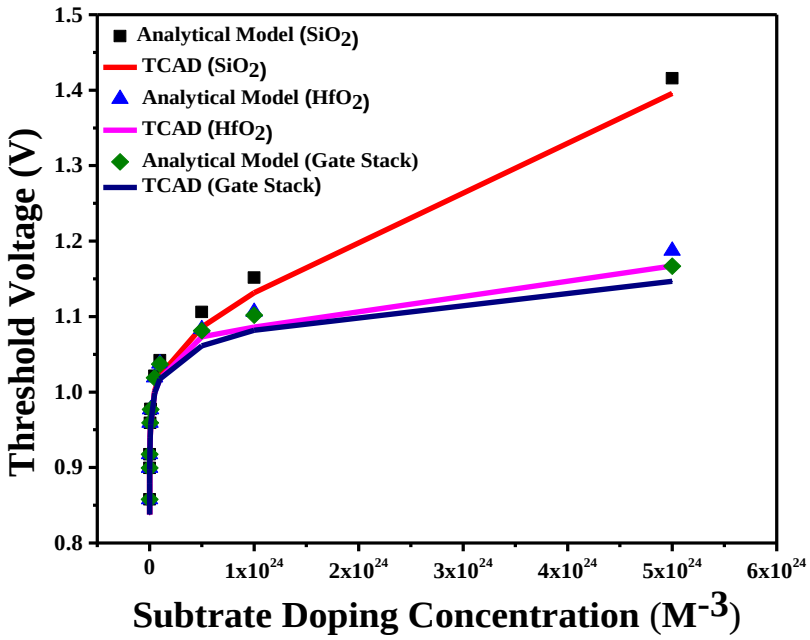

FIGURE 5.19. Threshold voltage for different doping concentration of GCDMDG

Figure 5.20 represents the variation of threshold voltage with drain voltage using SiO_2 and high-k as an oxide interface. The changes in threshold voltage for drain voltage are almost negligible and in maximum case it is constant. The surface potential solely depends on the gate-source voltage and the threshold voltage depends on surface potential. The slight decrement of threshold voltage in the case of SiO_2 is for DIBL effect. The DIBL effect increases with the increment of drain voltage which helps to reduce threshold voltage and generate a large amount of current. This problem easily can be overcome by using high-k material.

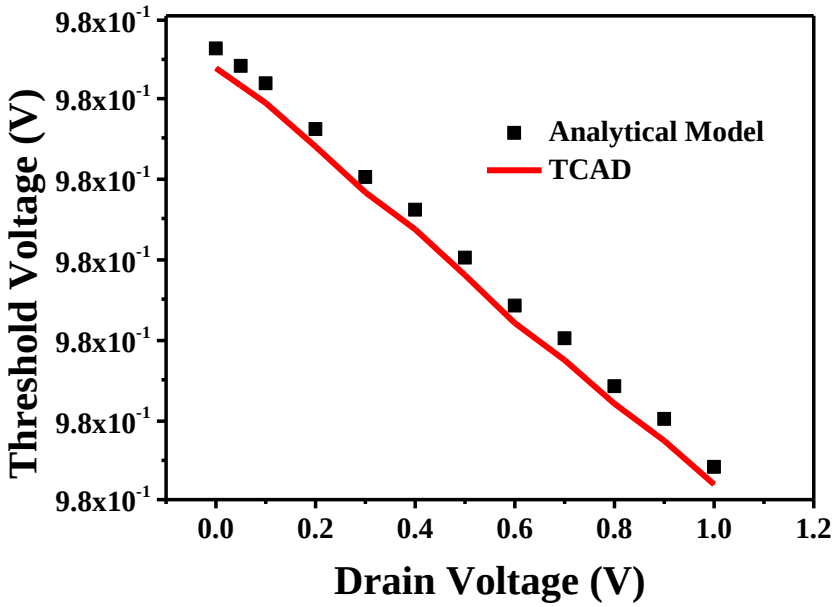

FIGURE 5.20. Threshold voltage for different drain voltage of GCDMDG

The small scale geometry of the device decreases the channel length, width as well as film thickness of the device. The scaling down of film thickness affects the threshold voltage of GCDMDG structure (Fig. 5.21). The ratio L/T_{si} decreases with the increase of T_{si} for a fixed channel length. With the increase in film thickness threshold voltage increases. Alternatively, it can be said that with the small-scale dimension of film thickness, the threshold voltage decreases. But decrement nature is different for different oxide materials. In the case of high-k material and gate stack design, the threshold voltage is almost constant with a small scale dimension of film thickness. This feature will help to remove SCEs and flow of unwanted current that

has been generated in lowering down the threshold voltage using SiO_2 oxide material with the small dimension of the device structure.

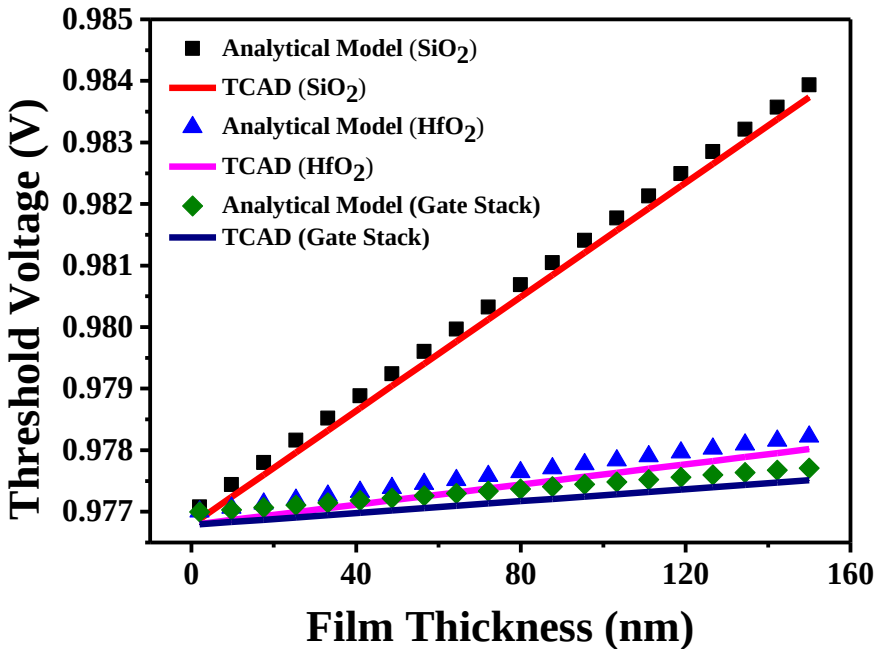

FIGURE 5.21. Threshold voltage for different film thickness of GCDMDG

As mentioned in Eqn. 3.59-3.62, with the variation of temperature the substrate, source and drain doping concentrations, the energy bandgap of the semiconductor and the thermal voltage changes. These effects will produce an influence on the threshold voltage. With the increasing temperature, the threshold voltage of the GCDMDG structure increases as illustrated in Fig. 5.22. Though the threshold voltage decreases with decreasing temperature but it is of higher value compared to DMDG structure. So, it can be stated that at a very low temperature the GCDMDG structure does not allow to flow the unwanted current. And also it is to be mentioned that the increment nature of the threshold voltage is the same for three different cases as depicted in the representation (Fig. 5.22). Table 5.2 represents the variation of V_{th} with temperature.

The working threshold voltage of the structure lies under the high work function gate material with a higher substrate doping concentration region. So the work function also has a great impact on the characteristics. Threshold voltage increases with the increasing value of work function difference depicted in Fig. 5.23. Keeping the gate length ratio at $L_1 : L_2$ = 1:1, the work function value of the 2nd polysilicon (n^+) material

is kept at ϕ_{M2} = 4.17 eV and the work function value of the 1st gate material (p^+) is changed. The difference between them is represented as ΔW . All the structures have projected the same performance with changing work functions. Table 5.3 denoted the changes of threshold voltage with ΔW in a tabular formation for different gate oxide material engineering. That tabular representation also depicted as bar diagram in Fig. 5.23 for clear visualization.

Table 5.2: Variation of V_{th} with temperature

Temperature (K)	SiO_2		HfO_2		Gate Stack	
	V_{th} (Proposed Model)	V_{th} (TCAD)	V_{th} (Proposed Model)	V_{th} (TCAD)	V_{th} (Proposed Model)	V_{th} (TCAD)
20	0.65329	0.65324	0.65328	0.65323	0.65328	0.65323
80	0.72472	0.72467	0.72466	0.72461	0.72465	0.72460
120	0.77344	0.77339	0.77332	0.77326	0.77331	0.77325
160	0.82288	0.82283	0.8227	0.82265	0.82269	0.82263
200	0.87294	0.87289	0.87269	0.87264	0.87267	0.87262
240	0.92354	0.92349	0.92321	0.92316	0.92318	0.92313
280	0.9746	0.97454	0.97418	0.97412	0.97415	0.97410
300	1.00028	1.00023	0.99982	0.99977	0.99978	0.99973
350	1.0649	1.06484	1.06432	1.06427	1.06427	1.06421
410	1.14311	1.14306	1.14238	1.14233	1.14231	1.14225
500	1.26155	1.26150	1.26057	1.26052	1.26048	1.26043

Table 5.3: Variation of V_{th} with work function difference

Work Function Difference	SiO_2		HfO_2		Gate Stack	
	V_{th} (Proposed Model)	V_{th} (TCAD)	V_{th} (Proposed Model)	V_{th} (TCAD)	V_{th} (Proposed Model)	V_{th} (TCAD)
0.2	0.09754	0.09752	0.09708	0.09706	0.09704	0.09702
0.4	0.29754	0.29752	0.29708	0.29706	0.29704	0.29702
0.6	0.49754	0.49752	0.49708	0.49706	0.49704	0.49702
0.8	0.69754	0.69752	0.69708	0.69706	0.69704	0.69702
1	0.89754	0.89752	0.89708	0.89706	0.89704	0.89702
1.07	0.96754	0.96753	0.96708	0.96706	0.96704	0.96702

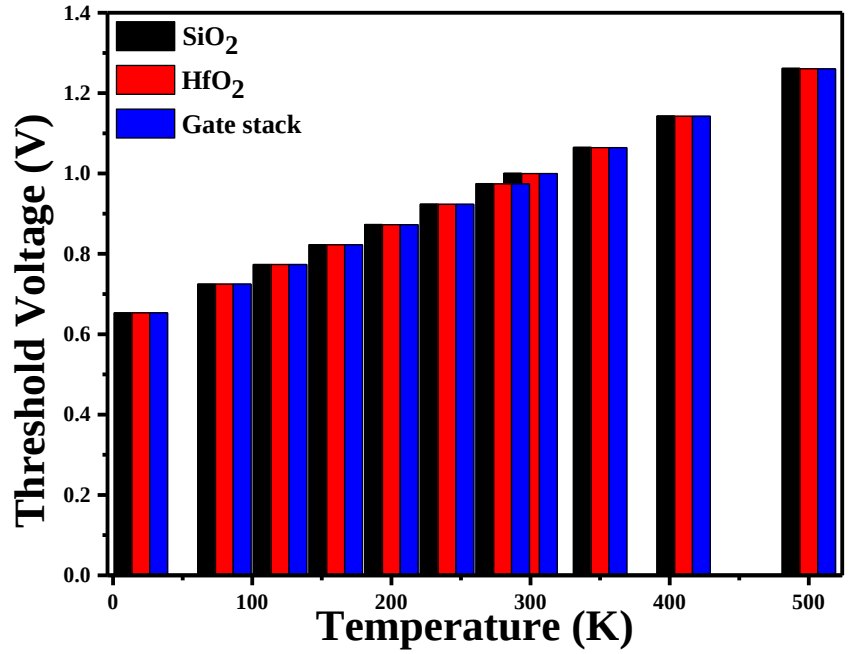

FIGURE 5.22. Threshold voltage with temperature of GCDMDG

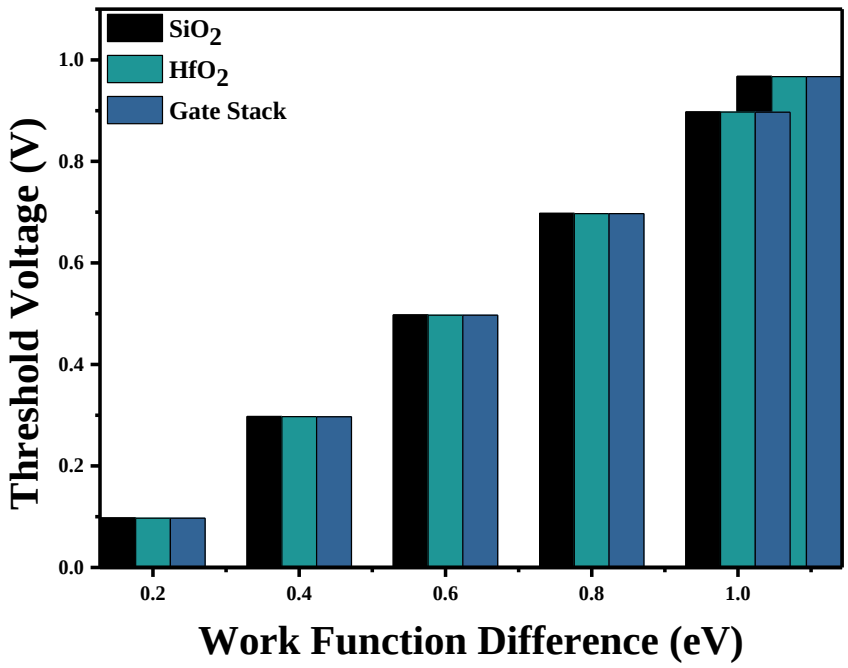

FIGURE 5.23. Threshold voltage with work function difference of GCDMDG

With small-scale dimensions, several device parameters such as channel length and oxide thickness will degrade down. Changing the dimension of oxide thickness also has a great influence on the threshold voltage. It would help to generate a SCE.

As a result, the threshold voltage decreases and a huge amount of current will flow through the channel. But from the representation of Fig. 5.24, it is clear that in the GCDMDG the changes of threshold voltage increases with oxide thickness, however using high-k the changes are almost negligible. So using a GCDMDG structure with high-k oxide material the SCEs almost can be eliminated.

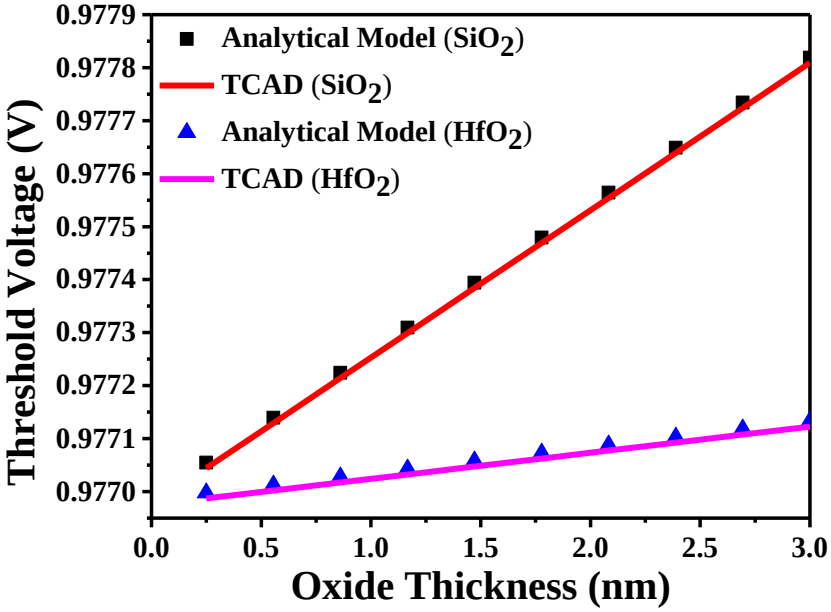

FIGURE 5.24. Threshold voltage with oxide thickness of GCDMDG

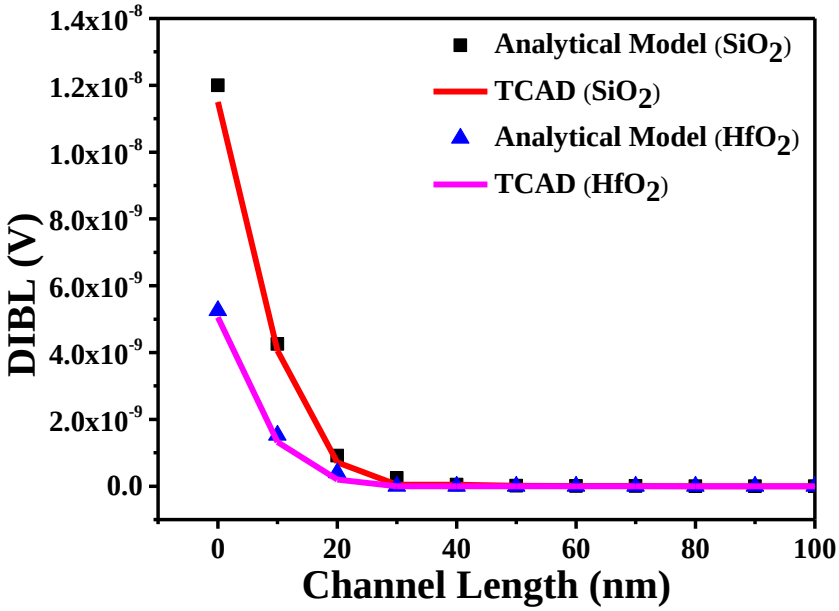

FIGURE 5.25. DIBL with channel length of GCDMDG

DIBL is defined as the difference in threshold voltage when the drain voltage is increased from linear region to saturation region (Eqn. 5.16). Overall DIBL effect is deceased with the increasing channel length for the device using both the materials. For both cases, the DIBL effect maintains a constant value up to the 20nm channel length (Fig. 5.25), below this it increases. But increment of DIBL using high-k material is smaller than the conventional one. So using of GCDMDG structure with high-k oxide material, the drain voltage induction on the SCE can be reduced.

5.5. Summary

Being an important characteristic, the threshold voltage is main feature to demonstrate. In the DMDG device structure, its value is comparatively low but at a small scale channel dimension, it shows a rolling off nature. This will enhance the short channel current. Using high-k material this problem can be overcome to some extent. On the other hand, using the GCDMDG structure, the threshold voltage is higher than DMDG but it does not show the rolling off nature with small scale device dimension. The threshold voltage in this case is an almost constant value. Using high-k material the result will be more accurate. So the GCDMDG structure with high-k oxide material as a dielectric constant will be a better combination to overcome the SCEs. Several other constraints like oxide thickness, temperature, substrate doping, film thickness, etc. have a great influence on the threshold voltage. At the time of device fabrication, these parameters have to be considered.

In view of DIBL, both the device exhibits a very good result. That means this type of SCE can be overcome with these devices. Also, the subthreshold swing has reached up to the ideal value in the case of the DMDG structure. For all the cases using high-k oxide material has given a better result than SiO_2.

CHAPTER

6

Drain Current

6.1. Introduction

The device current conduction capability can be expressed as drain current. When comparing different devices, it can be used as a guide. All the device performances like transconductance, voltage gain, switching capability, etc. can be depicted with the help of drain current. However, the device structure should not allow the overrated drain current to flow through it. The maximum drain current is governed by the device's current capabilities, as well as the device's maximum channel temperature, safe operation, and other relevant characteristics. The channel is fully inverted at threshold voltage, and the drain current begins to flow due to free charge particle movement. It is a function of both the gate-source and drain-source voltages. Initially, it increases with the increasing value of drain-source voltage-formed linear region. Here, the performance of all MOSFETs has been taken into account. The device functions as a good amplifier due to its high impedance. The current becomes saturated after certain drain voltage and does not rise with added drain voltage. This is referred to as the saturation region (Cerdeira et al., 2008; Chiang, 2016; Francis et al., 1994). However, as the gate voltage is increased, the drain current increases, and the saturation voltage changes as a result.

The channel current is just equal to the drain current before saturation occurs. Nonlocal effects such as channel length modulation, velocity overshoot, and DIBL (Eqn. 5.16) become increasingly effective as the device dimension shrinks and have a significant impact on the drain current model. The most important consequence in the drain current model is velocity overshoot, which is directly connected to the transconductance due to SCEs (Chen & Kuo, 1996; Jin et al., 2010). The step function

generated in the electric field causes the electron velocity to overshoot its saturation value for a period shorter than the energy relaxation time. Over the past few years, the scaling factor has become a challenge to the conventional MOSFET technology. However, to achieve high speed, packing density and for better performance, the device dimension has to shrink according to scaling law (Dennard et al., 1974; Nicollian et al., 1982). With the scale down, the charge sharing between source and drain increases that helps to reduce the gate controllability over the channel depletion region. So the reduction of device dimension specifically declining channel length increases several SCEs like DIBL, hot carrier effects, threshold voltage roll off, channel length modulation, etc. (Maity et al., 2015; Neamen, 1992). Reduction of channel width also increases the electric field at the field isolation edge which helps to decrease the current drivability and hot carrier induced degradation (Maity et al., 2017).

DG structure and DMG structures provide very good immunity to SCEs, however, at some level they fail to perform. DMG structure is not suitable to perform in a deep submicron regime. However parasitic capacitance effects and interface charge effects are major problems here. In DMDG structure (combining DG and DMG), the difference in work function at gate material creates an electric field at the interface of two gates. It helps to improve the carrier transport efficiency, carrier transport speed and device driving capability (A. Cerdeira et al., 2008; Chaudhry & Kumar, 2004b; Kumar & Chaudhry, 2004; Kumar & Reddy, 2004; Lin & Taur, 2017; Saxena et al., 2004). This structure also helps to reduce the electric field at the drain end which increases the controllability over the channel conduction and reduces the hot carrier effects. The n^+ type polysilicon gate material near the drain side absorbs the additional variation of drain potential generated after the saturation level, therefore reduces the DIBL and CLM effects (Chiang, 2012; Tsormpatzoglou et al., 2007). As a result, it protects the device from adverse effects such as mobility degradation and random microscopic fluctuation of dopant atoms. This structure also helps to increase the capability and the controllability of the drain current. Consequently, the transconductance improves and drain conductance drops down.

In GCDMDG structure, there are two threshold voltages for two different gate materials (Chen et al., 2003; Darwin & Samuel, 2020; Goel et al., 2016; Maity et al.,

2018; Suzuki & Sugii, 1995; Tsormpatzoglou et al., 2008). Due to the doping concentration of the channel their values are different. It was mentioned in the previous chapter that, in the case of GCDMDG structure, the threshold voltage is higher than uniformly doped DMDG. Though it helps to reduce the unwanted current flow side by side it also reduces the performance of the device than normal DMDG. In this chapter, a comparative study has been made between two structures over different constraints i.e. oxide thickness, drain current, gate voltage and the temperature effect (Shahidi et al., 1988; Widiez et al., 2005), etc.

Due to small dimensions and SCEs, several parameters like impact ionization, velocity overshoot, channel length modulation and DIBL affect the drain current (Assaderaghi et al., 1993; Chen et al., 1995; Chou et al., 1985; Sai-Halasz et al., 1988). To generate the accurate analytical model of drain current for DMDG structure, all these parameters have been considered for the device model (Shahidi et al., 1988). According to a recent study it has been proved that with using high-k dielectric material (Maity et al., 2020; Salmani-Jelodar et al., 2016) (like HfO_2) instead of SiO_2 the gate tunneling current, the leakage power reduces drastically and delivers astounding performance and greater energy efficiency (Arora et al., 1994; Chaudhry & Kumar, 2004a; N. Maity et al., 2019; Maity et al., 2016; Narang et al., 2013; Roldan et al., 1997; Roldan et al., 1998). Therefore the proposed device is also verified by using high-k material.

6.2. Analytical Model for Drain Current of DMDG MOSFET

DMDG structure has generated step function in surface potential as well as in the electric field. The lateral portion of the electric field is higher than its previous one and it will affect more in the saturation region than the linear region. As a consequence, the impact ionization and parasitic BJT effects generate a strong influence on the current conduction of the device. Depending on the biasing, the channel region moved from accumulation to the moderate inversion and then the strong inversion region. At the strong inversion, the channel gets inverted and the current I_{ch} will flow due to the drift of the minority carrier. The high speed drifting electrons collide with the lattice and generate electron-hole pairs at the high electric field region at the drain side. Due to the high electric field, the electrons move towards the drain and holes move toward

the source direction resulting in the impact ionization current I_h. Also, a fraction of the impact ionization current KI_h is directed towards the source and as a result, the holes get accumulated in the thin film. The hot carriers are moved around the channel and they easily penetrate the thin oxide level. The generated high energy electron-hole pairs moves from n channel to gate (made of p^+ polysilicon) and also into the p type substrate (p-n-p formation). This phenomenon helps to activate the parasitic bipolar transistor effect (Chiang, 2012). Consequently the current flow for the movement of these free particles can be calculated as the transistor current equation. The current is also effected the original drain current flowing through the channel. Some amount of the holes recombine with electrons in the base region (channel) and drainage down. A part of the collector current $K'I_C$ (composed of electrons) flows due to a vertical electric field through the parasitic bipolar transistor. These electrons also collide with lattice and consequently generate a huge amount of electron-hole pairs.

Combining all the above-stated factors, the total drain current I_D is composed of the channel current I_{ch}, the impact ionization current I_h and the collector current I_C of the parasitic bipolar device (Chiang, 2012),

$$I_D = I_{ch} + I_h + I_C \tag{6.1}$$

The collector current itself can be expressed in terms of the emitter current I_E ,

$$I_C = \alpha_0 I_E + I_{CBO} \tag{6.2}$$

I_{CBO} is the leakage current between the collector and the base with emitter-base junction opened. It is a function of the gate voltage,

$$I_{CBO} = \frac{WT_{si}I_{so}}{1+\theta_1\left(V_{GS}-V_{th_1}\right)} \tag{6.3}$$

where W is the channel width of the device and I_{so} is the leakage current per unit cross section in the collector-base junction. θ_1 is a constant term. The expression of the drain current in the saturation region can be expressed as (Shahidi et al., 1988),

$$I_{D,sat} = GI_{ch} + HI_{CBO} \tag{6.4}$$

$$G = 1 + \frac{M\left\{1-\left(1-K_k\right)\alpha_0\right\}}{1-\left(1+K_k K^{'} M\right)\alpha_0} \tag{6.5a}$$

$$H = \frac{1+K^{'}M}{1-\left(1+K_k K^{'} M\right)\alpha_0} \tag{6.5b}$$

$$M = \left\{\alpha\left(V_{DS}-V_{DS,sat1}\right)\exp\left(\frac{-\beta}{\left(V_{DS}-V_{DS,sat1}\right)}\right)\right\}+1 \tag{6.5c}$$

Considering impact ionization and parasitic BJT effect, CLM (Kumar et al., 2004), Velocity overshoot (Chen et al., 1995) and DIBL effect (Maity et al., 2019), the channel current in the linear region (Chiang, 2012; N. P. Maity et al., 2019) can be expressed as,

$$I_{ch} = \sum_{i=1,2}\left[\left\{\frac{W\mu_{neff}c_{ox}}{L\left(1-\frac{l_d}{L}+\frac{V_{DS}}{LE_c}\right)}\times\left\{\left(V_{GS}-V_{thi}^{'}\right)V_{DS}-\frac{1}{2}V_{DS}^2\right\}\right\}+\left\{\frac{\lambda_a W}{\left(L-l_d\right)^2}\right\}\times\left\{\left(V_{GS}-V_{thi}^{'}\right)V_{DS}-\frac{1}{2}V_{DS}^2\right\}\right] \tag{6.6}$$

In the saturation region, the channel current can be expressed as,

$$I_{D,sat} = G\sum_{i=1,2}\left[\left\{\frac{W\mu_{neff}c_{ox}}{L\left(1-\frac{l_d}{L}+\frac{V_{DS,sati}}{LE_c}\right)}\times\left\{\left(V_{GS}-V_{thi}^{'}\right)V_{DS,sati}-\frac{1}{2}V_{DS,sati}^2\right\}\right\}+\left\{\frac{\lambda_a W}{\left(L-l_d\right)^2}\right\}\times\left\{\left(V_{GS}-V_{thi}^{'}\right)V_{DS,sati}-\frac{1}{2}V_{DS,sati}^2\right\}\right]+HI_{CBO} \tag{6.7}$$

where,

$$V_{thi}^{'} = V_{th_i}-\left(DV_{DS}\right) \qquad \text{for } i=1 \text{ and } 2 \tag{6.8}$$

V_{th_i} is the threshold voltage generated for the front and back gate. $V_{DS,sati}$ is the saturation voltage for the front and back gate ($i=1$ and 2). Which gives

$$V_{DS,sati} = \frac{\left(V_{GS}-V_{th_i}\right)}{\left(1+\frac{\left(V_{GS}-V_{th_i}\right)}{LE_c}\right)} \tag{6.9}$$

$$E_c = \frac{2v_{ns}}{\mu_{neff}} n \tag{6.10}$$

The electron velocity (v_{ns}) saturates at the critical field. μ_{neff} is the effective mobility of the inversion layer electrons and n is a constant term (values are given at Table 6.1). Effective mobility is a combination of mobility associated with phonon scattering (μ_{ph}) and mobility associated with surface roughness scattering μ_{sr} (Maity et al., 2019)

When the applied drain-source voltage V_{DS} is greater than saturation voltage $V_{DS,sat1}$, the channel length modulation has to be considered, then the velocity saturation or 'pinch off point' moves towards the source. As a consequence, the effective channel length decreases. The voltage difference $\left(V_{DS} - V_{DS,sat1}\right)$ is dropped across the distance l_d as a result of CLM (Kumar et al., 2004),

$$l_d = l \ln\left(1 + \frac{\left(V_{DS} - V_{DS,sat1}\right)}{V_{pp}}\right) \tag{6.11}$$

Where, $V_{pp} = 2lE_c$ is the fitting parameter,

$$l = X_j \sqrt{\left(\frac{t_{ox}\varepsilon_{si}}{n\varepsilon_{ox}}\right)} \quad \text{and} \quad X_j = \sqrt{\left(\frac{2\varepsilon_{si}\left(\phi_s - V_{gs}\right)}{qN_a}\right)} \tag{6.12}$$

Like other electrical parameters, the drain current of the DMDG structure also very much depends on the temperature. The temperature effect is described in Eqn. 3.32 and 3.33 have been introduced in the drain current model and study the variances. A comparative study has been made between SiO_2 and high-k material HfO_2 for all the characteristics.

6.3. Analytical Model for Drain Current of GCDMDG MOSFET

In the GCDMDG structure instead of using a uniform doping channel, a graded doping channel has been used as discussed earlier. Near the source side, the substrate is highly doped and denoted as N_{a_1} whereas near the drain side the substrate is

comparatively low doped and denoted as N_{a_2}. So the CLM for different doping concentrations can be expressed as,

$$l_{d_1} = l_1 \ln\left(1+\frac{\left(V_{DS}-V_{DS,sat1}\right)}{V_{pp_1}}\right) \text{ and } \; l_{d_2} = l_2 \ln\left(1+\frac{\left(V_{DS}-V_{DS,sat1}\right)}{V_{pp_2}}\right) \tag{6.13}$$

the fitting parameters are $V_{pp_1} = 2l_1E_c$ and $V_{pp_2} = 2l_2E_c$,

$$l_1 = X_{j_1}\sqrt{\left(\frac{t_{ox}\varepsilon_{si}}{n\varepsilon_{ox}}\right)} \text{ and } \; l_2 = X_{j_2}\sqrt{\left(\frac{t_{ox}\varepsilon_{si}}{n\varepsilon_{ox}}\right)}$$

$$X_{j_1} = \sqrt{\left(\frac{2\varepsilon_{si}\left(\phi_s - V_{GS}\right)}{qN_{a_1}}\right)} \text{ and } \; X_{j_2} = \sqrt{\left(\frac{2\varepsilon_{si}\left(\phi_s - V_{GS}\right)}{qN_{a_2}}\right)} \tag{6.14}$$

The two threshold voltages for the GCDMDG structure have already been explained in an earlier chapter (Eqn. 5.27),

$$V_{GC,th_1} = V_{GS} = 2\phi_{F1} - 2\sqrt{\left(A_{gc}B_{gc}\right)} + V_{FB,\,fp} + \frac{qN_{a1}T_{si}}{c_{ox}}$$

Similarly, another one is

$$V_{GC,th_2} = V_{GS} = 2\phi_{F_2} - 2\sqrt{\left(C_{gc}D_{gc}\right)} + V_{FB,\,fn} + \frac{qNa_2T_{si}}{c_{ox}} \tag{6.15}$$

Putting all these expressions and considering the impact ionization, parasitic BJT effect, CLM, velocity overshoot and DIBL effects in the linear current and saturation current expression described in Eqn. 6.6 and 6.7. The linear and saturation current expression for the GCDMDG structure will be

$$I_{ch} = \sum_{i=1,2}\left[\left\{\frac{W\mu_{neff}c_{ox}}{L\left(1-\frac{l_{d_i}}{L}+\frac{V_{DS}}{LE_c}\right)}\times\left\{\left(V_{GS}-V'_{thi}\right)V_{DS}-\frac{1}{2}V_{DS}^2\right\}\right\}+\left\{\frac{\lambda_a W}{\left(L-l_{d_i}\right)^2}\right\}\times\left\{\left(V_{GS}-V'_{thi}\right)V_{DS}-\frac{1}{2}V_{DS}^2\right\}\right] \tag{6.16}$$

$$I_{D,sat}=G\sum_{i=1,2}\left[\left\{\frac{W\mu_{neff}c_{ox}}{L\left(1-\frac{l_d}{L}+\frac{V_{DS,sati}}{LE_c}\right)}\times\left\{\left(V_{GS}-V'_{thi}\right)V_{DS,sati}-\frac{1}{2}V^2_{DS,sati}\right\}\right\}+\left\{\frac{\lambda_a W}{\left(L-l_d\right)^2}\times\left\{\left(V_{GS}-V'_{thi}\right)V_{DS,sati}-\frac{1}{2}V^2_{DS,sati}\right\}\right\}+HI_{CBO}\right] \quad (6.17)$$

6.4. Results and Discussions

All the design parameters that have been considered to construct the drain current model have been listed in Table 6.1. The drain current for the DMDG structure was computed using data from (Roldan et al., 1998; Arora et al., 1994; Assaderaghi et al., 1993; Chen et al., 1995), among others. The characteristics generated from the analytical model of the drain current of uniformed doping DMDG structure using SiO_2 and HfO_2 have been elaborated in the first section. In the second part, the characteristics of graded doping DMDG structure have been explained with mentioned oxide materials. All the analytical results are portraying outstanding agreement with TCAD simulation results.

Drain current with respect to drain to source voltage has been signified in Fig. 6.1. In this representation V_{GS} is considered as a constant term. Here the effective gate voltage (i.e gate voltage – threshold voltage) has been considered as gate-source voltage. The two distinct regions of the V-I characteristics curve can be visible, one is linear region, the second one is saturation region. At the initial stage when the drain current increases sharply with increasing value of drain voltage that region is called linear region or non-saturation region. In this section, first weak inversion mode followed by moderate inversion and after that the strong inversion mode has been generated and the gate voltage reaches up to the threshold voltage. Therefore with a small increment of drain voltage the free carrier moves rapidly through the channel hence the current flows. At weak inversion mode, the current flows only for the diffusion process of the carrier, at moderate inversion the current flows for both diffusion and drift process. However at strong inversion mode, the current flows totally for the drift process and the drain voltage is a prime factor for the current flow. After reaching a certain gate voltage called “Pinch of voltage” the inversion channel

thickness reduces to zero. In this situation, the current flow has been restricted and reaches a constant value. This section is called the saturation region.

Table 6.1. Design parameters to evaluate Drain Current

Sl. No.	Parameters	Values
1.	N_a - Uniform body doping concentration	10^{15} cm^{-3}
2.	N_{a1} - substrate doping concentration near the source	10^{16} cm^{-3}
3.	N_{a2} - substrate doping concentration near the drain	10^{15} cm^{-3}
4.	N_d - Source/ Drain doping concentration	5×10^{19} cm^{-3}
5.	T_{si} - Thickness of film	12 nm
6.	L - Device channel length	100 nm
7.	L_1 - Gate length of M_1 p^+ Polysilicon	50 nm
8.	L_2 - Gate length of M_2 n^+ Polysilicon	50 nm
9.	n_i - Intrinsic carrier concentration	1.5×10^{10} cm^{-3}
10.	t_{ox} - Gate oxide thickness	2 nm
11.	t_{oxb} - Back gate oxide thickness	2 nm
12.	V_{DS} - Drain source voltage	0.75 V
13.	V_{GS} - Gate source voltage	1 V
14.	V_{SB} - Body bias	-1V
15.	μ_{neff} - Effective mobility	0.039
16.	v_{ns} - electron velocity	8×10^4
17.	n - Constant term	0.8
18.	K_k - Constant term	0.85
19.	K' - Constant term	0.85
20.	α_0 - Constant term	0.994
21.	α - Constant term	0.15
22.	β - Constant term	15.7
23.	λ_a - Constant term	25×10^{-11}
24.	θ_1 - Constant term	6
25.	I_{so} - leakage current	80×10^{-6} A

In this section, the current flow does not increase with the increasing value of the drain voltage. However, with the increasing drain-source bias, the gate to source

voltage also changes its value. As a result, channel thickness reduction changes its position and the channel modulation process is considered. Consequently, the current flow has been stopped. If the drain voltage increases further, then the breakdown has generated and a huge amount of current starts to flow through the channel. This mode is called the cut-off region, represented as a slight hike portion above the saturation region. Using high-k material as a dielectric oxide, the drain current is higher than using SiO_2. In the previous chapter, it has been mentioned that comparatively low threshold voltage can be achieved using high-k. Therefore the device can be triggered at a low voltage hence the drain current is higher. As a result, transconductance increases and drain conductance decreases which helps to overcome the SCEs.

Another interesting feature that has to be mentioned from the characteristics is that with the increasing gate-source voltage the drain current increases for both cases. With the increment of gate voltage more quantity of free particles are accumulated in the channel region and with the help of drain voltage, they start to flow and conduct current. Strong evidence of the prediction has been depicted in Fig. 6.2. With the increment of gate-source voltage drain current increases, however, the saturation voltage also has been changed for both the material. This graph is considered for a fixed drain voltage of 0.75V. This characteristic is represented as transconductance. Using high-k material the transconductance is higher than using SiO_2 – this quality makes the device a better one. The channel length is defined by the transconductance that has been produced by electron velocity overshoot.

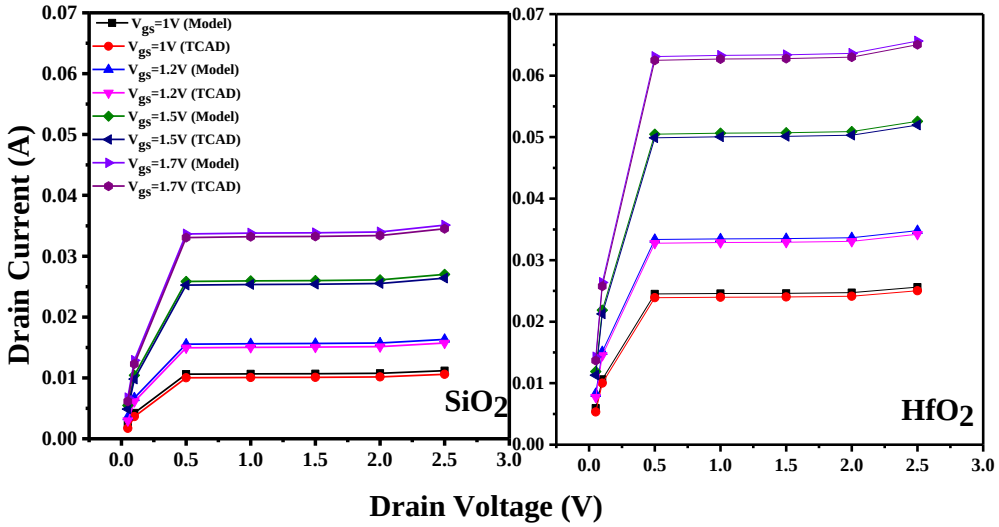

FIGURE 6.1. Drain current with drain voltage

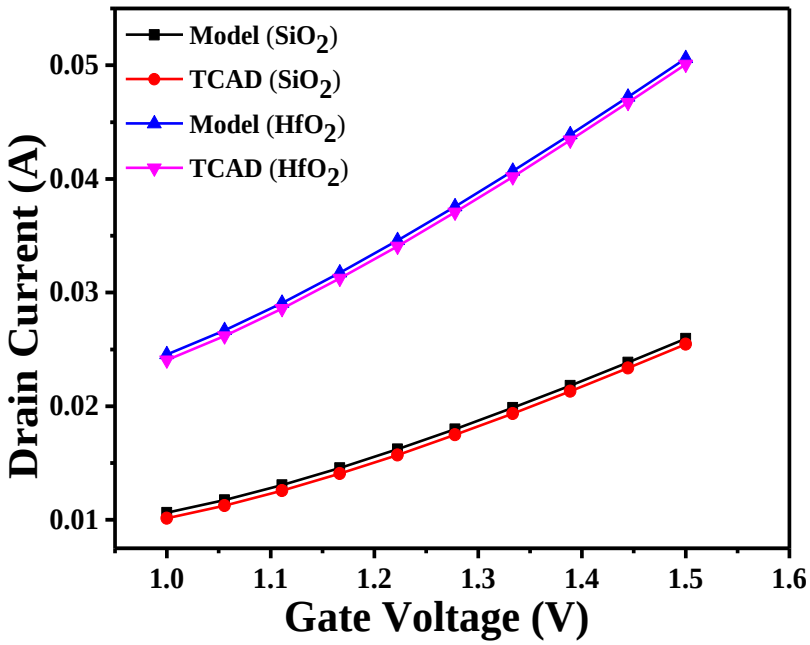

FIGURE 6.2. Drain current with gate voltage

The variation of drain current with film thickness has been defined in Fig. 6.3 for V_{GS} = 1V and V_{DS} = 0.75V. The overall drain current decreases with the decreasing value of film thickness or more perfectly, with the small scale dimension of the device. Earlier it has been described (Fig. 5.7) that with the decreasing value of film thickness threshold voltage increases. However, using a high-k substance the increment nature is lower than SiO_2. This is also reflected in Fig. 6.3. Threshold voltage increasing means drain current decreases. So the unwanted drain current, generated due to SCEs will not flow for the decreasing film thickness. This will be advantageous in the case of small scale devices. Yet the decreasing nature of drain current using high-k material device is higher. Even the drain current is almost constant up to 10 nm film thickness. Conversely, using SiO_2, the decreasing nature is quite stiff.

The deviation of drain current with respect to oxide thickness has represented in Fig. 6.4. As the oxide thickness decreases the drain current increases for both cases, but the increment of drain current in the case of high-k material is higher. As the increment of drain current leads to the decrement of threshold voltage (Fig. 5.9), it may tend to flow unwanted current when the device will be scaling down. However

comparing the characteristics, using a high-k substance, the problem may be overcome.

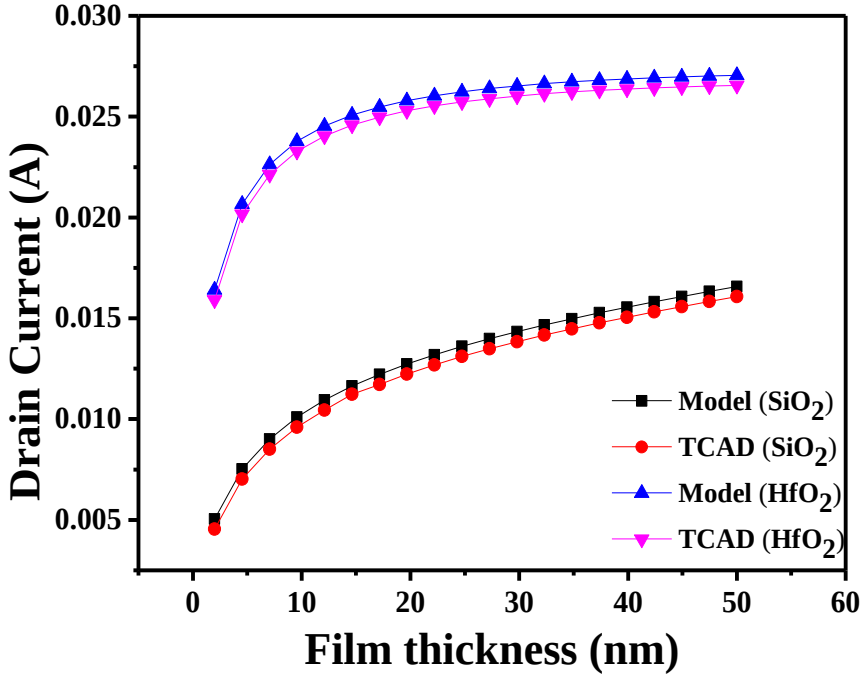

FIGURE 6.3. Drain current with film thickness

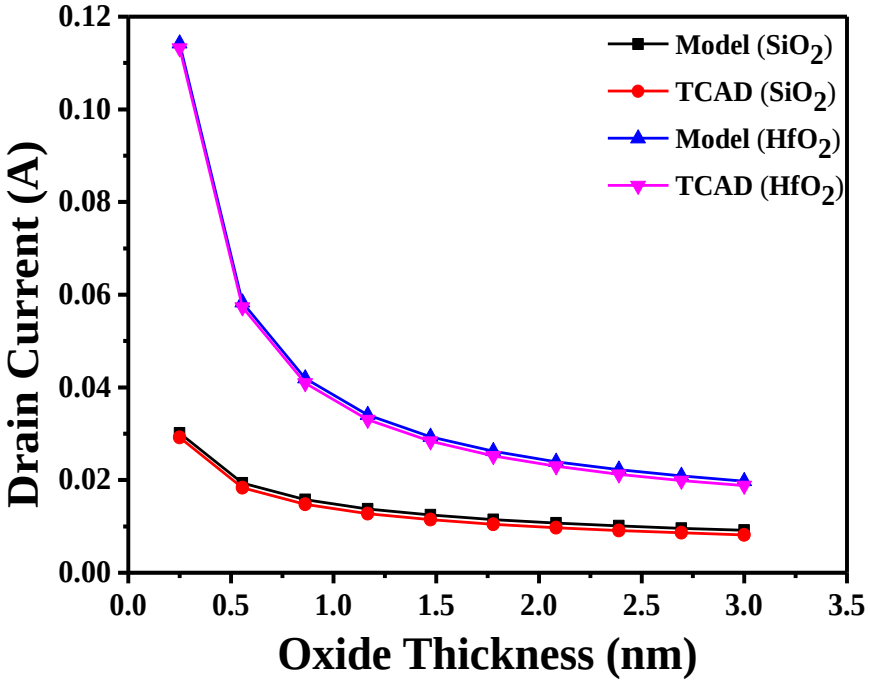

FIGURE 6.4. Drain current with oxide thickness

Drain current also has a temperature effect (Fig. 6.5). Due to changes in temperature the bandgap energy as well as the concentrations of the semiconductor changes as discussed earlier. Changes in those parameters also have effects on the threshold voltage of a device (Fig. 5.8). Threshold voltage has a direct relation with drain current. So the drain current gradually decreases with the increment of temperature. It also can be confirmed from Fig. 5.8 that after a certain temperature the threshold voltage increases with increasing temperature. An increment of threshold voltage leads to a decrement of drain current (Fig. 6.5). Though using HfO_2 material, the drain current decreases at about 0.02A throughout the range whereas using SiO_2 the drain current decreases at about 0.04A. The relationship has been taken for some constant values of V_{GS} =1V and V_{DS} = 0.75V.

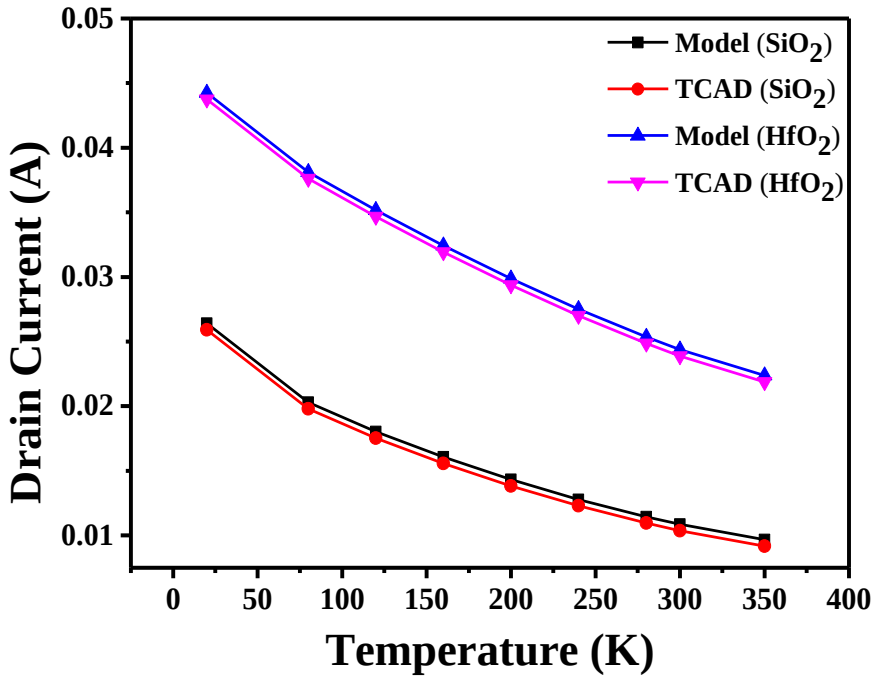

FIGURE 6.5. Drain current with temperature change

Deviation of drain conductance (g_d) with the channel length for a fixed gate-source voltage V_{GS} = 1V and the variation of transconductance (g_m) with the channel length for a fixed value of drain-source voltage V_{DS} = 0.75V with respect to channel length have been represented in Fig 6.6 and 6.7 respectively. The output or drain

conductance (g_d) can be generated from the slope of drain current vs drain voltage graph (between V_{DS} = 0.5V to V_{DS} = 0.75V) and transconductance (g_m) can be extracted from the slope of drain current vs gate voltage graph (between V_{GS} =1V to V_{GS} =1.5V). The DMDG structure has a better transconductance and low value of drain conductance than other devices because of the step function generated in the surface potential (Chiang, 2012) (Fig. 3.3). The drain conductance is almost constant up to 30 nm channel length using SiO_2, but after that it will increase with decreasing channel length. So it can be predicted that, at a small scale channel length the device will generate drain current with a stiffer slope. However, using high-k material the drain conductance becomes almost constant up to 20 nm channel length as well as it increases up to a very small value with the channel length degradation. The value of transconductance is significantly improving with the decreasing value of gate length, it will be advantageous for the device structure at a small scale. By using high-k material the transconductance increases and drain conductance decreases than SiO_2 as stated earlier. This characteristic of high-k material helps to decrease the DIBL and several SCEs generated mainly due to small scale devices.

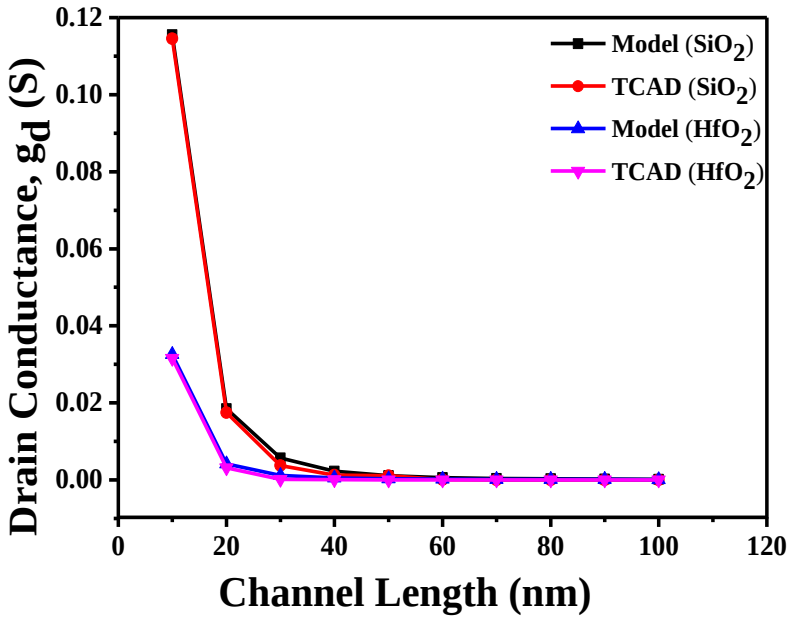

FIGURE 6.6. Drain conductance with channel length

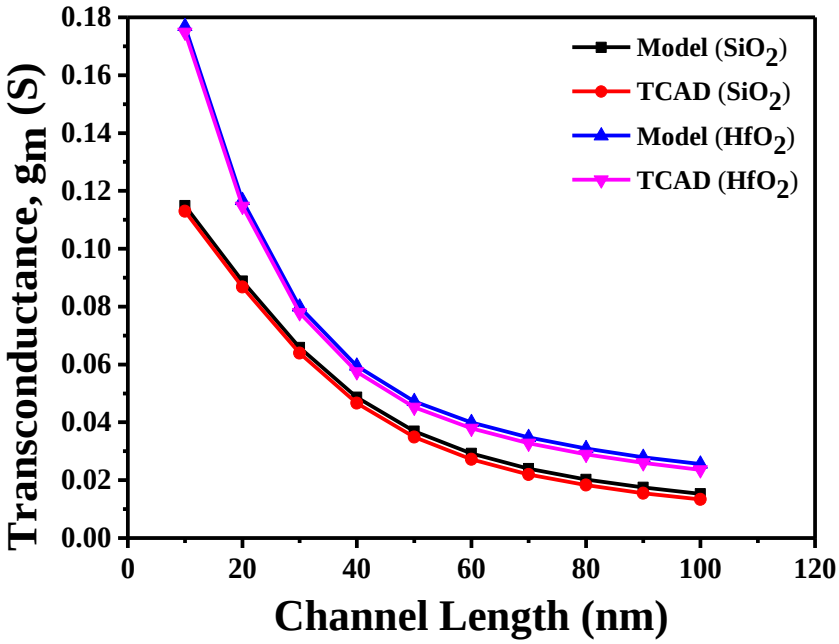

FIGURE 6.7. Transconductance with channel length

Figure 6.8 illustrates the voltage gain with respect to the channel length. Voltage gain is represented by the ratio of drain voltage and gate voltage. Here the voltage gain has been measured from the ratio of transconductance and drain conductance. Using high-k material the voltage gain increases because using it, the transconductance increases and drain conductance decreases than SiO_2. So finally a better performance can be achieved by the uniform doping DMDG structure using high-k substances compared with other devices.

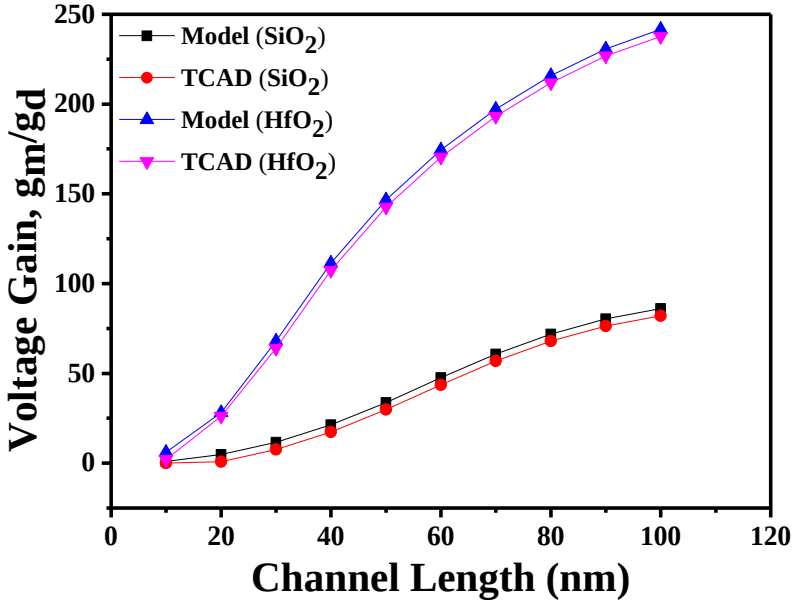

FIGURE 6.8. Voltage gain with channel length

The V-I characteristics curve for different gate voltages of graded nature DMDG structure has been depicted in Fig. 6.9. The variation of drain current with drain voltage has been taken for a particular gate voltage. Similar to uniform doping DMDG structure, the characteristic curve has two regions, linear and saturation. It was illustrated in Fig. 5.18 that, the threshold voltage of GCDMDG is higher than the uniform doping DMDG structure. It implies that the drain current will be lesser in GCDMDG structure than uniform doping DMDG when the other parameters are the same. It is visible from the graphical representation of Fig. 6.9. Due to the higher value of threshold voltage, the minority carrier concentration is lesser in the channel region for the same gate voltage. The drain current depends on the minority carrier concentration at the channel region. Lesser concentration generates a lower amount of current. When the other parameters are same the drain current is about mA range for both the material. However, using high-k material the drain current increases.

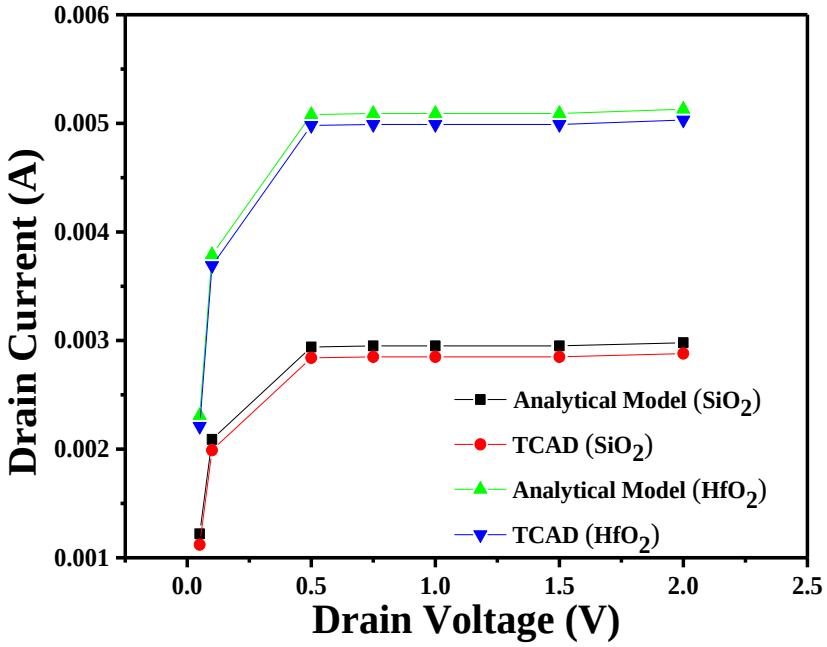

FIGURE 6.9. Drain current with drain voltage for GCDMDG

The drain current characteristics increases with increasing gate voltage value because with the increasing value of gate voltage the minority carrier concentration increases at the channel region. As a result, carrier flow through the channel increases and hence the current flow. This also can be illustrated from Fig. 6.10 that with the

increasing value of gate voltage the drain current increases. Also, it needs to mention that, using high-k material the drain current increases more than SiO_2. With the increasing value of film thickness the drain current increases very slightly shown in Fig. 6.11 alternatively it can be said that with the variation of film thickness the drain current remains almost constant for both oxide materials. This type of performance improvement compared to uniform doping structure (Fig.6.3) will enhance the device performance at a small scale structure. Figure 6.12 represents the change of drain current with oxide thickness. Like uniform doping DMDG structure, here also the drain current increases with decreasing value of oxide thickness. Increasing drain current leads to decreasing threshold voltage, which helps to increase the SCEs. However, using high-k material, the increment is greater than using SiO_2. The temperature has a great impact on the device performance that has been discussed previously. In the case of the GCDMDG structure, the drain current generates opposite characteristics with temperature than the uniform DMDG structure shown in Fig 6.13. Beforehand in the uniform doping DMDG structure, overall the drain current decreases with increasing temperature. However, in the GCDMDG structure, at about 75K temperature the drain current reaches its minimum value. Above and below this temperature the drain current increases. After 150K temperature, it becomes almost constant. That typical characteristic has been symbolized for both high-k and SiO_2 materials. The variation of drain current with temperature has been shown in a bar diagram representation. It can be seen that using SiO_2 and HfO_2, the nature of the characteristics are almost same. To some extent, it differs in case of HfO_2 when the characteristics increases from its minimum value.

Figure 6.14 illustrated the output or drain conductance variation with channel length. As depicted earlier, the drain conductance (g_d) can be generated from the slope of drain current vs drain voltage characteristics (between V_{DS} = 0.5V to V_{DS} = 0.75V) for a fixed gate to source voltage (V_{GS} = 1.3V). The drain conductance value for the device remains almost constant up to 30 nm channel length for SiO_2 oxide material, but below this value, at small channel length, it increases. However, using high-k material, the drain conductance curve remains almost constant up to 20 nm channel length, below this value it increases. It also can be depicted from the figure that, at a

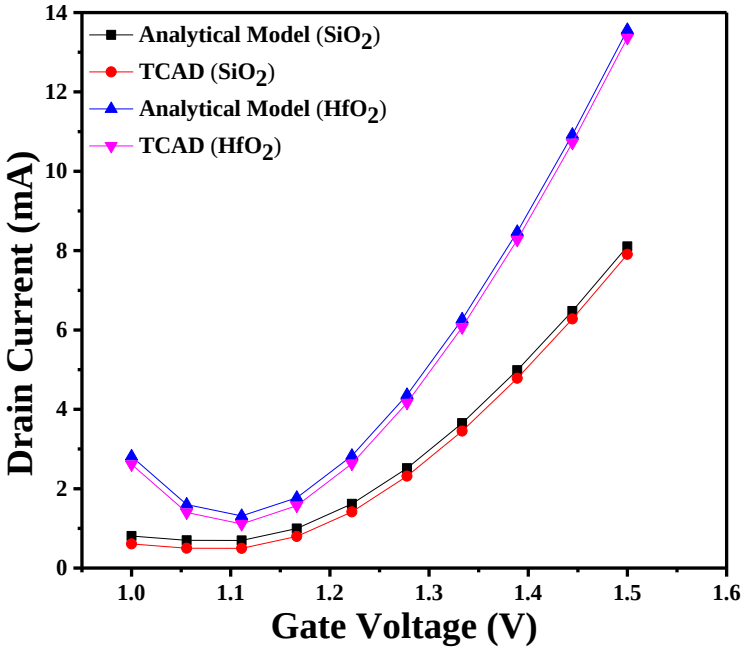

FIGURE 6.10. Drain current with gate voltage for GCDMDG

small channel length of the device the drain conductance generates a lower value in the case of high-k material than SiO_2. On the other side, the transconductance (g_m) which is generated from the slope of drain current vs gate voltage graph (between V_{GS} =1V to V_{GS} =1.5V) for a fixed value of drain-source voltage V_{DS} = 0.75V, increases with decreasing channel length (Fig. 6.15). This value is almost the same for both the oxide materials. The increasing value of transconductance with decreasing channel length enhances the device to better performance and helps to reduce the DIBL as well as several SCEs generated mainly due to small scale device. Voltage gain (ratio of transconductance and drain conductance) with respect to channel length has been represented in Fig. 6.16 for both oxide materials. Here also the voltage gain increases with the increasing value of channel length but the amplification factor is smaller than uniform doping DMDG structure. Using high-k material the performance is better than SiO_2.

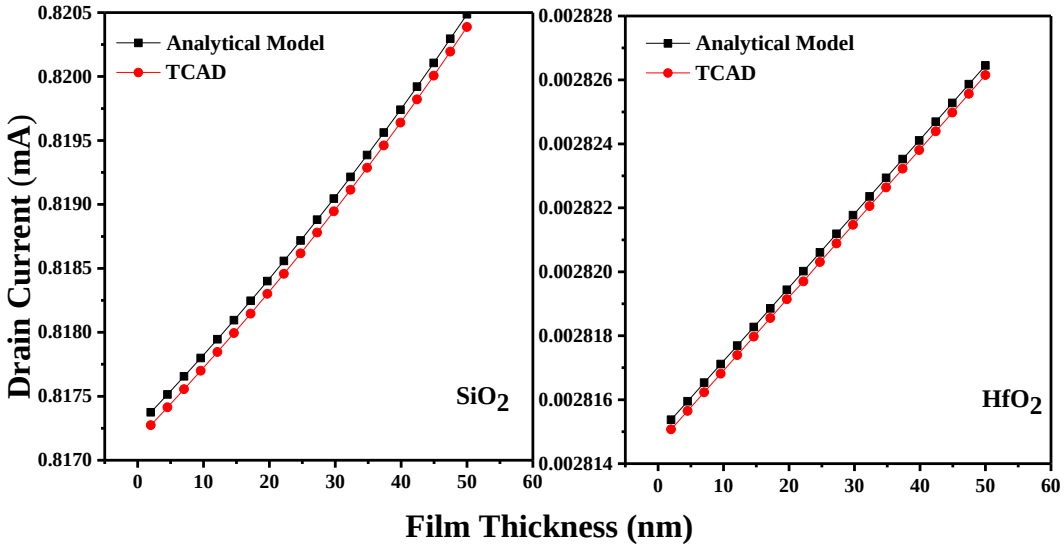

FIGURE 6.11. Drain current with film thickness for GCDMDG

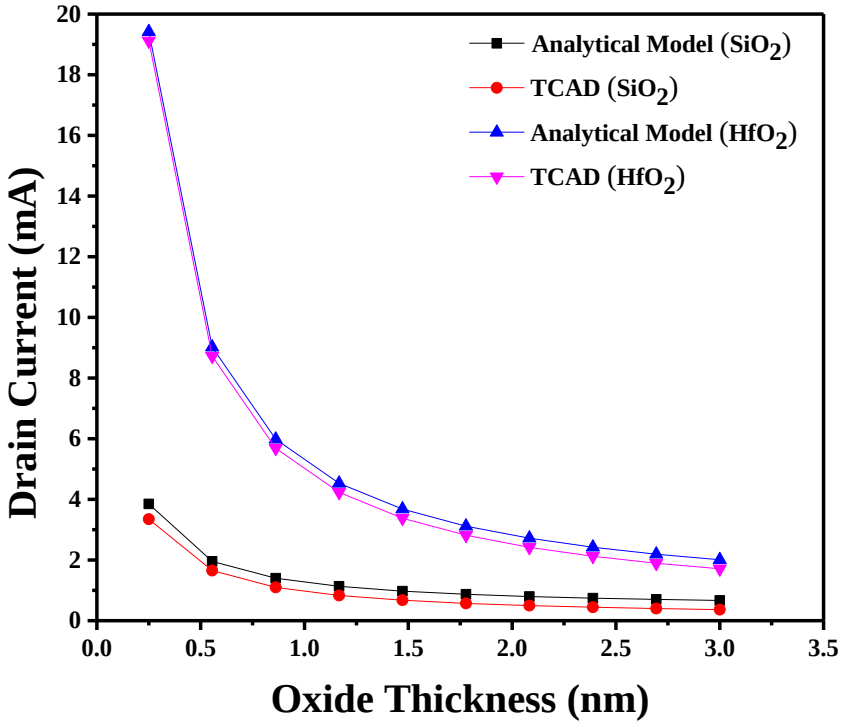

FIGURE 6.12. Drain current with oxide thickness for GCDMDG

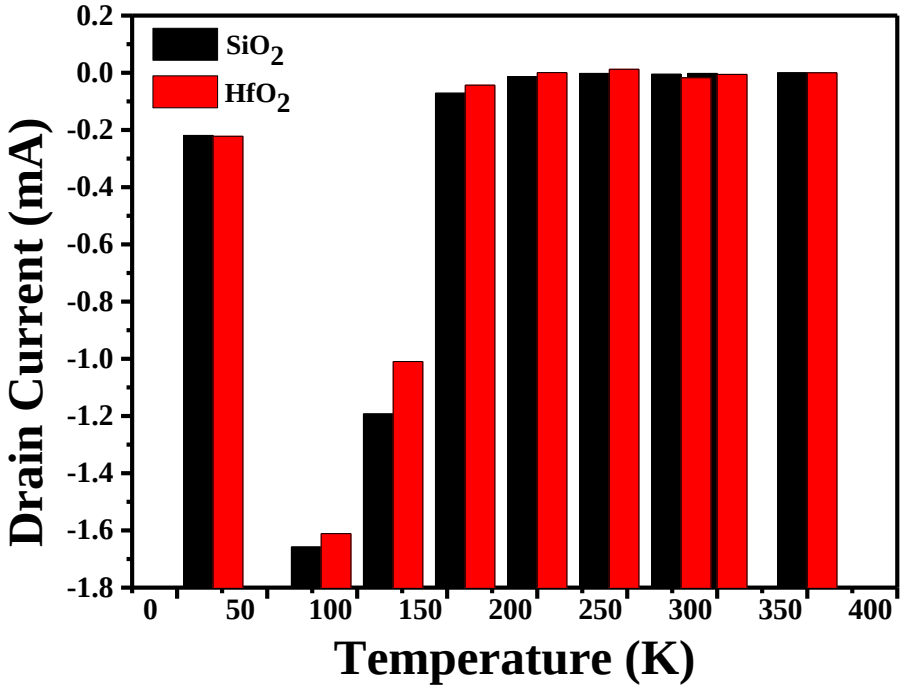

FIGURE 6.13. Drain current with temperature for GCDMDG

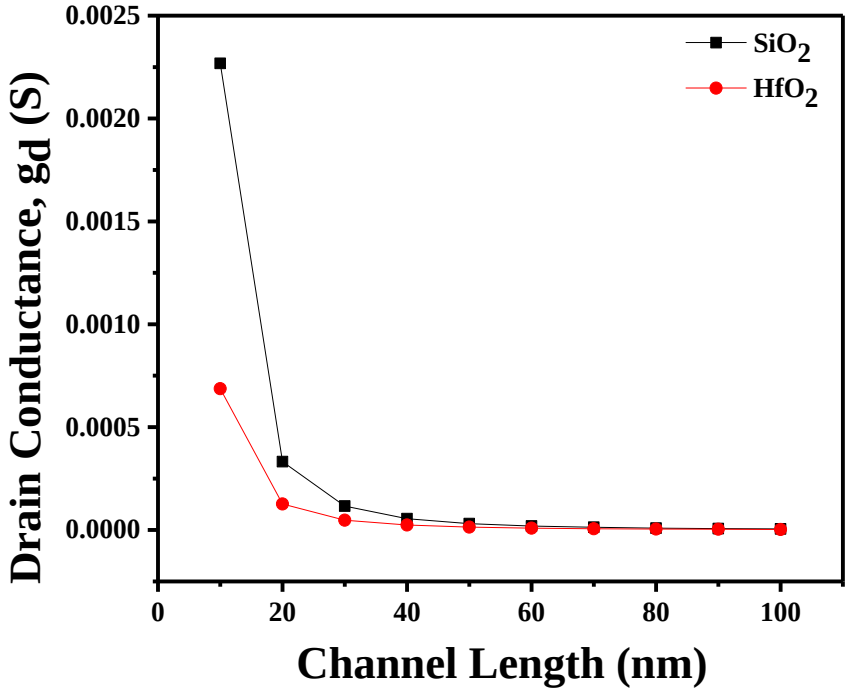

FIGURE 6.14. Drain conductance with channel length for GCDMDG

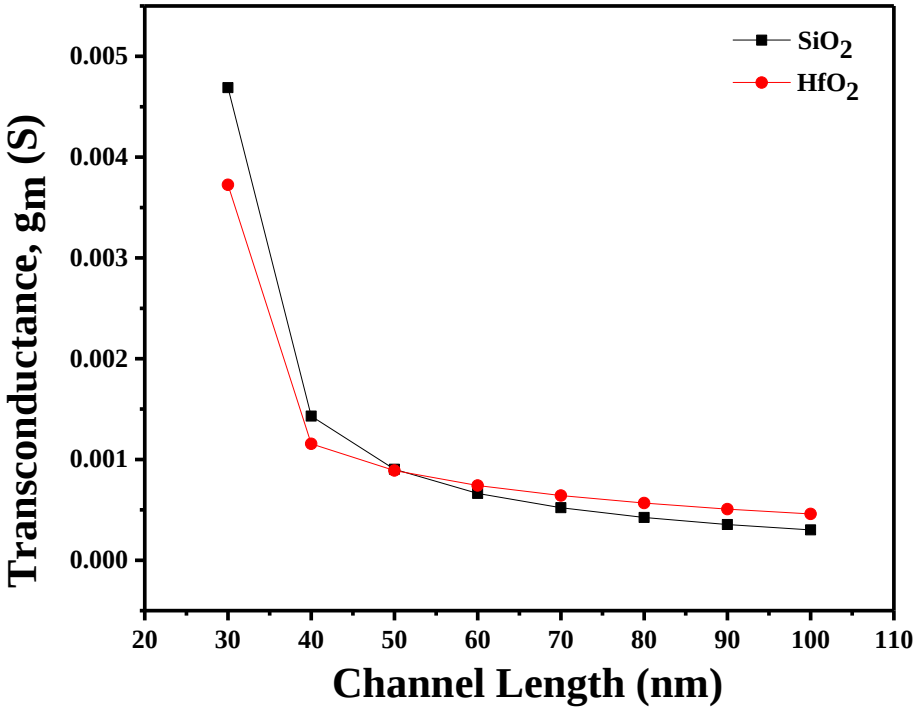

FIGURE 6.15. Transconductance with channel length for GCDMDG

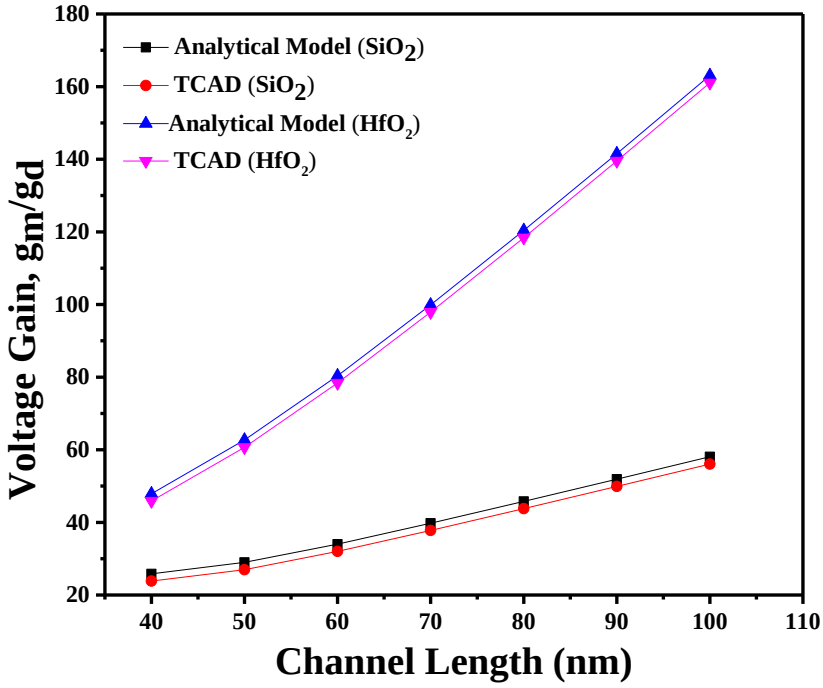

FIGURE 6.16. Voltage gain with channel length for GCDMDG

6.5. Summary

In DMDG and GCDMDG, the variations that are present in their channel doping concentration make them unique from each other. The uniformed doped DMDG structure has a lower value of threshold voltage which is more inclined to enhance the SCEs. It may increase the flow of unwanted current. Lower threshold voltage generates higher drain current and better voltage gain. A higher amplification factor enhances the device's performance. On the other hand, graded channel doping structure generates higher threshold voltage. That is more immune to the flow of unwanted current and hence SCEs. But higher threshold voltage generates lower drain current and low amplification factor. So on the ground of performance analysis, GCDMDG is inferior to uniformed doped DMDG structure but it helps to prevent SCEs at small scale device structure. It makes the device better than a uniformed one. So each one is applicable on its respective ground and exhibits their out most presentation. Again using the high-k as an oxide material boost the performance of DMDG. All these combinations promote DMDG SOI MOSFET using high-k material structure a prime candidature for the CMOS ultra large scale integration (ULSI) chip designing.

CHAPTER

7

Conclusion and Future Scope

7.1. Conclusion

Several electrical parameters such as surface potential, electric field, threshold voltage and drain current of DMDG and GCDMDG have been described in this research work. The problems generated due to fabrication process (effect of interface charge) and environment effects (effects of temperature) upon these characteristics and the modifications on them also have been discussed. The developed model equations strongly follow the device physics and the number of adjustable parameters are retained at the minutest values. The developed model is also valid in all regions even using high-k material as a gate oxide interface.

For any amplifying device's surface potential is a fundamental and crucial feature. The step function generated at the surface potential features of the DMDG structure is unique due to the presence of various polysilicons. Consequently, the surface potential at the drain side is reduced. The surface potential of the high-k material is found to be lower than that of the standard oxide material. In case of high-k materials, the oxide material thickness can be raised to attain a comparable amount of surface potential. To some extent, it will assist to overcome the tunnelling current problem. Involvement of HfO_2 leads to increase in oxide thickness to keep the surface potential and drain current constant. The surface potential can be enhanced for the minimum oxide thickness by adjusting the substrate doping concentration, temperature, and gate-source voltage. Better results can be found by adjusting the device gate length. The threshold voltage drops as the surface potential decreases, resulting in the flow of many uncontrollable currents across the device structure. This undesired current ruins the device's construction. The electric field, threshold voltage, and drain current show the excellent quality of the surface potential. The threshold

voltage can also be increased by increasing the surface potential. Using the DMDG structure, on the other hand, helps to reduce the additional SCEs, formed as a result of scaling down. Hence, it can be concluded that combining a DMDG structure with a high-k dielectric material as dielectric material eliminates all of the challenges associated with scaling down the structure.

The potential profile for GCDMDG structure is better than DMDG. Although it drops due to usage of high-k, it is still higher than a DMDG counterpart. Similar to DMDG it has a step function potential profile with two lobes. The surface potential for the GCDMDG structure can also be enhanced for the minimum thickness value of the oxide level at different temperatures. The electric field over the DMDG structure, on the other hand remains unaffected. In comparison to the single material DG structure, the electric field at the drain side is reduced in the DMDG and GCDMDG structures, which helps to generate fewer hot carriers in the channel and lowers impact ionization. As a result, the GCDMDG structure outperforms the DMDG structure in terms of short channel immunity, gate controllability, carrier transportability, and hot carrier motions. It is concluded that the GCDMDG structure has the largest source-channel potential barrier (i.e., large threshold voltage) among the DMDG, SMG, and GCDMDG structures. It lowers the number of SCEs created as a result of the device structure scaling. DIBL impacts can also be reduced by using GCDMDG structure HCEs. The GCDMDG MOSFET possesses the strongest immunity to SCEs and related HCEs among the three MOSFET devices under investigation. When the GCDMDG structure is combined with a high-k material, most of the challenges that are generally caused as a result of device scaling down can be eliminated.

The threshold voltage is relatively modest in the DMDG device construction, however, it demonstrates a rolling off tendency at a tiny scale channel dimension. This will boost the short channel current. This difficulty can be mitigated to some extent by using high-k materials. On the other hand, the threshold voltage is higher with the GCDMDG structure than with the DMDG, however, it does not show the rolling off nature with tiny scale device dimensions. In this scenario, the threshold voltage is nearly constant. The result is more accurate due to the involvement of high-k material. In the GCDMDG structure, a greater threshold voltage signifies a higher switching voltage. It can be depicted that with decreasing device dimensions the roll off is not

generated, so the induction of leakage current in GCDMDG is lower than in DMDG. It has an advantage over SCEs. The challenges caused by narrow channel effects can be mitigated by utilising high-k material. To counteract the SCEs, the GCDMDG structure with a high-k oxide material as a dielectric constant will be a preferable combination. Other factors such as oxide thickness, temperature, substrate doping, and film thickness and so on have a significant impact upon threshold voltage. These parameters must be taken into account during device manufacturing. In terms of DIBL, both devices produce excellent results. As a result, these devices can counteract this type of short channel impact. In the case of the DMDG structure, the subthreshold swing has also reached the optimal value. Using HfO_2 has yielded better results in all circumstances than silicon dioxide.

As the uniformly doped DMDG structure has a lower threshold voltage, it is more prone to enhance SCEs. It has the potential to enhance the flow of undesired current. Higher drain current and improved voltage gain are generated by lowering the threshold voltage. The device's performance is improved by a larger amplification factor. The threshold voltage of a graded channel doping structure, on the other hand, is higher. As a result, it is more resistant to the flow of undesired current and SCEs. In addition to that, the higher threshold voltage results in reduced drain current and amplification factor. All the characteristics are indicated that the DMDG structure is better on the ground of performance analysis. It has better voltage gain, better transconductance than GCDMDG. While GCDMDG is inferior to uniformly doped DMDG structure in terms of performance, it aids in the prevention of SCEs in small size device structures.

As a result, each device is applicable on its turf and provides its best presentation. DMDG's performance is boosted once further by employing high-k as an oxide material. All of these factors make the DMDG SOI MOSFET with a high-k material structure an excellent candidate for CMOS ULSI chip design. Table 7.1 represents a comparative study of surface potential, electric field, threshold voltage and drain current between DMDG and GCDMDG structure using SiO_2 and HfO_2 material. The minimum value of the surface potential is considered because the threshold voltage depends on it. It generates at about 20 nm channel length position. Threshold voltage has been considered for 50 nm channel length and drain current is consider for 1.2 V

effective gate voltage. The table represents that using HfO_2 the device performance is much better.

Table 7.1. Comparative study of two devices according to parameters

Parameters	Minimum Value of Surface Potential (V)		Average Electric Field (mV/cm)		Threshold Voltage (V)		Drain Current (A)	
Materials	SiO_2	HfO_2	SiO_2	HfO_2	SiO_2	HfO_2	SiO_2	HfO_2
DMDG	-0.024	-0.168	-174	-768	0.146	-0.021	0.0156	0.033
GCDMDG	0.127	-0.004	-174	-768	0.978	0.977	0.003	0.005

7.2. Future Scope

Several advancements have been established over device dimensions in VLSI technology. 3D structures like FINFET with its double gates, triple gates layer have been started for manufacturing by INTEL Corporation. But still, some planar structures like DMDG are the target of many researchers because such planar structures are easy to fabricate.

In this research work, all the model has been established based on classical structure. But with due respect to shrinking, the device dimension has been reduced to below the 10nm range. At this range instead of 'bulk' properties, atomic properties also have to be considered. So the classical structure is not capable to describe all the behaviours. Quantum effects have to be incorporated with classical physics in this case. Nowadays, germanium is a potential candidate which can be used as the channel. The same models can be explored with germanium semiconductors and investigate

their behavioural changes. In this work graded concentration changing with horizontal direction has been considered. But the doping concentration can be changed in a vertical direction also. On application of Green's function model over the graded channel structure with high-k may discover a new dimension of research.

References

Abd El Hamid, H., Guitart, J. R., & Iñíguez, B. (2007). Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs. *IEEE Transactions on Electron Devices*, *54*(6), 1402-1408.

Abdi, M. A., Djeffal, F., Meguellati, M., & Arar, D. (2009, December). Two-dimensional analytical threshold voltage model for nanoscale Graded Channel Gate Stack DG MOSFETs. In *2009 16th IEEE International Conference on Electronics, Circuits and Systems-(ICECS 2009)* (pp. 892-895). IEEE.

Alvarado, J., Iniguez, B., Estrada, M., Flandre, D., & Cerdeira, A. (2010). Implementation of the symmetric doped double- gate MOSFET model in Verilog- A for circuit simulation. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, *23*(2), 88-106.

Arora, N. D., Rios, R., Huang, C. L., & Raol, K. (1994). PCIM: A physically based continuous short-channel IGFET model for circuit simulation. *IEEE transactions on electron devices*, *41*(6), 988-997.

Assaderaghi, F., Kop, P. K., & Hu, C. (1993). Observation of velocity overshoot in silicon inversion layers. *IEEE electron device letters*, *14*(10), 484-486.

Auth, C. P., & Plummer, J. D. (1997). Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. *IEEE Electron Device Letters*, *18*(2), 74-76.

B, B. (2019). Modeling simulation and analysis of double gate MOSFET structures for biosensing applications. Ph.D, Information and communication engineering, Anna University, Chennai.

Baishya, S. (2009). A surface potential and quasi-Fermi potential based drain current model for pocket-implanted MOS transistors in subthreshold regime. *Microelectronics Reliability*, *49*(7), 681-688.

Baishya, S., Mallik, A., & Sarkar, C. K. (2007). Subthreshold surface potential and drain current models for short-channel pocket-implanted MOSFETs. *Microelectronic engineering*, *84*(4), 653-662.

Balestra, F., Cristoloveanu, S., Benachir, M., Brini, J., & Elewa, T. (1987). Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance. *IEEE Electron Device Letters*, *8*(9), 410-412.

Bhattacherjee, S., & Biswas, A. (2007). Modeling of threshold voltage and subthreshold slope of nanoscale DG MOSFETs. *Semiconductor science and technology*, *23*(1), 015010.

Bouazra, A., Nasrallah, S., Said, M., & Poncet, A. (2008). Current tunnelling in MOS devices with Al2O3/SiO2 gate dielectric. *Physics Research International*, *2008*.

Cerdeira, A., Estrada, M., Alvarado, J., Garduño, I., Contreras, E., Tinoco, J., & Flandre, D. (2013). Review on double-gate MOSFETs and FinFETs modeling. *Facta universitatis-series: Electronics and Energetics*, *26*(3), 197-213.

Cerdeira, A., Iniguez, B., & Estrada, M. (2008). Compact model for short channel symmetric doped double-gate MOSFETs. *Solid-State Electronics*, *52*(7), 1064-1070.

Cerdeira, A., Moldovan, O., Iñiguez, B., & Estrada, M. (2008). Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs. *Solid-State Electronics*, *52*(5), 830-837.

Chaudhry, A., & Kumar, M. J. (2004). Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability*, *4*(1), 99-109.

Chaudhry, A., & Kumar, M. J. (2004). Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability*, *4*(1), 99-109.

Chaudhry, A., & Kumar, M. J. (2004). Investigation of the novel attributes of a fully depleted dual-material gate SOI MOSFET. *IEEE Transactions on Electron Devices*, *51*(9), 1463-1467.

Chen, Q., Harrell, E. M., & Meindl, J. D. (2003). A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs. *IEEE Transactions on electron devices*, *50*(7), 1631-1637.

Chen, S. S., & Kuo, J. B. (1996). Deep submicrometer double-gate fully-depleted SOI PMOS devices: A concise short-channel effect threshold voltage model using a quasi-2D approach. *IEEE Transactions on Electron Devices*, *43*(9), 1387-1393.

Chen, X., Zhao, H., Xiong, Y., Wei, F., Du, J., Tang, Z., & Yan, J. (2016). Study of Hf-Ti-O thin film as high-k gate dielectric and application for ETSOI MOSFETs. *Journal of Electronic Materials*, *45*(8), 4407-4411.

Chen, Y. G., Kuo, J. B., Yu, Z., & Dutton, R. W. (1995). An analytical drain current model for short-channel fully-depleted ultrathin silicon-on-insulator NMOS devices. *Solid-State Electronics*, *38*(12), 2051-2057.

Chiang, T. K. (2009). A new two-dimensional subthreshold behavior model for the short-channel asymmetrical dual-material double-gate (ADMDG) MOSFET's. *Microelectronics Reliability*, *49*(7), 693-698.

Chiang, T. K. (2009). A new two-dimensional subthreshold behavior model for the short-channel asymmetrical dual-material double-gate (ADMDG) MOSFET's. *Microelectronics Reliability*, *49*(7), 693-698.

Chiang, T. K. (2012). A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs. *IEEE Transactions on Electron Devices*, *59*(9), 2284-2289.

Chiang, T. K. (2016). A short-channel-effect-degraded noise margin model for junctionless double-gate MOSFET working on subthreshold CMOS logic gates. *IEEE Transactions on Electron Devices*, *63*(8), 3354-3359.

Chiu, W. Y., & Horng, J. W. (2011). Voltage-mode biquadratic filters with one input and five outputs using two DDCCs.

Choi, J. H., Mao, Y., & Chang, J. P. (2011). Development of hafnium based high-k materials—A review. *Materials Science and Engineering: R: Reports*, *72*(6), 97-136.

Chou, S. Y., Antoniadis, D. A., & Smith, H. I. (1985). Observation of electron velocity overshoot in sub-100-nm-channel MOSFET's in silicon. *IEEE Electron Device Letters*, *6*(12), 665-667.

Colinge, J. P. (2004). Multiple-gate soi mosfets. *Solid-state electronics*, *48*(6), 897-905.

Colinge, J. P. (Ed.). (2008). *FinFETs and other multi-gate transistors* (Vol. 73). New York: Springer.

Colinge, J. P. (Ed.). (2008). *FinFETs and other multi-gate transistors* (Vol. 73). New York: Springer.

Colinge, J. P., Gao, M. H., Romano-Rodriguez, A., Maes, H., & Claeys, C. (1990, December). Silicon-on-insulator'gate-all-around device'. In *International Technical Digest on Electron Devices* (pp. 595-598). IEEE.

Colinge, J. P., Gao, M. H., Romano-Rodriguez, A., Maes, H., & Claeys, C. (1990, December). Silicon-on-insulator'gate-all-around device'. In *International Technical Digest on Electron Devices* (pp. 595-598). IEEE.

Colinge, J. P., Gao, M. H., Romano-Rodriguez, A., Maes, H., & Claeys, C. (1990, December). Silicon-on-insulator'gate-all-around device'. In *International Technical Digest on Electron Devices* (pp. 595-598). IEEE.

Contreras, E., Cerdeira, A., Alvarado, J., & Pavanello, M. A. (2010). Application of the symmetric doped double-gate model in circuit simulation containing double-gate graded-channel transistors. *Journal of Integrated Circuits and Systems*, *5*(2), 110-115.

Contreras, E., Cerdeira, A., Alvarado, J., & Pavanello, M. A. (2010). Application of the symmetric doped double-gate model in circuit simulation containing double-gate graded-channel transistors. *Journal of Integrated Circuits and Systems*, *5*(2), 110-115.

Darwin, S., & Arun Samuel, T. S. (2020). A holistic approach on Junctionless dual material double gate (DMDG) MOSFET with high k gate stack for low power digital applications. *Silicon*, *12*(2), 393-403.

Das, D. (2015). VLSI design. *Oxford University Press*.

De Almeida, R. M. C., & Baumvol, I. J. R. (2003). Reaction–diffusion in high-k dielectrics on Si. *Surface Science Reports*, *49*(1-3), 1-114.R.

Dennard, R. H., Gaensslen, F. H., Yu, H. N., Rideout, V. L., Bassous, E., & LeBlanc, A. R. (1974). Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE Journal of solid-state circuits*, *9*(5), 256-268.

Desgreniers, S., & Lagarec, K. (1999). High-density ZrO 2 and HfO 2: Crystalline structures and equations of state. *Physical Review B*, *59*(13), 8467.

Dhiman, G. (2018). Ph.D, Engineering, Mody University of science & technology, Rajasthan.

Diagne, B., Prégaldiny, F., Lallement, C., Sallese, J. M., & Krummenacher, F. (2008). Explicit compact model for symmetric double-gate MOSFETs including solutions for small-geometry effects. *Solid-State Electronics*, *52*(1), 99-106.

E. Tutorial. [Online] Available: https://www.electronicstutorials.ws/capacitor/cap_1.html.

Faggin, F., Hoff, M. E., Mazor, S., & Shima, M. (1996). The History of the 4004. *Ieee Micro*, *16*(6), 10-20.

Farrah, H. R., & Steinberg, R. F. (1967). Analysis of double-gate thin-film transistor. *IEEE Transactions on Electron Devices*, *14*(2), 69-74.

Francis, P., Terao, A., Flandre, D., & Van de Wiele, F. (1994). Modeling of ultrathin double-gate nMOS/SOI transistors. *IEEE Transactions on Electron Devices*, *41*(5), 715-720.

Frank, D. J., Dennard, R. H., Nowak, E., Solomon, P. M., Taur, Y., & Wong, H. S. P. (2001). Device scaling limits of Si MOSFETs and their application dependencies. *Proceedings of the IEEE*, *89*(3), 259-288.

Garduño, S. I., Cerdeira, A., Estrada, M., Alvarado, J., Kilchytska, V., & Flandre, D. (2011). Contribution of carrier tunneling and gate induced drain leakage effects to the gate and drain currents of fin–shaped field–effect transistors. *Journal of Applied Physics*, *109*(8), 084524.

Garduño, S. I., Cerdeira, A., Estrada, M., Alvarado, J., Kilchytska, V., & Flandre, D. (2011). Contribution of carrier tunneling and gate induced drain leakage effects to the gate and drain currents of fin–shaped field–effect transistors. *Journal of Applied Physics*, *109*(8), 084524.

Garrigues, M., & Belland, B. (1986). Hot carrier injection into SiO 2 instabilities in silicon devices. *IEEE journal of Solid State Circuits*, *1*, 441-502.

Goel, E., Kumar, S., Singh, K., Singh, B., Kumar, M., & Jit, S. (2016). 2-D analytical modeling of threshold voltage for graded-channel dual-material double-gate MOSFETs. *IEEE Transactions on Electron Devices*, *63*(3), 966-973.

Guha, K., Kumar, M., Agarwal, S., & Baishya, S. (2015). A modified capacitance model of RF MEMS shunt switch incorporating fringing field effects of perforated beam. *Solid-State Electronics*, *114*, 35-42.

Gupta, N., (2019). Performance Enhancement of Multigate MOSFET Using Engineering Technique-A Review. *Ijrar*, 6(2), 431-440.

Haensch, W., Nowak, E. J., Dennard, R. H., Solomon, P. M., Bryant, A., Dokumaci, O. H., & Fischetti, M. V. (2006). Silicon CMOS devices beyond scaling. *IBM Journal of Research and Development*, *50*(4.5), 339-361.

Han, J., & Ferry, D. K. (1998). Non-equilibrium electron dynamics phenomena in scaled sub-100 nm gate length metal semiconductor field effect transistors: Gate-fringing, velocity overshoot, and short-channel tunneling. *Japanese journal of applied physics*, *37*(9R), 4672.

Hoefflinger, B. (2011). ITRS: The international technology roadmap for semiconductors. In *Chips 2020* (pp. 161-174). Springer, Berlin, Heidelberg.

Hosseini, M., Zhu, G., & Peter, Y. A. (2007). A new formulation of fringing capacitance and its application to the control of parallel-plate electrostatic micro actuators. *Analog Integrated Circuits and Signal Processing*, *53*(2), 119-128.

Jin, X., Liu, X., Lee, J. H., & Lee, J. H. (2010). A continuous current model of fully-depleted symmetric double-gate MOSFETs considering a wide range of body doping concentrations. *Semiconductor science and technology*, *25*(5), 055018.

Kahng, D. (1976). A historical perspective on the development of MOS transistors and related devices. *IEEE Transactions on Electron Devices*, *23*(7), 655-657.

Kaur, H., Kabra, S., Haldar, S., & Gupta, R. S. (2007). An analytical drain current model for graded channel cylindrical/surrounding gate MOSFET. *Microelectronics Journal*, *38*(3), 352-359.

Kaur, H., Kabra, S., Haldar, S., & Gupta, R. S. (2008). An analytical threshold voltage model for graded channel asymmetric gate stack (GCASYMGAS) surrounding gate MOSFET. *Solid-state electronics*, *52*(2), 305-311.

Khan, H. R., Mamaluy, D., & Vasileska, D. (2008). Approaching optimal characteristics of 10-nm high-performance devices: A quantum transport simulation study of Si FinFET. *IEEE transactions on Electron Devices*, *55*(3), 743-753.

Khan, H. R., Mamaluy, D., & Vasileska, D. (2008). Approaching optimal characteristics of 10-nm high-performance devices: A quantum transport simulation study of Si FinFET. *IEEE transactions on Electron Devices*, *55*(3), 743-753.

Kilby, J. S. (1976). Invention of the integrated circuit. *IEEE Transactions on electron devices*, *23*(7), 648-654.

Kumar, A., Nagumo, T., Tsutsui, G., & Hiramoto, T. (2004). Analytical model of body factor in short channel bulk MOSFETs for low voltage applications. *Solid-State Electronics*, *48*(10-11), 1763-1766.

Kumar, M. J., & Chaudhry, A. (2004). Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs. *IEEE Transactions on Electron Devices*, *51*(4), 569-574.

Kumar, M. J., & Reddy, G. V. (2004). Evidence for suppressed short-channel effects in deep submicron dual-material gate (DMG) partially depleted SOI MOSFETs–A two-dimensional analytical approach. *Microelectronic engineering*, *75*(4), 367-374.

Kumar, P. R., & Mahapatra, S. (2009). Quantum threshold voltage modeling of short channel quad gate silicon nanowire transistor. *IEEE Transactions on Nanotechnology*, *10*(1), 121-128.

Kumar, S., Goel, E., Singh, K., Singh, B., Kumar, M., & Jit, S. (2016). A compact 2-D analytical model for electrical characteristics of double-gate tunnel field-effect transistors with a SiO 2/High-$ k $ stacked gate-oxide structure. *IEEE Transactions on Electron Devices*, *63*(8), 3291-3299.

Kumar, S., Goel, E., Singh, K., Singh, B., Singh, P. K., Baral, K., & Jit, S. (2017). 2-D analytical modeling of the electrical characteristics of dual-material double-gate TFETs with a SiO 2/HfO 2 stacked gate-oxide structure. *IEEE Transactions on Electron Devices*, *64*(3), 960-968.

Kumar, V., Thomas, D. M., Shruti, K., Samuel, P. C., & Kumar, M. (2011, April). Impact of gate engineering on double gate MOSFETs using high-k dielectrics. In *2011 3rd International Conference on Electronics Computer Technology* (Vol. 1, pp. 31-34). IEEE.

Kumari, V., Ilango, A., Saxena, M., & Gupta, M. (2014, December). Charge-based modeling of channel material-engineered P-type double gate MOSFET. In *2014 IEEE 2nd International Conference on Emerging Electronics (ICEE)* (pp. 1-4). IEEE.

Lazaro, A., Cerdeira, A., Nae, B., Estrada, M., & Iñiguez, B. (2009). High-frequency compact analytical noise model for double-gate metal-oxide-semiconductor field-effect transistor. *Journal of Applied Physics*, *105*(3), 034510.

Lee, C. W., Ferain, I., Afzalian, A., Yan, R., Akhavan, N. D., Razavi, P., & Colinge, J. P. (2010). Performance estimation of junctionless multigate transistors. *Solid-State Electronics*, *54*(2), 97-103.

Lilienfeld, J. E. (1926). *Method and apparatus for controlling electric currents. US Patent, 1745175* (Vol. 28). 1930-01.

Lin, H. H., & Taur, Y. (2017). Effect of source–drain doping on subthreshold characteristics of short-channel DG MOSFETs. *IEEE Transactions on Electron Devices*, *64*(12), 4856-4860.

Liu, F., He, J., Zhang, J., Chen, Y., & Chan, M. (2008). A non-charge-sheet analytic model for symmetric double-gate MOSFETs with smooth transition between partially and fully depleted operation modes. *IEEE transactions on electron devices*, *55*(12), 3494-3502.

Lolivier, J., Widiez, J., Vinet, A., Poiroux, T., Dauge, F., Previtali, B., & Deleonibus, S. (2004, September). Experimental comparison between double gate, ground plane, and single gate SOI CMOSFETs. In *Proceedings of the 30th European Solid-State Circuits Conference (IEEE Cat. No. 04EX850)* (pp. 77-80). IEEE.

Long, W., Ou, H., Kuo, J. M., & Chin, K. K. (1999). Dual-material gate (DMG) field effect transistor. *IEEE Transactions on Electron Devices*, *46*(5), 865-870.

Lou, H., Zhang, L., Zhu, Y., Lin, X., Yang, S., He, J., & Chan, M. (2012). A junctionless nanowire transistor with a dual-material gate. *IEEE Transactions on Electron Devices*, *59*(7), 1829-1836.

Lowther, J. E., Dewhurst, J. K., Leger, J. M., & Haines, J. (1999). Relative stability of ZrO 2 and HfO 2 structural phases. *Physical Review B*, *60*(21), 14485.

Lu, H., & Taur, Y. (2006). An analytic potential model for symmetric and asymmetric DG MOSFETs. *IEEE Transactions on Electron Devices*, *53*(5), 1161-1168.

Maity, N. P., & Maity, R. (2020). Tunneling Current Density and Tunnel Resistivity: Application to High-k Material HfO2. *High-k Gate Dielectric Materials: Applications with Advanced Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)*, 73.

Maity, N. P., Maity, R., & Baishya, S. (2017). Voltage and oxide thickness dependent tunneling current density and tunnel resistivity model: application to high-k material HfO2 based MOS devices. *Superlattices and Microstructures*, *111*, 628-641.

Maity, N. P., Maity, R., & Baishya, S. (2018). A tunneling current model with a realistic barrier for ultra-thin high-k dielectric ZrO2 material based MOS devices. *Silicon*, *10*(4), 1645-1652.

Maity, N. P., Maity, R., & Baishya, S. (2019). An analytical model for the surface potential and threshold voltage of a double-gate heterojunction tunnel FinFET. *Journal of computational electronics*, *18*(1), 65-75.

Maity, N. P., Maity, R., Maity, S., & Baishya, S. (2019). A new surface potential and drain current model of dual material gate short channel metal oxide semiconductor field effect transistor in sub-threshold regime: application to high-k material HfO2. *Journal of Nanoelectronics and Optoelectronics*, *14*(6), 868-876.

Maity, N. P., Maity, R., Maity, S., & Baishya, S. (2019). Comparative analysis of the quantum FinFET and trigate FinFET based on modeling and simulation. *Journal of Computational Electronics*, *18*(2), 492-499.

Maity, N. P., Maity, R., Thapa, R. K., & Baishya, S. (2014). Study of interface charge densities for ZrO2 and HfO2 based metal-oxide-semiconductor devices. *Advances in Materials Science and Engineering*, *2014*.

Maity, N. P., Maity, R., Thapa, R. K., & Baishya, S. (2015). Effect of image force on tunneling current for ultra thin oxide layer based metal oxide semiconductor devices. *Nanoscience and Nanotechnology Letters*, *7*(4), 331-333.

Maity, N. P., Maity, R., Thapa, R. K., & Baishya, S. (2016). A tunneling current density model for ultra thin HfO2 high-k dielectric material based MOS devices. *Superlattices and Microstructures*, *95*, 24-32.

Maity, N. P., Pandey, A., Chakraborty, S., & Roy, M. (2011). High-k HfO2 based metal-oxide-semiconductor devices using silicon and silicon carbide semiconductor.

Maria Jossy, A., Vigneswaran, T., Malarvizhi, S., & Nagarajan, K. K. (2019). Characterization and modeling of dual material double gate tunnel field effect transistor using superposition approximation method. *Concurrency and Computation: Practice and Experience*, *31*(14), e4860.

Mohankumar, N., Syamal, B., & Sarkar, C. K. (2010). Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs. *IEEE transactions on Electron Devices*, *57*(4), 820-826.

Mohankumar, N., Syamal, B., Sarkar, C. K., & Ravi, S. (2008, December). Influence of gate engineering on the analog and RF performance of DG MOSFETs. In *2008 International Conference on Computing, Communication and Networking* (pp. 1-4). IEEE.

Moore, G. E. (1965). Cramming more components onto integrated circuits.

Moore, G. E. (1975). Progress in digital integrated electronic in Electron devices meeting, *Washington, DC*, 21, 11-13.

Moore, G. E. (1998). Cramming more components onto integrated circuits. *Proceedings of the IEEE*, 86(1), 82-85.

Moore, G. E. (2006). Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff. *IEEE solid-state circuits society newsletter*, *11*(3), 33-35.

Muller, D. A., Sorsch, T., Moccio, S., Baumann, F. H., Evans-Lutterodt, K., & Timp, G. (1999). The electronic structure at the atomic scale of ultrathin gate oxides. *Nature*, *399*(6738), 758-761.

Nakagawa, T., Sekigawa, T., Tsutsumi, T., Suzuki, E., & Koike, H. (2003, December). Primary consideration on compact modeling of DG MOSFETs with four-terminal operation mode. In *2003 Nanotechnology Conference and Trade Show-Nanotech 2003* (pp. 330-333).

Nandi, A., Pandey, N., & Dasgupta, S. (2018). Analytical modeling of gate-stack DG-MOSFET in subthreshold regime by Green's function approach. *IEEE Transactions on Electron Devices*, *65*(10), 4724-4728.

Narang, R., Saxena, M., Gupta, R. S., & Gupta, M. (2013). Impact of temperature variations on the device and circuit performance of tunnel FET: a simulation study. *IEEE transactions on Nanotechnology*, *12*(6), 951-957.

Narang, R., Saxena, M., Gupta, R. S., & Gupta, M. (2013). Impact of temperature variations on the device and circuit performance of tunnel FET: a simulation study. *IEEE transactions on Nanotechnology*, *12*(6), 951-957.

Narendar, V., & Girdhardas, K. A. (2018). Surface potential modeling of graded-channel gate-stack (GCGS) high-K dielectric dual-material double-gate (DMDG) MOSFET and analog/RF performance study. *Silicon*, *10*(6), 2865-2875.

NCBI. [Online] Available: https://www.ncbi.nlm.nih.gov/books/NBK321721/figure/oin_tutorial.F3/

Neaman, D. (1997). *Semiconductor Physics and Devices* (IRWIN, Chicago). 10, 457.

Neamen, D. A. (1992). Semiconductor physics and devices. *McGraw-Hill*.

Nicollian, E. H., & Brews, J. R. (2002). *MOS (metal oxide semiconductor) physics and technology*. John Wiley & Sons.

Noor, S. L., Safa, S., Khan, M., & Rahman, Z. (2016). Dual-material double-gate tunnel FET: Gate threshold voltage modeling and extraction. *Journal of Computational Electronics*, *15*(3), 763-769.

Ohl, R. S. (1946). *U.S. Patent No. 2,402,662*. Washington, DC: U.S. Patent and Trademark Office.

Orouji, A. A., & Rahimian, M. (2012). Leakage current reduction in nanoscale fully-depleted SOI MOSFETs with modified current mechanism. *Current Applied Physics*, *12*(5), 1366-1371.

Ortiz-Conde, A., & Garcia-Sanchez, F. J. (2012). A rigorous classical solution for the drain current of doped symmetric double-gate MOSFETs. *IEEE transactions on electron devices*, *59*(9), 2390-2395.

Ortiz-Conde, A., García-Sánchez, F. J., & Malobabic, S. (2005). Analytic solution of the channel potential in undoped symmetric dual-gate MOSFETs. *IEEE Transactions on electron Devices*, *52*(7), 1669-1672.

Ortiz-Conde, A., Garcia-Sanchez, F. J., Muci, J., Malobabic, S., & Liou, J. J. (2006). A review of core compact models for undoped double-gate SOI MOSFETs. *IEEE Transactions on Electron Devices*, *54*(1), 131-140.

P. Ghosh. (2013). Analytical modeling and simulation of dual material gate stack architecture cylindrical/ surroundedgate MOSFET. *Ph.D, Electronics Science, University of Delhi, Delhi*.

Pal, A., & Sarkar, A. (2014). Analytical study of dual material surrounding gate MOSFET to suppress short-channel effects (SCEs). *Engineering Science and Technology, an International Journal*, *17*(4), 205-212.

Panchanan, S., Maity, R., Baishya, S., & Maity, N. P. (2021). A surface potential model for tri-gate metal oxide semiconductor field effect transistor: analysis below 10 nm channel length. *Engineering science and technology, an international journal*, *24*(4), 879-889.

Panigrahy, S., & Sahu, P. (2013). Performance enhancement and reduction of short channel effects of nano-MOSFET by using graded channel engineering," *IEEE International Conference on Circuits, Power and Computing Technologies (ICCPCT) Proceedings, 2013*, pp. 787-792.

Parker, G. W. (2002). Electric field outside a parallel plate capacitor. *American Journal of Physics*, *70*(5), 502-507.

Plummer, J. D., & Griffin, P. B. (2001). Material and process limits in silicon VLSI technology. *Proceedings of the IEEE*, *89*(3), 240-258.

Prégaldiny, F., Krummenacher, F., Diagne, B., Pêcheux, F., Sallese, J. M., & Lallement, C. (2006). Explicit modelling of the double- gate MOSFET with

VHDL- AMS. *INTERNATIONAL JOURNAL OF NUMERICAL MODELLING: electronic networks, devices and fields*, *19*(3), 239-256.

Puthenkovilakam, R., & Chang, J. P. (2004). An accurate determination of barrier heights at the HfO_2 / Si interfaces. *Journal of applied physics*, *96*(5), 2701-2707.

Quan, Y. C., Lee, J. E., Kang, H., Roh, Y., Jung, D., & Yang, C. W. (2002). Formation of reliable HfO2/HfSixOy gate-dielectric for metal-oxide-semiconductor devices. *Japanese journal of applied physics*, *41*(11S), 6904.

Ramesh, R. (2017). Influence of gate and channel engineering on multigate MOSFETs-A review. *Microelectronics journal*, *66*, 136-154.

Raskin, J. P., Chung, T. M., Kilchytska, V., Lederer, D., & Flandre, D. (2006). Analog/RF performance of multiple gate SOI devices: wideband simulations and characterization. *IEEE Transactions on Electron Devices*, *53*(5), 1088-1095.

Reddy, G. V., & Kumar, M. J. (2005). A new dual-material double-gate (DMDG) nanoscale SOI MOSFET-two-dimensional analytical modeling and simulation. *IEEE Transactions on Nanotechnology*, *4*(2), 260-268.

Ribes, G., Mitard, J., Denais, M., Bruyere, S., Monsieur, F., Parthasarathy, C., & Ghibaudo, G. (2005). Review on high-k dielectrics reliability issues. *IEEE Transactions on Device and materials Reliability*, *5*(1), 5-19.

Roldan, J. B., Gamiz, F., Lopez-Villanueva, J. A., & Carceller, J. E. (1997). Modeling effects of electron-velocity overshoot in a MOSFET. *IEEE Transactions on Electron Devices*, *44*(5), 841-846.

Roldan, J. B., Gamiz, F., Lopez-Villanueva, J. A., Cartujo, P., & Carceller, J. E. (1998). A model for the drain current of deep submicrometer MOSFETs including electron-velocity overshoot. *IEEE Transactions on Electron Devices*, *45*(10), 2249-2251.

S. Engineering. [Online] Available: https://semiengineering.com/scaling-up-and-down/

Sai-Halasz, G. A., Wordeman, M. R., Kern, D. P., Rishton, S., & Ganin, E. (1988). High transconductance and velocity overshoot in NMOS devices at the 0.1-mu m gate-length level. *IEEE Electron Device Letters*, *9*(9), 464-466.

Sallese, J. M., Chevillon, N., Pregaldiny, F., Lallement, C., & Iniguez, B. (2010). The equivalent-thickness concept for doped symmetric DG MOSFETs. *IEEE transactions on electron devices*, *57*(11), 2917-2924.

Salmani-Jelodar, M., Ilatikhameneh, H., Kim, S., Ng, K., Sarangapani, P., & Klimeck, G. (2016). Optimum high-k oxide for the best performance of ultra-scaled double-gate MOSFETs. *IEEE Transactions on Nanotechnology*, *15*(6), 904-910.

Sarkar, A., Das, A. K., De, S., & Sarkar, C. K. (2012). Effect of gate engineering in double-gate MOSFETs for analog/RF applications. *Microelectronics Journal*, *43*(11), 873-882.

Saurabh, S., & Kumar, M. J. (2010). Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. *IEEE transactions on Electron Devices*, *58*(2), 404-410.

Saxena, M., Haldar, S., Gupta, M., & Gupta, R. S. (2002). Physics-based analytical modeling of potential and electrical field distribution in dual material gate (DMG)-MOSFET for improved hot electron effect and carrier transport efficiency. *IEEE Transactions on Electron Devices*, *49*(11), 1928-1938.

Saxena, M., Haldar, S., Gupta, M., & Gupta, R. S. (2004). Design considerations for novel device architecture: hetero-material double-gate (HEM-DG) MOSFET with sub-100 nm gate length. *Solid-State Electronics*, *48*(7), 1169-1174.

Scaff, J. H., & Ohl, R. S. (1947). Development of silicon crystal rectifiers for microwave radar receivers. *The Bell System Technical Journal*, *26*(1), 1-30.

Schaller, R. R. (2004). *Technological innovation in the semiconductor industry: a case study of the International Technology Roadmap for Semiconductors (ITRS)* (p. xxii). Fairfax, VA: George Mason University.

Seoane, N., Indalecio, G., Nagy, D., Kalna, K., & Garcia-Loureiro, A. J. (2018). Impact of cross-sectional shape on 10-nm gate length InGaAs FinFET performance and variability. *IEEE Transactions on Electron Devices*, *65*(2), 456-462.

Shahidi, G. G., Antoniadis, D. A., & Smith, H. I. (1988). Electron velocity overshoot at room and liquid nitrogen temperatures in silicon inversion layers. *IEEE electron device letters*, *9*(2), 94-96.

Sharma, R. K., Antonopoulos, A., Mavredakis, N., & Bucher, M. (2013, March). Impact of design engineering on RF linearity and noise performance of nanoscale DG SOI MOSFETs. In *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)* (pp. 145-148). IEEE.

Sharma, R. K., Gupta, M., & Gupta, R. S. (2011). TCAD assessment of device design technologies for enhanced performance of nanoscale DG MOSFET. *IEEE Transactions on Electron Devices*, *58*(9), 2936-2943.

Sharma, R. K., Gupta, R., Gupta, M., & Gupta, R. S. (2009). Dual-material double-gate SOI n-MOSFET: gate misalignment analysis. *IEEE transactions on electron devices*, *56*(6), 1284-1291.

Shockley, W. (1949). The Theory of p- n Junctions in Semiconductors and p- n Junction Transistors. *Bell System Technical Journal*, *28*(3), 435-489.

Shockley, W., Sparks, M., & Teal, G. K. (1951). p− n Junction Transistors. *Physical Review*, *83*(1), 151.

Song, J., Yu, B., Yuan, Y., & Taur, Y. (2009). A review on compact modeling of multiple-gate MOSFETs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *56*(8), 1858-1869.

Srivastava, V. M., Yadav, K. S., & Singh, G. (2011). Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF switch. *Microelectronics Journal*, *42*(10), 1124-1135.

Stesmans, A., & Afanas' ev, V. V. (1998). Undetectability of the point defect as an interface state in thermal. *Journal of Physics: Condensed Matter*, *10*(1), L19.

Steven Pemberton., C. [Online] Available: https://homepages.cwi.nl/~steven/Talks/2016/01-08-internet/.

Streetman, B. G., & Banerjee, S. (2006). *Solid state electronic devices* (Vol. 10). Upper Saddle River: Pearson/Prentice Hall.

Suddapalli, S. R., & Nistala, B. R. (2021). The analog/RF performance of a strained-Si graded-channel dual-material double-gate MOSFET with interface charges. *Journal of Computational Electronics*, *20*(1), 492-502.

Suzuki, K., & Sugii, T. (1995). Analytical models for n/sup+/-p/sup+/double-gate SOI MOSFET's. *IEEE Transactions on Electron Devices*, *42*(11), 1940-1948.

Suzuki, K., Tanaka, T., Tosaka, Y., Horie, H., & Sugii, T. (1995). High-speed and low-power n+-p+ double-gate SOI CMOS. *IEICE transactions on electronics*, *78*(4), 360-367.

Suzuki, K., Tosaka, Y., & Sugii, T. (1996). Analytical threshold voltage model for short channel double-gate SOI MOSFETs. *IEEE Transactions on Electron Devices*, *43*(7), 1166-1168.

Takeda, E. (1984). Hot-carrier effects in submicrometre MOS VLSIs. *IEE Proceedings I-Solid-State and Electron Devices*, *131*(5), 153-162.

Tanaka, T., Horie, H., Ando, S., & Hijiya, S. (1991, December). Analysis of p/sup+/poly Si double-gate thin-film SOI MOSFETs. In *International Electron Devices Meeting 1991 [Technical Digest]* (pp. 683-686). IEEE.

Tang, S., Wallace, R. M., Seabaugh, A., & King-Smith, D. (1998). Evaluating the minimum thickness of gate oxide on silicon using first-principles method. *Applied Surface Science*, *135*(1-4), 137-142.

Taur, Y., & Ning, T. H. (2021). *Fundamentals of modern VLSI devices*. Cambridge university press.

Taur, Y., Liang, X., Wang, W., & Lu, H. (2004). A continuous, analytic drain-current model for DG MOSFETs. *IEEE Electron Device Letters*, *25*(2), 107-109.

Terrill, K. W., Hu, C., & Ko, P. K. (1984). An analytical model for the channel electric field in MOSFET's with graded-drain structures. *IEEE Electron Device Letters*, *5*(11), 440-442.

Tosaka, Y., Suzuki, K., & Sugii, T. (1994). Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET's. *IEEE electron device letters*, *15*(11), 466-468.

Tsividis, Y. (1987). *Operation and Modeling of the MOS Transistor*. McGraw-Hill, Inc.

Tsormpatzoglou, A., Dimitriadis, C. A., Clerc, R., Pananakakis, G., & Ghibaudo, G. (2008). Threshold voltage model for short-channel undoped symmetrical double-gate MOSFETs. *IEEE Transactions on Electron Devices*, *55*(9), 2512-2516.

Tsormpatzoglou, A., Dimitriadis, C. A., Clerc, R., Pananakakis, G., & Ghibaudo, G. (2008). Semi- analytical modelling of short channel effects in Si double gate, tri- gate and gate all- around MOSFETs. *physica status solidi c*, *5*(12), 3605-3608.

Tsormpatzoglou, A., Dimitriadis, C. A., Clerc, R., Rafhay, Q., Pananakakis, G., & Ghibaudo, G. (2007). Semi-analytical modeling of short-channel effects in Si

and Ge symmetrical double-gate MOSFETs. *IEEE Transactions on Electron devices*, *54*(8), 1943-1952.

Vadthiya, N., Tripathi, S., & Naik, R. (2018). A two-dimensional (2D) analytical modeling and improved Short Channel performance of Graded-Channel gate-stack (GCGS) dual-material double-gate (DMDG) MOSFET. *Silicon*, *10*(6), 2399-2407.

Venkatesan, S., Neudeck, G. W., & Pierret, R. F. (1992). Dual-gate operation and volume inversion in n-channel SOI MOSFET's. *IEEE electron device letters*, *13*(1), 44-46.

Wanlass, F. M. (1967). *U.S. Patent No. 3,356,858*. Washington, DC: U.S. Patent and Trademark Office.

Wanlass, F. M., & Sah, C. T. (1991). Nanowatt logic using field-effect metal-oxide semiconductor triodes. In *Semiconductor devices: pioneering papers* (pp. 637-638).

Widiez, J., Lolivier, J., Vinet, M., Poiroux, T., Previtali, B., Daugé, F., & Deleonibus, S. (2005). Experimental evaluation of gate architecture influence on DG SOI MOSFETs performance. *IEEE Transactions on Electron Devices*, *52*(8), 1772-1779.

Wikipedia [Online] Available: https://en.m.wikipedia.org/wiki/CMOS

Wikipedia. [Online] Available: https://en.wikipedia.org/wiki/MOSFET

Wu, H., Zhao, Y. S., & White, M. H. (2006). Quantum mechanical modeling of MOSFET gate leakage for high-k gate dielectrics. *Solid-state electronics*, *50*(6), 1164-1169.

Wu, Y. H., Yang, M. Y., Chin, A., Chen, W. J., & Kwei, C. M. (2000). Electrical characteristics of high quality La 2 O 3 gate dielectric with equivalent oxide thickness of 5/spl Aring. *IEEE Electron Device Letters*, *21*(7), 341-343.

Yang, M., Chan, V. W., Chan, K. K., Shi, L., Fried, D. M., Stathis, J. H., & Leong, M. (2006). Hybrid-orientation technology (HOT): Opportunities and challenges. *IEEE Transactions on Electron Devices*, *53*(5), 965-978.

Yeo, Y. C., King, T. J., & Hu, C. (2003). MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations. *IEEE Transactions on Electron Devices*, *50*(4), 1027-1035.

Young, K. K. (1989). Short-channel effect in fully depleted SOI MOSFETs. *IEEE Transactions on Electron Devices*, *36*(2), 399-402.

Yu, B., Lu, H., Liu, M., & Taur, Y. (2007). Explicit continuous models for double-gate and surrounding-gate MOSFETs. *IEEE Transactions on Electron Devices*, *54*(10), 2715-2722.

Zeitzoff, P. M., & Chung, J. E. (2005). A perspective from the 2003 ITRS: MOSFET scaling trends, challenges, and potential solutions. *IEEE circuits and devices magazine*, *21*(1), 4-15.

Zeitzoff, P. M., & Huff, H. R. (2005, September). MOSFET scaling trends, challenges, and key associated metrology issues through the end of the roadmap. In *AIP Conference Proceedings* (Vol. 788, No. 1, pp. 203-213). American Institute of Physics.

Zhou, X. (2000). Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFETs) with gate-material engineering. *IEEE Transactions on Electron Devices*, *47*(1), 113-120.

List of Publications

Journal Publications:

1. H. Chakrabarti, R. Maity and N. P. Maity, "Analysis of surface potential for Dual-Material-Double-Gate MOSFET based on modelling and simulation," *Microsystem Technologies*, vol. 25, no. 12, pp. 4675-4684, 2019. DOI: 10.1007/s00542-019-04386-3.
2. H. Chakrabarti, R. Maity, S. Baishya and N. P. Maity, "An Accurate Model for Threshold Voltage Analysis of Dual Material Double Gate Metal Oxide Semiconductor Field Effect Transistor," *Silicon*, vol. 13, pp. 1851–1861, 2021. DOI: 10.1007/s12633-020-00553-8.
3. H. Chakrabarti, R. Maity, S. Baishya and N. P. Maity, "An Accurate Drain Current Model of Dual Material Double Gate Metal Oxide Semiconductor Field Effect Transistor," *Silicon*, pp. 1-9, 2021. DOI: 10.1007/s12633-021-01321-y.
4. H. Chakrabarti, R. Maity, T. Kevkić, V. Stojanović and N. P. Maity, "Analysis of Surface Potential and Electric Field for Fully Depleted Graded Channel Dual-Material-Double-Gate MOSFET through Modeling and Simulation," *Trans. Electr. Electron. Mater,* vol. 22, pp. 489–501, 2021. DOI: 10.1007/s42341-020-00256-2.
5. H. Chakrabarti, R. Maity, S. Baishya and N. P. Maity, "An Accurate Model of Threshold Voltage and Effect of High-k Material for Fully Depleted Graded Channel DMDG MOSFET," *Silicon*, pp. 1-10, 2021. DOI: 10.1007/s12633-021-01412-w.
6. H. Chakrabarti, R. Maity, A. Baidya, S. Baishya, N. P. Maity, "A Precise Drain Current Analysis of SiO_2/HfO_2 Based Graded Channel Dual Material Double Gate MOSFET," *Silicon*, Manuscript ID: SCON-D-22-00301, 2022.

Conference publications:

1. H. Chakrabarti, M. Lalruatfela, R. Maity and N. P. Maity, "An Analytical Model of Surface Potential for Dual-Material-Double-Gate Silicon-on-Insulator MOSFET," *International Conference on Energy Systems, Drives and Automations, Kolkata,* pp. 34-39, 2018.
2. H. Chakrabarti, R. Maity and N. P Maity, "Modeling and simulation of threshold voltage for dual material double gate metal oxide semiconductor field effect transistor" *2nd International Conference on 'Energy Systems, Drives and Automations', Kolkata*, pp. 22, 2019.

BIO-DATA OF THE CANDIDATE

Name of Candidate	:	Himeli Chakrabarti
Date of Birth	:	02/12/1982
Contact	:	8697475881 himle212@gmail.com
Permanent Address	:	R.B.I Employees' Housing Complex, Plot-D, Sreenagar Main Road, Garia, Kolkata-700094
Married	:	Yes
Educational Details	:	
(a) B. Tech	:	Electronics and Communication Engineering
(b) M.Tech	:	Materials Engineering
(c) Ph.D Course work	:	SGPA of 8.33.
Present Occupation Details	:	Assistant Professor
Organization	:	Regent Education and Research Foundation Group of Institution
Job Profile	:	Working as an Assistant Professor in the Department of Electronics and Communication Engineering (ECE) of Regent Education and Research Foundation Group of Institution, Kolkata

PARTICULARS OF THE CANDIDATE

Name of Candidate	:	Himeli Chakrabarti
Degree	:	Ph.D.
Department	:	Electronics and Communication Engineering
Title of Thesis	:	Modeling and Performance Analysis of Dual Material Double Gate Metal Oxide Semiconductor Field Effect Transistor
Date of Admission	:	27/07/2018
Approval of Research Proposal		
1. DRC	:	08-09/04/2019
2. BOS	:	23/04/2019
2. School Board	:	30/04/2019
MZU Regn No	:	1800282
Ph.D. Regn No	:	MZU/Ph.D./1287 of 27.07.2018
Extension	:	NO

_____

Dr. Niladri Pratap Maity
Head
Dept. of Electronics and Communication Engineering

ABSTRACT

MODELING AND PERFORMANCE ANALYSIS OF DUAL MATERIAL DOUBLE GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

THIS THESIS IS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

HIMELI CHAKRABARTI

MZU REGN NO : 1800282

PH.D REGN NO : MZU/PH.D./1287 of 27.07.2018

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SCHOOL OF ENGINEERING AND TECHNOLOGY

SEPTEMBER 2021

MODELING AND PERFORMANCE ANALYSIS OF DUAL MATERIAL DOUBLE GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

BY

HIMELI CHAKRABARTI
Department of Electronics and Communication Engineering

Name of Supervisor : Dr. Niladri Pratap Maity

Submitted

In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Electronics and Communication Engineering of Mizoram University, Aizawl

Introduction

Benefits of using MOSFETs have made them the standard in the electronics field. Simple device applications, low power consumption, high packing density, fast device speed and resistance to SCEs are only a few of them. MOSFET is a one-of-a-kind device having fast communication speed and efficiency when operating at low voltage. According to Moore's Law, the number of components in IC doubles every year. It means that the size of the components shrinks every two years so that they can fit into the compact gadget adequately. With the scaling down of the devices, some parameters like threshold voltage, channel length, film thickness and gate oxide thickness must be lowered. According to ITRS, next-generation MOSFET devices require oxide thickness in 1 nm range. It increases different SCEs like threshold voltage roll off, impact ionization, HCEs, GIDL together with DIBL effects. SCE creates an uncontrolled carrier movement in the channel region which enhances the motion of the current through the channel. This leaked current is not accounted with the current that is passing through the channel. The quantum mechanical tunnelling effect enhances with decreasing oxide thickness (below 1.2 nm), as a result, through the gate region huge amount of gate leakage current flows. The gate oxide material SiO_2 won't be able to perform to refrain the excess tunnelling current. This high current damages the device. It generates power loss, increases power dissipation and produces surplus heat.

Double gate (DG) idea has proven to be quite effective in suppressing SCEs. The channel is protected by the top and bottom double gates of this structure. As a result, the channel is completely surrounded by gates. The channel is inverted when the gate voltage is applied from both sides. The unregulated current flow through the channel is minimized as the gate voltage covers the channel. This type of design helps to reduce SCEs automatically. Another model for reducing SCEs is double material gate (DMG) architecture. Two types of work-functioned polysilicon are used at the gate in this construction. The potential profile of the surface region is changed in this architecture to increase electron transport efficiency. On the source side, a polysilicon material with a high work function is used, whereas on the drain side, a polysilicon material with a lower work function is used. Due to the presence of two distinct material gates, two

different values of surface potential and threshold voltage have been formed. With the increase of the electric field under the gate terminal the average lifetime of the device is increased for DMG structure. The step function profile which is generated in the surface potential and electric field due to use of different work functions polysilicon materials in two different gate section helps to reduce SCEs.

The DMDG SOI MOSFET structure is created by combining these two architectures. The advantages of the two structural concepts are combined in this construction. The electric field at the drain terminal end is lowered, but the drain breakdown voltage increases. Transconductance improves as a result, whereas drain conductance decreases. Another modified MOSFET structure with an asymmetrically doped channel is graded channel DMDG (GCDMDG). The doping concentration on the source side is higher than on the drain side. The GC structure has a high immunity to SCEs as a result of this type of doping, which helps to lessen HCEs and impact ionization. A high doping channel near the source side reduces DIBL, whereas a low doping channel near the drain side promotes mobility and lowers the electric field's peak value. Apart from these advantages, the GC design generates a greater driving current and increases transconductance when compared to other uniformly doped devices.

According to recent study, it has been proved that with the use of high-k dielectric materials (such as HfO_2, ZrO_2, Ta_2O_5) as a gate oxide material instead of SiO_2, the gate tunneling current, the leakage power reduces drastically and delivers astounding performance and greater energy efficiency.

Objectives

Two threshold voltages have been established for DMDG and GCDMDG structure due to differences in gate materials. Leakage current coverage has been enhanced by using two threshold voltages. It is the most crucial feature of a device's functionality. The threshold voltage in the DMDG and GCDMDG structures has the lowest roll off factor among all other planar structure. The generated step function-like characteristics in the surface potential and electric field over the channel help to

increase drain potential variation and drain conductance while decreasing SCEs, with DIBL.

The highest value of the electric field distribution helps to generate uniformly expanded drift velocity of the electron along the channel so that it can minimize the HCEs which is a major problem of general MOSFET. The step potential will increase with the influence of temperature, interface charge effect, etc. All of the above characteristics is improved by using HfO_2.

- To generate the analytical model of surface potential, the 2D Poisson's equation for DMDG MOS transistor has to be solved with the help of six boundary conditions.
- To evaluate the threshold voltage, electric field, drain current and other parameters, the proposed surface potential model has been considered.
- To analyze the performance of ultrathin DMDG MOS transistor using high-k material.
- To validate the proposed analytical model with TCAD simulation results

Summary

The DMDG and GCDMDG structure has been compared on basis of some specific performance analysis like surface potential, electric field, threshold voltage and drain current. The device performance also being analyzed with HfO_2 oxide material.

In the Chapter 1, different varieties of MOSFET have been explained in order to familiarise with MOSFETs. A brief overview of the many types of SCEs is also provided. On the subject of lowering SCEs, a few notes on DMDG and GCDMDG have been discussed.

In the Chapter 2, a review of DMDG and GCDMDG MOSFET are elaborated, with high-k material used as the gate oxide material in both mechanisms. Various sorts of MOSFET parameters are described, and the study effort is based on them. The high-k material HfO_2 is discussed briefly.

In the Chapter 3, the surface potential of DMDG structure has been generated using SiO_2 as well as HfO_2. All the analytical result are also established with simulation result. The generated step like surface potential for high-k material is found to be lower than SiO_2. The oxide material thickness can be increased in high-k materials to achieve a comparable level of surface potential. It will help to overcome the current tunnelling problem to some extent. The presence of HfO_2 causes an increase in oxide thickness in order to maintain the surface potential and drain current. By modifying the substrate doping concentration, temperature, and gate-source voltage, the surface potential can be increased for the minimal oxide thickness. Adjusting the device gate length also gives better results. As a result, it can be stated that combining a DMDG structure with a high-k dielectric material as dielectric material eliminates all scaling-down issues.

In the Chapter 4, the GCDMDG structure is studied on the basis of surface potential and compared with DMDG and SMDG structures. The GCDMDG structure has a greater potential profile than DMDG. Although it decreases due to the use of high-k, it remains greater than a DMDG equivalent. It exhibits a two-lobed step function potential profile, similar to DMDG. At different temperatures, the surface potential of the GCDMDG structure can be increased for the minimal thickness value of the oxide level. On the other hand, the electric field over the DMDG structure is unaltered. In terms of short channel immunity, gate controllability, carrier transportability, and hot carrier movements, the GCDMDG structure surpasses DMDG. Among DMDG, SMDG, and GCDMDG structures, the GCDMDG structure has the biggest source-channel potential barrier (i.e., large threshold voltage).

In the Chapter 5, the threshold voltages of DMDG and GCDMDG structures have been considered. The threshold voltage in DMDG device construction is quite low, however, it shows a rolling off tendency at a small scale channel dimension. This will increase the current in the short channel. High-k materials can reduce this problem. GCDMDG structure, on the other hand, has a larger threshold voltage than DMDG structure, but it does not exhibit the rolling off nature with small scale device dimensions. The threshold voltage is almost constant in this circumstance. The output is more accurate while using high-k material.

In the Chapter 6, drain currents of the structures have been illustrated. The evenly doped DMDG structure is more prone to increase SCEs since its threshold voltage is lower. It has the ability to increase the flow of unwanted current. Lowering the threshold voltage results in increased drain current and improved voltage gain. A higher amplification factor improves the device's performance. A graded channel doping structure, on the other hand, has a larger threshold voltage. As a result, it is more resistant to unwanted current and SCEs flowing through it.

In the Chapter 7, the general conclusion has been reached based on the research findings.