MODELING, SIMULATION AND PERFORMANCE ANALYSIS OF FINFET

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MODELING, SIMULATION AND PERFORMANCE ANALYSIS OF FINFET

BY

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Submitted

In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Electronics & Communication Engineering of Mizoram University, Aizawl

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CERTIFICATE

This is to certify that the thesis entitled **"Modeling, Simulation and Performance Analysis of FinFET"** submitted to Mizoram University for the award of the degree of **Doctor of Philosophy** in **Electronics and Communication Engineering** by **Suparna Panchanan**, Ph.D. Registration No. **MZU/Ph.D./1682 of 24.07.2019**, is Ph.D. scholar in the Department of Electronics and Communication, under my guidance and supervision and has not been previously submitted for the award of any degree in any Indian or foreign University. She has fulfilled all criteria prescribed by the UGC (Minimum Standard and Procedure governing Ph.D. Regulations). She has fulfilled the mandatory publication (Publication enclosed) and completed Ph.D. course work. It is also certified that the scholar has been admitted in the Department through an entrance test, followed by an interview as per UGC Regulation of 2016.

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DECLARATION

I, **Suparna Panchanan**, hereby declare that the subject matter of this thesis entitled "**Modeling, Simulation and Performance Analysis of FinFET**" is the record of work done by me, that the contents of this thesis did not form basis of the award of any previous degree to me or to do the best of my knowledge to anybody else, and that the thesis has not been submitted by me for any research degree in any other University/Institute.

This is being submitted to the Mizoram University for the degree of Doctor of Philosophy in **Electronics and Communication Engineering**.

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Abbreviation

#

2-D	Two Dimensional
3-D	Three Dimensional

A

ADSE	Asymmetric drain-spacer-extended
ASG	Asymmetric gate-work function

B

BSIM	Berkeley Short-Channel IGFET Model
BJT	Bipolar junction transistor
BOX	Buried oxide
BTI	Bias temperature instability

C

CAD	Computer-aided design
CD	Critical dimension
CGP	Contacted gate pitch
CLM	Channel length modulation
CMC	Compact Model Council
CMG	Common multi-gate
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
Cy-GAA	Cylindrical Gate-All-Around

D

DELTA	Depleted lean-channel transistor
DG	Double-gate
DIBL	Drain induced barrier lowering
DT	Direct tunnelling
DTCO	Design technology co-optimization

E

EGA	Extended gate area
EOT	Equivalent oxide thickness

F

FD	Fully depleted
Fe-FinFETs	Ferroelectric FinFET
FET	Field-effect transistor
FIBL	Fringing induced barrier lowering
FOM	Figures Of Merit

G

GAA	Gate-all-around
GIDL	Gate induced drain leakage
GS	Gate-stacked

H

HCI	Hot carrier injection
HK/MG	High-k/metal-gate
HP	High performance
HVM	High-volume manufacturing

I

IC	Integrated circuit
IFT	International Focus Team
IG	Independent-Gate
IGFET.	Insulated Gate Field Effect Transistors
IL	Interfacial-layer
IMG	Independent-multigate
IRDS	International Roadmap for Devices and Systems
ITRS	International Technology Roadmap for Semiconductors

L

LDD	Lightly Doped Drain
LER	Line-edge roughness
LOP	Low operating power
LSI	Large scale integration
LSTP	Low standby power

M

MAC	Multiply-accumulate
M-FinFET	Multiple fins constructed FinFET

MG	Multi-gate
MIGFET	Multiple Independent Gate FET
MOSFET	Metal oxide semiconductor Field-Effect Transistor

N

NBTI	Negative bias temperature instability
NC-FinFET	Negative capacitance FinFET
NMOS	n-channel metal-oxide semiconductor

P

PBTI	Positive bias temperature instability
PD	Partially depleted
PMOS	P-channel metal-oxide semiconductor
PPAC	Power, performance, area, and cost

Q

QFinFET	Quantum FinFET
QG	Quadruple-gate
QM	Quantum mechanical
QME	Quantum mechanical effect

R

RCS	Remote coulomb scattering
RDF	Resist-defined fin
RE-FinFET	Rectangular FinFET
RE-GAA	Rectangular Gate-All-Around
RFID	Radio-frequency identification
RGG	Ratio of average grain size to gate area
RPS	Remote phonon scattering
RTA	Rapid thermal annealing

S

SCE	Short channel effect
SDF	Spacer-defined fin
SG	Shorted-Gate
SHS	Symmetric high-k spacer
SOI	Silicon On Insulator
SR	Surrounding gate
SRAM	Static random access memory

T

TCAD	Technology computer-aided design
TDDB	Time-dependent dielectric breakdown
TG	Triple-gate
TGF	Transconductance generation factor
TI-FinFET	Triangular FinFET
TMD ML	Transitional metal dichalcogenide monolayer
TZ-FinFET	Trapezoidal FinFET

U

ULSI	Ultra-scale integration
UTB	Ultra-thin body
UTBB	Ultra-thin body and box

V

VLSI	Very-large-scale integration

W

WFV	Work function variation

Symbols

Symbol	Parameter Name
v_{sub}	Back gate potential
N_A	Body doping concentration of acceptor atom
K	Boltzmann constant
v_{bi}	Build-in potential
L	Channel length
k	Dielectric constant
Q_d	Drain charge
I_d	Drain current
v_{dsat}	Drain saturation voltage
v_d	Drain voltage
L_{eff}	Effective channel length
V_{def}	Effective drain voltage
W_{eff}	Effective fin width
μ_{eff}	Effective mobility
λ_{eff}	Effective natural length
ε_0	Electric permittivity of free space
v_q	Electron quasi-fermi potential
q	Electronic charge
H_{fin}	Fin height
W_{fin}	Fin width
v_{fb}	Flat band voltage

Symbol	Parameter Name
m_0	Free electron mass
Q_g	Gate charge
t_{ox}	Gate oxide thickness
v_{gs}	Gate to source voltage
v_g	Gate voltage
n_i	Intrinsic carrier concentration
Q_{inv}	Inversion sheet charge density
m^*	Isotropic effective mass of the electron
μ	Mobility of charge
λ	Natural length
λ_{asym}	Natural length of asymmetric DG-FinFET
λ_{sym}	Natural length of symmetric DG-FinFET
q_{ip}	Normalised sheet charge density
g_d	Output/drain conductance
C_{ox}	Oxide capacitance per unit area
ε_{ox}	Permittivity of dielectric medium / insulator
ε_{si}	Permittivity of silicon
v_{sat}	Saturation velocity
Q_{ip}	Sheet charge density
t_{oxb}	Silicon dioxide thickness
Q_s	Source charge
v_s	Source voltage
N_D	Source/ Drain doping concentration of donor atom
η	Subthreshold swing coefficient
Φ	Surface potential
v_{th}	Thermal voltage
Q_{th}	Threshold charge density

Symbol	Parameter Name
V_T	Threshold voltage
ΔV_T	Threshold voltage roll-off
g_m	Transconductance
ϕ_{ms}	Work function difference of metal-semiconductor
SS	Subthreshold swing

CHAPTER - 1

Introduction

1.1. Background

The electronic era of semiconductors was steered by the discovery of the bipolar junction transistor (BJT) in 1948 by Bardeen, Brattain, and Shockley at the Bell Telephone Laboratories (Ross, 1998). It was accelerated by creating an integrated circuit (IC) in 1958 by Jack Kilby in Texas Instruments (Ross, 1998). Being lightweight and small, ICs are widely used in different electronic components, viz., microprocessors, memory devices, radar etc., so that the dimension of the electronic system is reduced to a few square centimetres. The development of IC technology matures large-scale integration (LSI), very-large-scale integration (VLSI), and ultra-scale integration (ULSI). With this advancement of IC technology, semiconductor devices are now an integral part of our day-to-day lives.

Initially, the number of transistors increases exponentially with time. In 1965, Gordon Moore first noticed and forecasted that the amount of transistors fabricated within an IC increases twice every two consecutive years (Moore, 1975). The aforesaid emerging movement acknowledged as Moore's law became a golden rule of the semiconductor industry. The law is demonstrated in Fig.1.1 with the help of the Intel chronological processors. Here, the number of transistors in the successive processors is plotted against time (Dubash, 2005; Markoff, 2005).

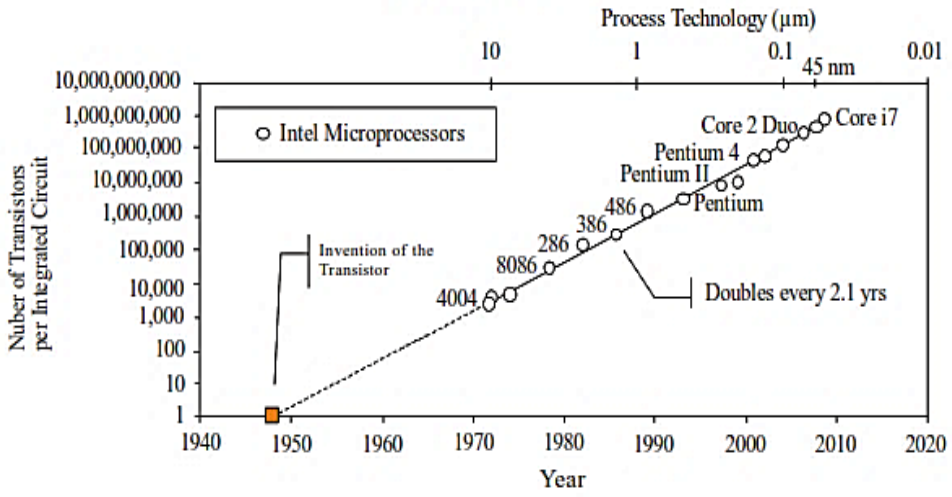


Fig.1.1: Road Map for Moore's Law (Moore, 1975)

The notion of scaling is to scale up the doping concentration and scale down device voltages and sizes using the same factor. Table 1.1 shows the scaling guidelines in tabular format.

Table 1.1: Scaling Rules (Dennard et al., 1974)

Physical Parameters	Consistent electric Field scaling factor	General scaling factors	General selective scaling factors
Insulator thickness, Channel length	$1/\alpha_O$	$1/\alpha_O$	$1/\alpha_O$
Wiring width, channel width	$1/\alpha_O$	$1/\alpha_O$	$1/\alpha_{O\_w}$
Electric Field in device	1	ε	E
Voltage	$1/\alpha_O$	ε/α_O	ε/α_{O_d}
On-current per device	$1/\alpha_O$	ε/α_O	ε/α_{O_w}
Doping	A	$\varepsilon\alpha_O$	$\varepsilon\alpha_{O\_d}$
Area	$1/\alpha_O^2$	$1/\alpha_O^2$	$1/\alpha_{O\_w}^2$
Capacitance	$1/\alpha_O$	$1/\alpha_O$	$1/\alpha_{O\_w}$
Gate delay	$1/\alpha_O$	$1/\alpha_O$	$1/\alpha_{O\_d}$
Power dissipation	$1/\alpha_O^2$	ε^2/α_O^2	$\varepsilon^2/\alpha_{O\_w}\alpha_{O\_d}$
Power density	1	ε^2	$\varepsilon^2\cdot\alpha_{O\_w}/\alpha_{O\_d}$

These principles merely give us instructions to compress a device (Dennard et al., 1974). However, they do not say how small the gadgets can be produced. According to (Dennard et al., 1974), α_0 is the scaling parameter of dimension, ε is the electric field scaling parameter, α_d indicates the gate length of the device and vertical dimension. Here, α_{0_w} relates to the width and wiring of the device.

To maintain power, performance, area, and cost (PPAC) scaling for mobility (μ), big data, and cloud (e.g., IOT and server) implementation, the More Moore International Focus Team (IFT) of the International Roadmap for Devices and Systems (IRDS) specifies the electrical, physical, and reliability requirements for logic and memory technologies. This has been done for mainstream/high-volume manufacturing (HVM) over 15 years.

Semiconductor device manufacturing is dedicated mainly to digital logic, which must offer two types of devices: 1) high-performance logic and 2) densely packed low-power logic; speed, power, density, and affordability are all important considerations for this technology platform. The More Moore idea lays out a strategy for metal oxide semiconductor field-effect transistor (MOSFET) miniaturisation to sustain historical patterns of improving device performance at lower power and cost.

Initially, the BJT fabrication was hindered due to uneven surface passivation of the semiconductor. To solve this problem, Kahng, D and his team found a new device, field-effect transistor (FET) (Kahng, 1960). A few years later, in 1963, the idea of MOSFET was developed by Hofstein, S. R., & Heiman, F. P. (Hofstein & Heiman, 1963). Wanlass, F. M., & Sah, C. T. proposed a complementary metal-oxide-semiconductor (CMOS) circuit in the same year (Wanlass & Sah, 1991). Since that time, CMOS has seized control of the semiconductor market. The cross-sectional structure of MOSFET and CMOS is given in Fig.1.2 and Fig.1.3, respectively.

In 1980, the sub-micron dimension boundary was overcome. At the end of the '90s, an excellent improvement in device performance was achieved by using a new substrate, silicon on insulator (SOI). The SOI MOS construction is given in Fig.1.4.

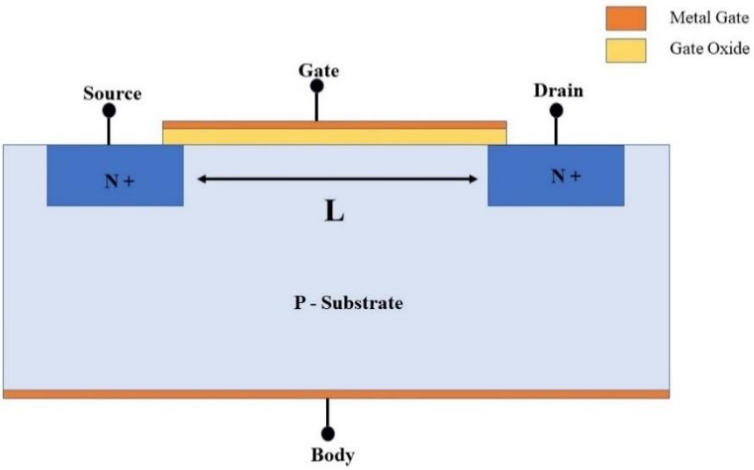


Fig.1.2: Cross-sectional structure of MOSFET (D. Das, 2015)

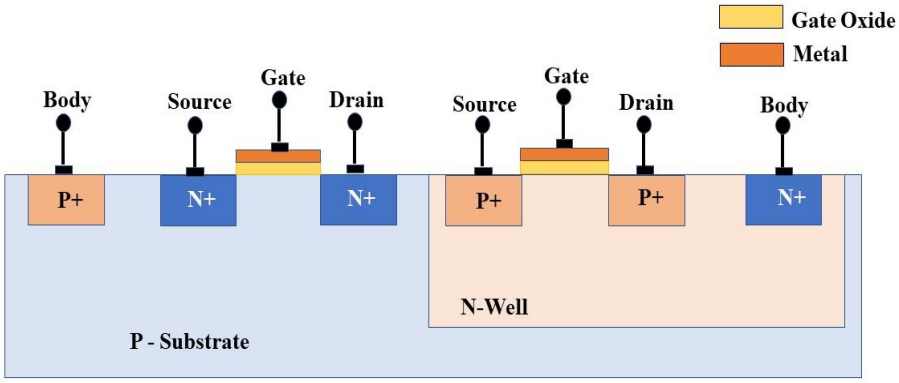


Fig.1.3: Cross-sectional structure of CMOS (Chattopadhyay, 2006)

The top silicon film is a high-quality single-crystal appropriate for a high packing density, high-performance circuit. The buried oxide (BOX) beneath the single-crystal reduces capacitance to the Si layer, i.e., base wafer or supporting substrate. The BOX layer also provides better isolation, low leakage current and most importantly reduces the short channel effects (SCEs). SOI MOSFET operates in either partially depleted (PD) or fully depleted (FD) modes. In FD-SOI mode, the thin silicon layer acting as a channel which is depleted of the majority carriers. On the other hand, PD-SOI transistors are fabricated on reasonably thick silicon layers, higher than the depletion width. The PD-SOI MOSFET's kink effect or floating body effect causes

higher current consumption. The small subthreshold swing (SS) (Berger et al., 1999), high speed and reduced power consumption make the FD device more popular than the PD device. It is also free from the kink effect (Cristoloveanu & Li, 1995). Different dielectric materials and base wafers are also reported to produce other varieties of SOI structures.

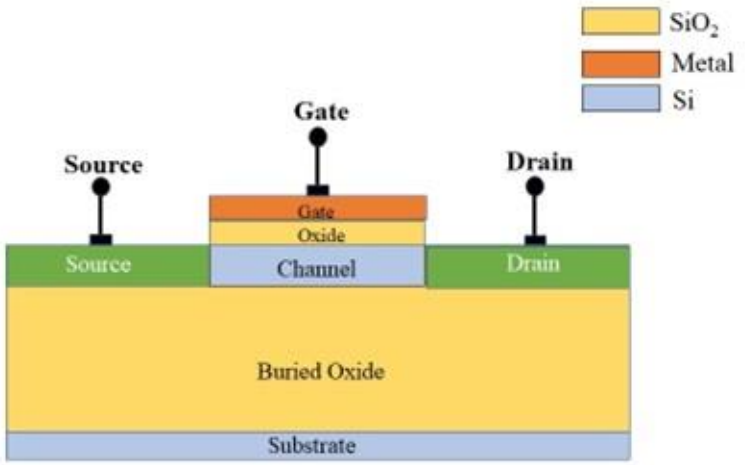


Fig.1.4: Cross-sectional view of SOI MOSFET structure (D. Das, 2015)

1.2. Short Channel Effects

SCEs are the sequence of events associated with the miniaturisation of the device dimension. It includes velocity saturation (v_{sat}), drain induced barrier lowering (DIBL), threshold voltage roll-off (ΔV_T), mobility degradation, hot carrier effect and most importantly, high leakage current.

1.2.1 Velocity saturation and Mobility degradation

The longitudinal electric field is assumed to be significantly small in the long channel device. So, the carrier velocity is proportional to the field. But this assumption is not effective in short channel devices and the velocity saturates with the electric field, which is illustrated in Fig.1.5.

The effect on device characteristics due to the lack of proportionality between these two parameters is known as the velocity saturation effect. The short channel

device's drain current (I_d) depends on gate length rather than the gate voltage (v_g), it may saturate at lower voltage (J.-W. Han, C.-H. Lee, D. Park, & Y.-K. Choi, 2007; Hwang et al., 2009; H. Wong & Poon, 1997).

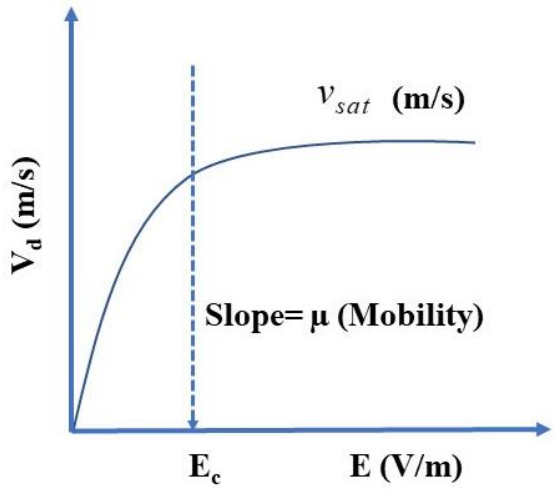


Fig.1.5: Representing velocity saturation (v_{sat}) ***(D. Das, 2015)***

The carrier movement in a particular direction is taking place in the semiconductors due to the presence of external bias. The velocity of the carriers is linearly proportionate to the applied electric field, commonly identified as μ. But this relation is ineffective at a high electric field and carriers' velocity gets saturated, as depicted in Fig.1.5. The collision of the charge carriers with the interface degrades the carriers' μ at the electric field in the range of 10^5 to 10^7 V/cm. The gradual channel approximation is invalid in the short channel device and increased vertical field results in carrier scattering adjacent to the surface. Therefore, μ degradation is a noticeable effect in a short channel device.

1.2.2 Drain induced barrier lowering

The field lines begin at the source and the drain ends at the channel if the width of space charge region of the drain and source is comparable to the length of the channel. Hence, with the increment of drain voltage (v_d), drain field penetrates

through the channel to the source, reducing the barrier drastically; consequently, v_d regulates the threshold voltage (V_T). This event is known as DIBL. The DIBL is shown in Fig.1.6. $E_c(y)$ indicates the conduction band energy and the channel is along the y-direction.

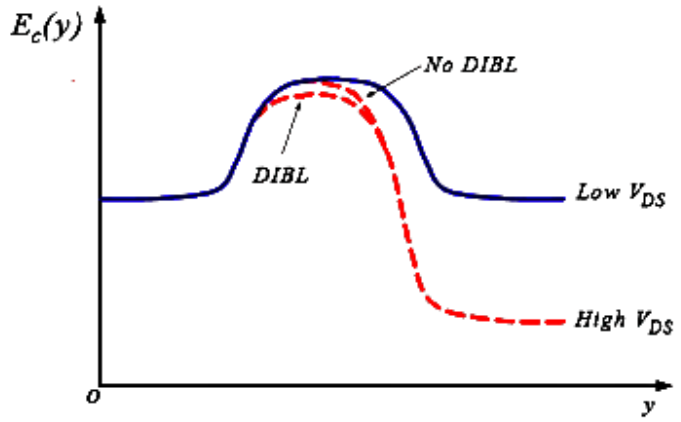


Fig.1.6: Bending of conduction due to DIBL (Yannis Tsividis, 1987)

1.2.3 Threshold voltage roll-off

Traditionally, V_T reduction with the diminution of the gate length is a renowned SCE called ΔV_T, which arises as a consequence of the restriction of gate control over the channel. Hence, I_d increases with the decrement of V_T. At $v_g = 0\,\text{V}$ i.e., in cut-off region, the $(v_{gs} - V_T)$ produces a small negative voltage, which produces a large leakage current and leakage power. Here, v_{gs} is the gate to source voltage. This effect will be further enhanced with an increment of v_d. ΔV_T is shown in Fig.1.7.

1.2.4 Channel length modulation

Instead of a parallel curve in the saturation zone, the short channel device generates drain characteristics curves with a positive slope. Hence, this is the indication of SCE and it is to be calculated and addressed as channel length modulation (CLM). As the device enters into the saturation, the inversion charge density reduces and the velocity of the charge carriers increases to support the current. At a certain v_d

, the carriers near the drain region attain a saturation velocity and carrier density reaches its minimum value. With the increment of v_d, the region mentioned above extends into the channel and is filled with acceptor atom concentration (N_A). Hence, the actual channel length (L) decreases with the increment of v_d. Hence, CLM is the term used to describe this type of channel modification with v_d. Fig.1.8 depicts the CLM.

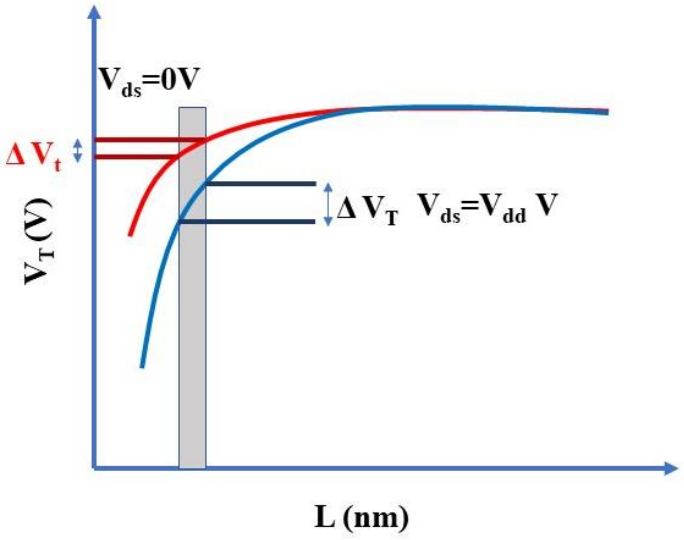


Fig.1.7: Representing ΔV_T (Sze, Li, & Ng, 2021)

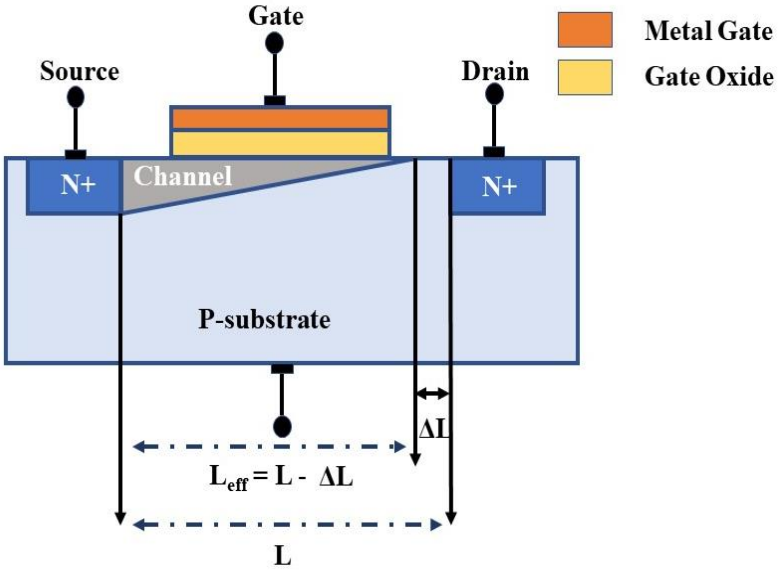


Fig.1.8: Block diagram representing channel length modulation

1.2.5 Punch through

The extreme case of CLM is punch through. In this condition, the space charge regions around the source and drain fuse all together and form a single depletion region. It causes rapid growth of I_d with the small increment of drain to source voltage. This event is visualised in Fig.1.9. It will increase the output/drain conductance (g_d) and limit the maximum operating voltage (Y Taur & Ning, 1998).

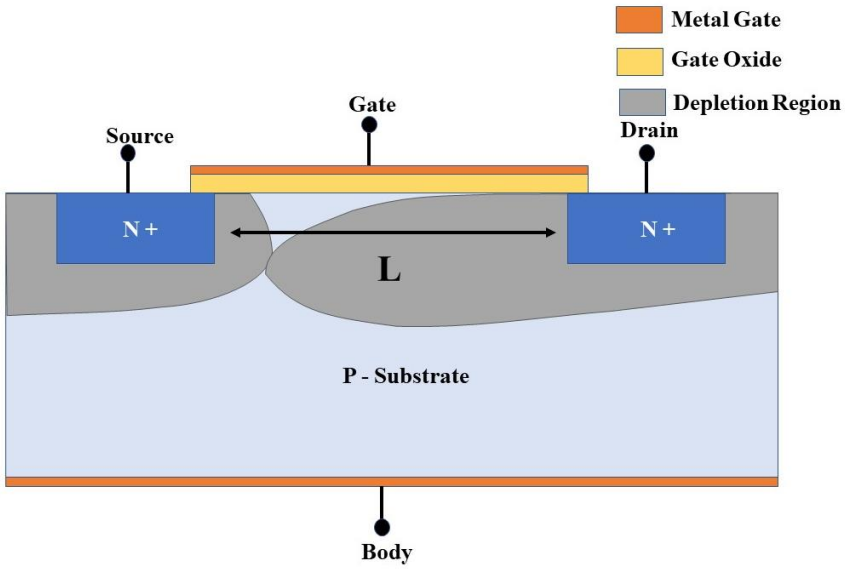


Fig.1.9: Schematic diagram of punch through (Yannis Tsividis, 1987)

1.2.6 Hot carrier effect

At reverse bias, the energetic electrons in the channel can tunnel the barrier and be trapped in the oxide layer. These trapped charges will modify the short channel device's V_T and I-V characteristics. This event is known as the hot carrier effect. This problem can be minimised in Lightly Doped Drain (LDD) structure, where most of the drain and source region is heavily doped and the region adjacent to the channel is lightly doped. Therefore, this structure reduces the field between drain and channel; as a result, the hot carrier effect diminishes. The hot electron effect is shown in Fig.1.10.

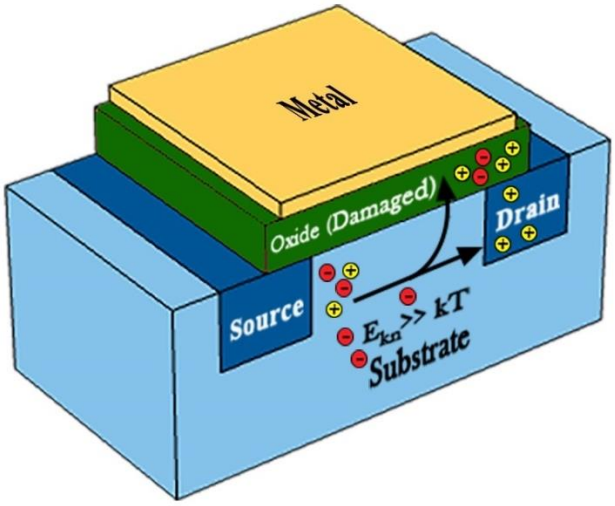


Fig.1.10: The hot electron effect (D'Agostino & Quercia, 2000)

1.2.7 Impact ionisation

Impact ionisation is the consequence of the hot electron effect. Many electron-hole pairs are produced by the impact ionisation of the energetic carriers with the Si atoms. The drain terminal collects the excess amount of electrons. But the holes retain in the body and produce substrate or body current, which is one of the important reasons for the power loss in a short channel device. It also affects the g_d and holding time of MOS memory device. Fig.1.11 explains the impact ionisation process.

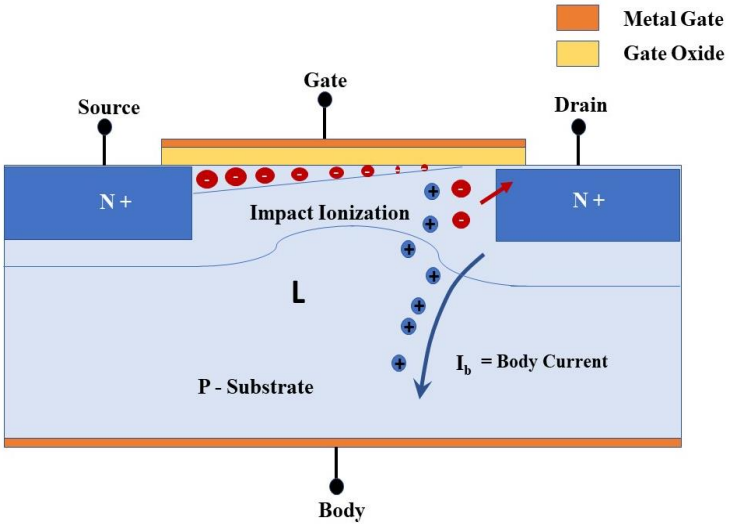


Fig.1.11: Schematic representation of the impact ionisation process (Bhattacharyya, 2009)

1.2.8 Subthreshold swing

SS that develops as a result of generated electrons in the channel prior to the strong inversion condition is the effect that is made worse by the short channel device. In this condition, these induced electrons diffuse from source to drain, making it hard to switch off the device below the threshold. The DIBL effect exacerbates the subthreshold current. The slope of log of I_d with v_{gs} is the measure of *SS* (Tosaka, Suzuki, & Sugii, 1994). It can be found out by differentiating v_{gs} with respect to $\log(I_d)$

$$SS = \frac{dv_{gs}}{d(\log I_d)} \tag{1.1}$$

A typical $\log(I_d)$ versus v_{gs} graph is shown in Fig.1.12. In-room temperature, *SS* is 60 mV/decade for the ideal transistor. It indicates that the subthreshold current is reduced by one-tenth with the reduction of $v_g = 60\,\text{mV}$.

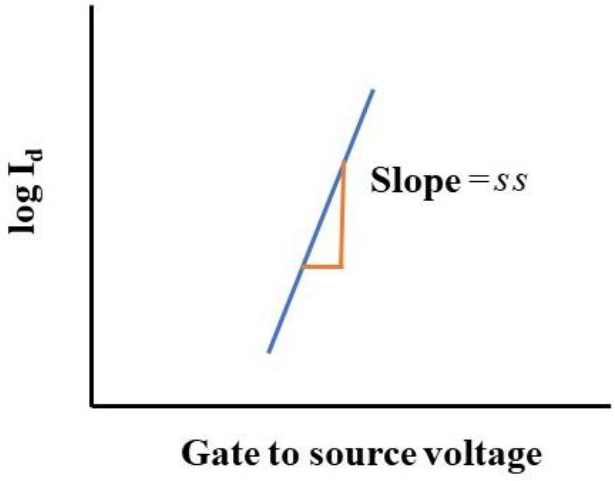


Fig.1.12: $\log I_d$ ***Vs*** v_{gs} ***curve (D. Das, 2015)***

1.2.9 Quantum mechanical effect

Quantum mechanical effect (QME) is very important in small geometry devices. As the carrier energy quantisation is triggered due to the structural

confinement, the energy gap widens and electrons will be in the first sub-band above the conduction band. This results in an increased V_T .

1.2.10 Gate induced drain leakage

Gate induced drain leakage (GIDL) current is materialised due to band-to-band tunnelling mechanism. When drain is linked to a positive bias and the gate is near to zero voltage or a negative voltage, the drain region below the gate is exhausted of free carriers and even it will be inverted under the action of a vertical electric field, as illustrated in Fig.1.13. As the drain is heavily doped, a narrow depletion region and a large electric field is created between the drain and gate. Due to these two-fold effects, electrons tunnel from the valence to the conduction band and are collected by the drain. This kind of leakage current also occurs due to trap assisted tunnelling under low electric field conditions. GIDL contributes significant power loss in a short channel device (Chan, Chen, Ko, & Hu, 1987; Semenov, Pradzynski, & Sachdev, 2002).

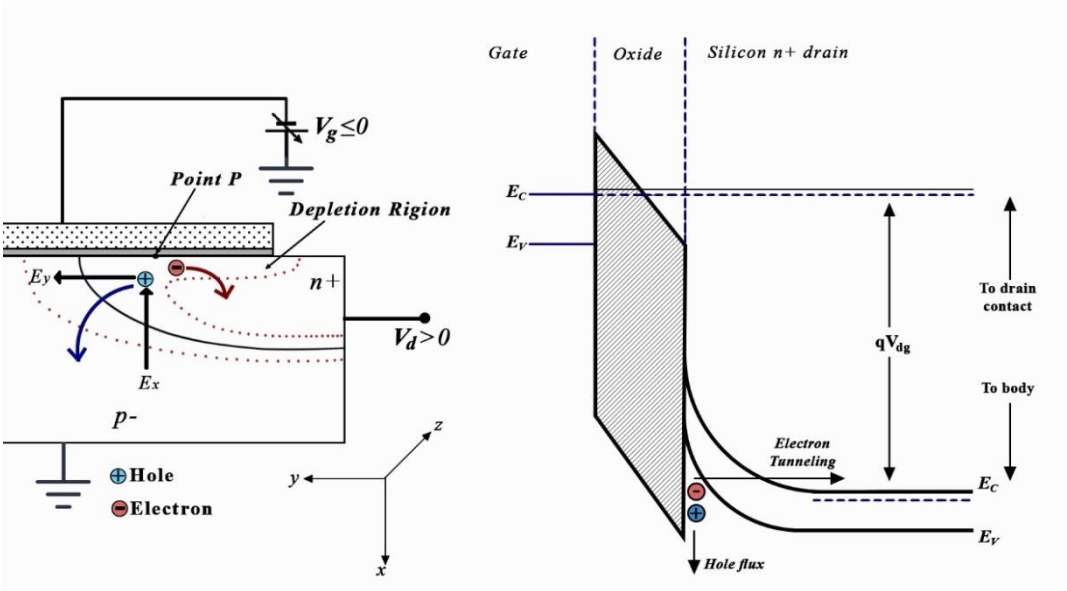


Fig.1.13: Graphical representation of GIDL (J.-H. Chen, Wong, & Wang, 2001)

1.2.11 Fringing induced barrier lowering

The gate leakage current can be reduced by replacing SiO_2 with high-k dielectrics. But the higher dielectric materials enhance the equivalent oxide thickness (EOT), which produces a fringing electric field from source to drain, deteriorating the

gate control over the channel. This incident is identified as fringe induced barrier lowering (FIBL) (Q. Chen, Wang, & Meindl, 2005; P. Liang, Jiang, & Song, 2008; X. Liu, Kang, Sun, Han, & Wang, 2002).

Fig.1.14 explains the FIBL. The physical distance is the distance measured from point X to the different electrodes. The drain electrode is linked with the channel through path I and path II. It is important to mention that path II coupling can be ignored in long channel devices owing to the small physical width of the gate oxide. But it plays an important role in short channel devices as it is governed by the dielectric gate thickness and the drain-side overlap area. The electrical equivalent distance of path I can be kept constant following the scaling rules. But, the distance between channel and drain decreases in the lateral direction due to improper scaling. Owing to the higher physical thickness of the high-k material, the lines of force decrease at the overlap regions, increasing the fringing effect (Mohapatra, Desai, & Rao, 2003). The increased fringing field is responsible for widening the depletion region beyond the gate in the width direction. Hence, more gate charge is required to create the inversion channel, resulting in enhancement of V_T .

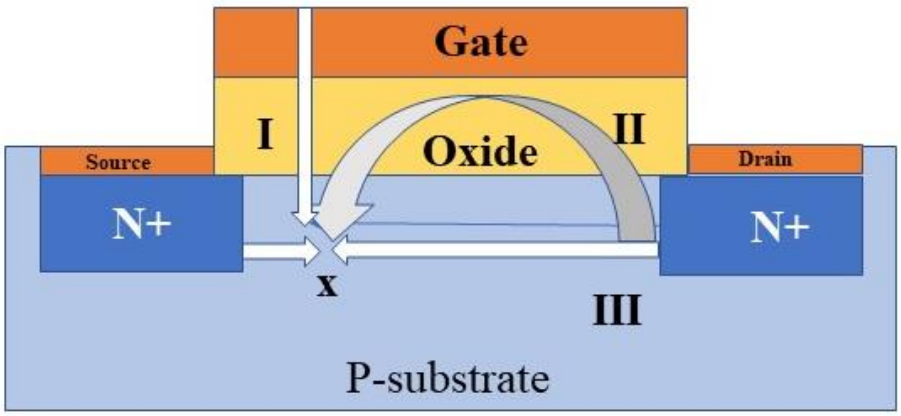


Fig.1.14: Schematic representation of FIBL (Mohapatra et al., 2003)

1.2.12 Parasitic BJT effect

The parasitic BJT effect is mainly visible in power MOSFET. In this type of device, the body act as a base. The source and the drain act as emitter and collector,

respectively. Normally, the body is shorted with the source to turn off the BJT otherwise, the potential at the body terminal may turn on the BJT and the device will enter into the latch up condition and may damage the device (Baliga, 1996).

1.2.13 Time-dependent dielectric breakdown

Due to the miniaturisation of the semiconductor device, the transverse electric field produces huge stress on the ultra-thin gate oxide. If this device operates under the high electric field for a long time, gate oxide will be degraded and may destroy the device. This phenomenon is known as time-dependent dielectric breakdown (TDDB).

1.3 Multi-gate MOSFET

Over the past decade, the SOI MOSFET matures from the single gate, planar structure to the multi-gate (MG) structure. While the research on it was started in early 60s (Baliga, 1996; Cobbold & Trofimenkoff, 1964, 1965). The SCEs are more prominent when L of CMOS goes down below 100 nm regime. Thermal injection and quantum mechanical (QM) tunnelling lead the device's electrical barriers to drop their insulating characteristics (Yuan Taur et al., 1997). These cause the rapid increase of the chip's standby power, limit the integration level and the switching speed. Therefore, scaling is no more an adequate solution. Processing modules, tools, material qualities, and other factors make scaling a challenging issue. The fabrication process encounters new challenges because of the requirement of new processing steps. Therefore, to address these challenges, it needs a device engineering revolution and a new concept of physics. Hence, the planar MOSFET is transformed into a three dimensional (3-D) MG structure.

The MG arrangement acts as an electrostatic buffer, shielding the channel region from the parasitic field generated by the gate and drain. The absence of transverse field improves μ. As L goes down, two or more inversion volumes are produced, resulting in a faster carrier movement and high drive current. In a MG structure, the channel is controlled by more than one gate; thereby, lower DIBL and a better SS can be achieved. The first fabricated double-gate (DG) SOI MOSFET, fully depleted lean-channel transistor (DELTA, 1989) was constructed on a thin, tall silicon island, generally known as a finger, leg or fin (Hisamoto, Kaga, Kawamoto, & Takeda,

1989). DG, triple-gate (TG) structure such as quantum wire (J.-P. Colinge, Baie, Bayot, & Grivei, 1996) , FinFET (Huang et al., 1999) and quadruple structure viz. gate-all-around (GAA) (J.-P. Colinge, Gao, Romano-Rodriguez, Maes, & Claeys, 1990), vertical pillar MOSFETs (C. P. Auth & Plummer, 1998), Pi-gate SOI MOSFETs (Park, Colinge, & Diaz, 2001) are few examples of MG structure. It is important to mention that a single gate probe is placed on opposite sides of the DG device. Following the same technique in TG structure, a single gate electrode is connected to the gate metal, which covers the device from three sides. The multiple independent gate FET (MIGFET) is a notable exception, as two separate gate electrodes are at two unlike potentials. It was reported that if L is below 30 nm, manufacturers must adopt the MG devices to catch up with the International Technology Roadmap for Semiconductors (ITRS) (Association, 2007). Not only the MG structure but vertical scaling is more efficient in the era of the 20^{th} century. It was reported that this device will be the most significant architecture that could sustain scaling until 2025 (C. Auth et al., 2017; Veloso et al., 2016; Yeap et al., 2019). The various MG structure is shown in Fig.1.15.

The improved controllability of SCEs and the healthy compatibility with the existing CMOS fabrication technique make the FinFET a potential alternative of CMOS. Generally, FinFET with superior scalability support, undoped or lightly doped channel reduces dopants' random fluctuation (Park & Colinge, 2002; V. Subramanian et al., 2007; S. Xiong & Bokor, 2003; Zhang, Fossum, Mathew, & Du, 2005). The vertical narrow channel which is controlled by more than one gate provides improved electrostatic integrity, that will reduce the scaling of fin body thickness compared to the ultra-thin body and box FD-SOI (UTBB FD-SOI) (Mitard et al., 2014; Xie et al., 2016). Fig.1.16 depicts the classification of FinFET in chart format.

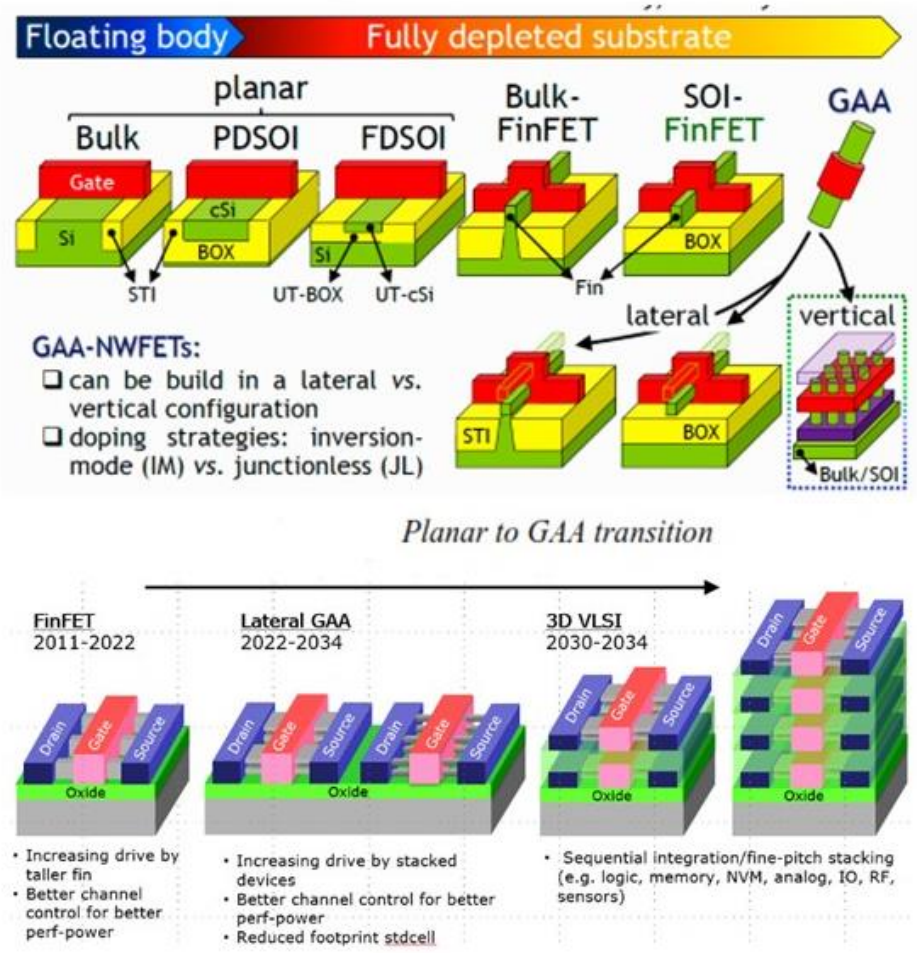


Fig.1.15: Scaling scenario for device architecture and development of device architecture in the IRDS Roadmap (IEEE, 2020)

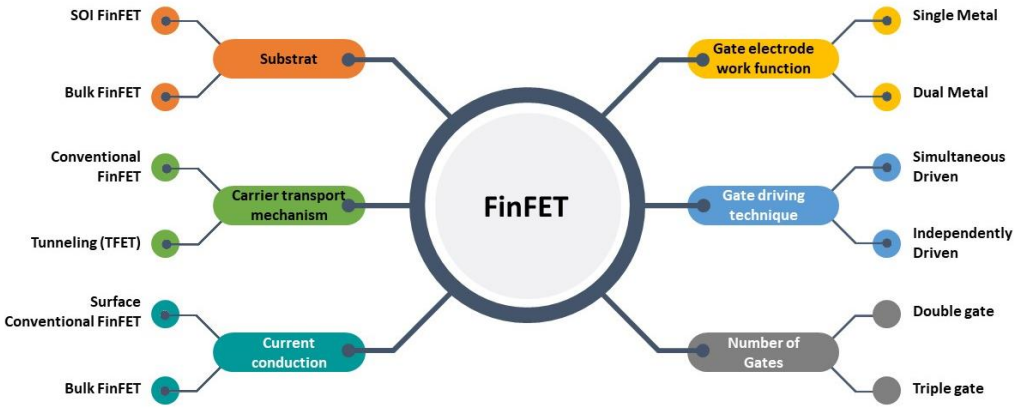


Fig.1.16: Classification of FinFET (Lakshmi, 2013)

1.4 Concept of FinFET

The ongoing increase in integration levels gave rise to FinFET technology. To achieve the enormous gains in integration levels, numerous parameters have been changed. Feature sizes have been decreased to manufacture of more devices in a given space. As process technologies reach 20 nm, it will become impossible to achieve the correct scaling of numerous device parameters since individual device scalability has limits. The supply voltage is the most important aspect in defining dynamic power and it is mainly affected by scaling. Optimising one variable, for example, performance, led to unintended trade-offs in other areas, such as power. As a result, additional options had to be considered. Hence, FinFET comes.

The term FinFET is a generic name. Generally, it denotes any fin-based, MG transistor architecture regardless of gate numbers. Profs. Chenming Hu, Tsu-Jae King-Liu, and Jeffrey Bokor of the University of California, Berkeley were the pioneers of this structure.

The FinFET is a 3-D structure. The vertical fin forms the channel. It also serves as the source and drain, allowing larger volumes in the same area as a standard planar transistor. Therefore, the height of the fin plays a vital role in creating the channel width. The gate is orientated at a right angle and warps the vertical fin. The gate can be viewed as a "multiple" gate surrounding the narrow channel. These MG might exhaust the channel of carriers completely and as a result, better electrostatic control of the channel and improved electrical characteristics can be achieved. The improved electrical characteristics mean the channel can be "choked off" more easily, i.e., near-ideal sub-threshold behaviour (related with leakage), which is intricated to attain in the planar technology. One most important feature that makes the transition easier from the planar structure to the vertical structure is that the back-end of the procedure is essentially identical for both, so most of the design flow related to the back-end remains the same.

In this research work, a short channel FinFET is considered and depicted in Fig.1.17. The thin fin-shaped silicon (Si) channel is considered on the silicon dioxide (SiO_2) with a thickness represented by t_{oxb}. The gate electrode surrounds the fin with the fin height $\left(H_{fin}\right)$, fin width $\left(W_{fin}\right)$ and L. The gate oxide thickness $\left(t_{ox}\right)$ is

uniform on the three sides of the fin. Thus, the construction forms a TG-FinFET structure.

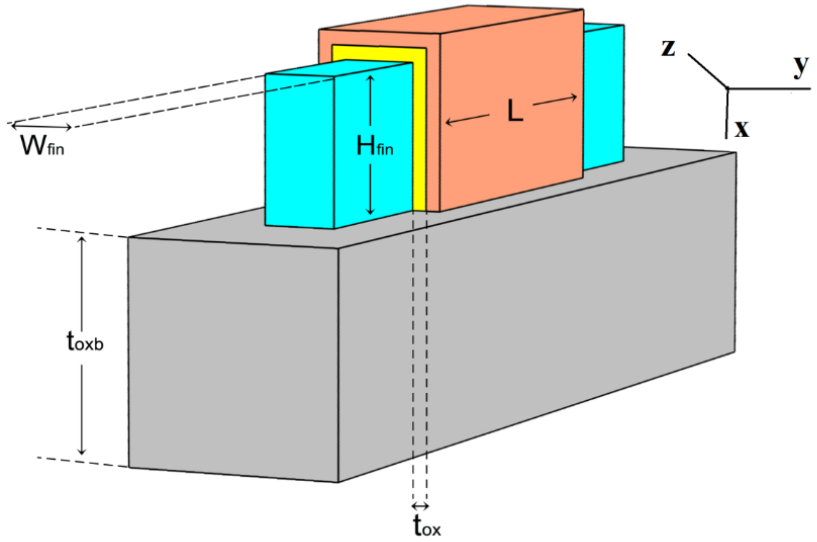


Fig.1.17: Schematic view of TG-FinFET

1.5 Need for High-k materials

With the advancement of semiconductor technology, the size of MOSFETs has been scaled down to sub-100 nm. However, the scalability of individual device parameters has its own limits. The SiO_2 layer with a thickness of 1.2 nm provides a direct tunnelling (DT) current through the gate terminal in the order of 1 A/cm^2 at 1 V. This leads to unacceptable static power dissipation and generates excess heat, which may vandalize the device (Gusev, Narayanan, & Frank, 2006; Ortiz-Conde et al., 2016). Likewise, the fabrication of such thin films is very tough and defective. Thus, SiO_2 had to be replaced.

Semiconductor device makers successfully implement the CMOS technology with high-k dielectric materials to reduce the device lengths to the extent of 45 nm and lower nodes (Kuhn et al., 2012). Transition metals from groups III-IV, lanthanides, and Al constitute a family of binary and ternary metal oxide insulators with a relative permittivity generally 9 refer to as high-k dielectric materials. The formula of relative dielectric constant, k, is given in equation (1.2), where ε_{ox} is dielectric permittivity of

the oxide or insulator and ε_0 is free space permittivity. Aluminum oxide (Al_2O_3), Hafnium oxide (HfO_2), Zirconium dioxide (ZrO_2) and Titanium dioxide (TiO_2) are examples of a few potential high-k dielectrics. k is dielectric constant.

$$k = \frac{\varepsilon_{ox}}{\varepsilon_0} \tag{1.2}$$

In FET the I_d depends on the gate-oxide capacitance per unit area (C_{ox}), which is simply represented as,

$$C_{ox} = \frac{\varepsilon_0 k}{t_{ox}}$$

$$\text{or, } C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{1.3}$$

Therefore, the same capacitance with larger t_{ox} can be achieved for the high-k dielectric. As the tunnelling current diminutions exponentially with increasing t_{ox}, the tunnelling problem is solved by replacing SiO_2 with a thicker high-k material layer.

The problem of gate leakage had been recognised since the late 1990s (S.-H. Lo, Buchanan, Taur, & Wang, 1997), but the measures of selecting the oxide were unidentified. Intel is now manufacturing chips with the second generation of high-k/metal stacks and has also integrated high-k for FinFET architectures. The criteria for choosing a good high-k dielectric material

- Its k value should be adequately high to economically support a fair number of scaling nodes.
- It must be thermodynamically stable, as it is near the Si channel.
- The band offsets with Si should be greater than 1 eV to reduce the carrier injection (Robertson, 2000). The band offset is shown in Fig.1.18.
- It should be kinetically stable.
- It should form a decent electrical interface with Si.
- It should contain less amount of electronic defects.

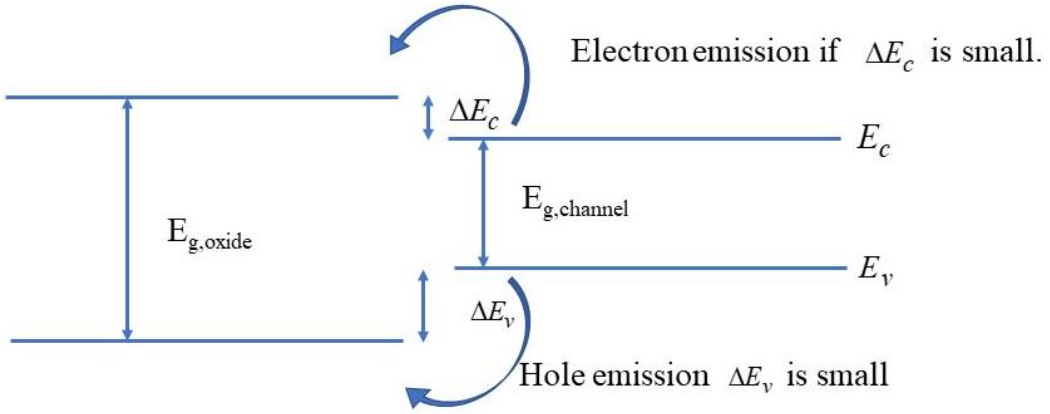


Fig.1.18: Band diagram showing the band offset (Persson, 2004)

Among the aforesaid parameters, the value of k and the offset energy are the most important criteria for choosing the high-k material. The value of k and the offset energy of a few high-k materials are given in table 1.2.

Table 1.2: Parameters of few high-k materials with respect to Si (Robertson, 2000; H.-S. P. Wong, 2005)

Material	k value	Bandgap (eV)	Conduction band offset (eV)	Leakage current reduction w.r.t SiO_2	Thermal stability w.r.t Si
SiO_2	3.9	1.11	3.2	NA	$>1050^0$C
ZrO_2	25	5.8	1.5	10^4-10^5	~900^0C
HfO_2	22	5.8	1.5	10^4-10^5	~950^0C
Al_2O_3	9	8.8	2.8	10^2-10^3	~1000^0C RTA
TiO_2	80	3.5	0	---	Not stable
La_2O_3	21	6	---	---	---

*RTA rapid thermal annealing

1.5.1 Why HfO_2?

Lanthanum oxide (La_2O_3) has a large k value, but it is hygroscopic. The low dielectric constant (k:8-13) of Al_2O_3 makes it a poor dielectric concerning Si though it has a high band gap (8.8 eV) and is electrically stable. Depending on the deposition process TiO_2 provides permittivity of 80-100, but it could not provide thermodynamical stability at Si interface (Hubbard & Schlom, 1996). It forms a reaction layer at the channel interface as well as on the metal electrodes.

Column IV has both Zr and Hf, which are extremely similar components. HfO_2 and ZrO_2 with large relative permittivity (20-25) have good stability on Si; enough band offsets to operate as a barrier for electrons and holes. These can resist annealing temperatures up to 900°C. But, later research revealed that ZrO_2 is somewhat more reactive with Si and can form silicide (Copel, Gribelyuk, & Gusev, 2000). As a result, HfO_2 is preferred to ZrO_2.

Hence from the above discussions, the motive for selecting HfO_2 as a high-k dielectric for this research work is summarised as

1) High dielectric constant of ~25-30

2) Despite of a lower bandgap than SiO_2, HfO_2 offers a more than 1ev band offset (1.5eV conduction band offset and 3.4eV valence band offset).

3) In comparison with other high-k dielectrics, the reaction energy around 47.6Kcal/mol at 727 °C makes it a most steady material on Si substrate.

4) Hf silicide, unlike other silicides, will be oxidised easily to create HfO_2.

5) MOS devices with HfO_2 gate dielectrics produced on Si substrate by conventional thermal evaporation do not cause much interface damage.

Therefore, the discussed characteristics of HfO_2 make it an attractive substitute for SiO_2.

1.6 Scope of the thesis

Before the 130 nm node, transistors benefited from Dennard scaling (Dennard et al., 2007). The gate length, width and the EOT of transistors were all scaled by a constant factor to improve latency at constant power density. Presently, there are a lot of verities of input parameters and hence, the output parameters depend on these input

parameters. According to IRDS (IRDS 2020), FinFET is still the most important device architecture for scaling till 2025 (IEEE, 2020). Electrostatics and fin depopulation i.e., raising H_{fin} while reducing the number of fins per unit footprint area, are the most practical ways to increase the proficiency of the device. As a result of tightening design regulations, parasitic improvement is projected to remain a primary pedal for performance enhancement. It is expected that these parasites will continue to be a dominant term in critical path performance. Nowadays, controlling source/drain series resistance within acceptable bounds will become a tough challenge. These smaller dimensions devices with high current density demand low resistance. Conferring to IRDS 2020 report the saturation current is degraded near about 40 % by the series resistance (IEEE, 2020). The parasitic capacitance and series resistance between gate and source/drain terminal also increase with technology scaling. This will put a limit on the increment of H_{fin}.Therefore, from the above discussion, it can be stated that FinFET will become a potential candidate for the recent semiconductor technology and it offers an enormous scope of the research area.

The device demands accurate modeling before application as modeling offers an insight into the operation of devices. On the other hand, simulation histrionically reduces the development costs and time-to-market.

This thesis concentrates on the characterisation of TG-FinFET scaled nanoscale dimensions. The main focus of this research work is to propose a powerful analytical model of surface potential (Φ), V_T, and I_d. The model is enriched by including QE in the V_T model, which would also reflect in other parameters. LambertW function is used to find I_d. The transconductance (g_m) and g_d are formulated from the current equation. The research work also deals with the SCEs such as ΔV_T, SS, DIBL, transconductance generation factor (TGF). The trans-capacitances at each node of the device are calculated using MATLAB. It offers a comparative study of the effect of the cross-sectional shape on the device on its performance. Most importantly, this work carefully considers Technology Computer-Aided Design (TCAD) model to validate the analytical model. V_T, I_d and SS have been compared with the published experimental results. According to the reported

study, at $L = 50\,\text{nm}$, $H_{fin} = 65\,\text{nm}$ and $W_{fin} = 25$ nm, the threshold voltage was 0.304 V and using the same parameters, this model provides 0.384 V (Tsormpatzoglou et al., 2011). A FinFET with $L = 910\,\text{nm}$, $H_{fin} = 65\,\text{nm}$, and $W_{fin} = 875\,\text{nm}$ produced a I_d of 10^{-7} A at $v_d = 1.02\,\text{V}$ and $v_g = 0.5\,\text{V}$ according to the study (Tsormpatzoglou, Dimitriadis, Mouis, Ghibaudo, & Collaert, 2009). This study offers I_d in the order of 200 nA while maintaining the parameters constant. For 50 nm channel, *SS* was approximately 81 mV/decade whereas using this model it is 86.687 mV/decade (Ritzenthaler, Lime, Faynot, Cristoloveanu, & Iñiguez, 2011).

Hence, this powerful modeling will be crucial in developing the FinFET device. It predicts the performance of the device in various operating conditions. It also provides insight into the underlying physical mechanisms that govern FinFET device behaviour. The mathematical model is strongly supported by the TCAD simulation, which indicates the feasibility of the fabrication of the device. Overall this study is significant for the successful development and commercialization of the device.

1.7 Thesis organisation

Chapter 1 the concept of TG-FinFET, including its structure, operation and advantages, is compactly introduced in this chapter. The remaining research study is organised as follows

Chapter 2 explores an extensive review of FinFETs. The various models of short channel FinFETs and their outcomes are briefed in this chapter. Basically, a wide literature review has been carried out to reflect current research. It also deliberates the several strategies for suppressing SCEs. Detail conversations on performance exploration based on various structures have also been provided. The extensive use of high-k materials, particularly the most promising high-k compatible with MOSFETs, is also reported.

Chapter 3 deals with the Φ model. Firstly, the TG device is viewed as a combination of symmetric and asymmetric DG-FinFET. The two dimensional (2-D)

equation Poisson's is solved individually for two DG devices. The Φ of the TG-FinFET is calculated by combining Φ of the DG devices using the perimeter-weighted sum method. The effect of the structural parameters such as gate length, H_{fin}, W_{fin} and t_{ox} are discussed. The impact of v_g, v_d, N_A and source/drain doping concentration (N_D) are also studied. All the above characteristics are validated with TCAD simulation. The percentage error between simulation and an analytical model is also conferred. The electric field is formulated from Φ. The electric field (E) variation along the channel with doping, v_g and v_d has also been examined. A comparative study is also done between SiO_2 and HfO_2.

Chapter 4 follows the similar outline of chapter 3 to formulate V_T of TG-FinFET using the perimeter-weighted sum method. The inversion charge method calculates V_T of the symmetric and asymmetric DG-FinFET. The model is applied to the $L = 10$ nm device; hence QME is also included in this model. The variation of V_T with L and W_{fin} with different electrical and structural parameters is discussed in this chapter. The increment of V_T due to the presence of QM confinement is mathematically and graphically analysed. The SCEs, namely ΔV_T and DIBL, are also studied. Likewise, in chapter 3, this model is applied to SiO_2 and HfO_2 and validated using TCAD simulation. The V_T model is compared with the published experimental results.

Chapter 5 describes the calculation of I_d for the short channel TG-FinFET device. The model is developed for a lightly doped or undoped device that is operated in the strong inversion region. The LambertW function describes the inversion charge. The CLM, 33effective drain voltage (V_{def}) and effective mobility (μ_{eff}) are used to build a precise I_d model. The small frequency parameters namely g_m and g_d are also discussed in this chapter. This model is also applied to SiO_2 and HfO_2 and validated using TCAD simulation. The model is confirmed with experimental data.

Chapter 6 deals with the trans-capacitance of the TG-FinFET device. The charge on the three terminals is estimated from the concept of I_d continuity equation and the Ward-Dutton linear charge partition method. The trans-capacitances are calculated using the MATLAB simulation by differentiating the charges with respect to terminal voltages. This model is tested individually for two dielectric materials, SiO_2 and HfO_2, and confirmed using TCAD simulation.

Chapter 7 discusses the effect of the fin shape on the device's efficacy. With the help of the models discussed in the previous chapters, this chapter offers a comparative study of V_T, I_d, g_d and g_m for rectangular, trapezoidal, triangular-shaped TG-FinFET. The SCEs viz. SS, ΔV_T and DIBL are also compared for the three shapes. A comparative study of SiO_2 and HfO_2 is discussed for the triangular-shaped device. The comparative study is authenticated using TCAD simulation.

Chapter 8 draws the overall conclusions of the research work. The pros and cons of high-k material as a gate oxide are illustrated in this section. This chapter also comprehends the limitation and the future aspect of this model.

CHAPTER - 2

FinFET – A Review

2.1. Introduction

The pandemic during the years 2020-2021, which is also the first pandemic of the twenty-first century, swept the globe dramatically. The need to conduct banking and business operations, obtain commodities etc. drastically shifted to online mode, which in turn, boosted various sectors of the electronics industry. In 2020, both the semiconductor and electronics industries were in excellent shape. Today's computing and mobile industries are revolutionizing at a prompt pace, producing more power-efficient and high-performing devices within the smaller structure. To make this a reality, transistors need to be made smaller so that a huge number of electronic components can fit in the same space. The pronounced outcome is the SCEs (Y Taur & Ning, 1998). Hence, the technology requires a structural transition other than planar structure and scaling. FinFET is a potential substitute to address the issues of SCEs (V Narendar, Rai, & Mishra, 2012). Therefore, it is crucial to conduct a comprehensive literature review in order to understand manufacturing difficulties, device modeling challenges and hitches of circuit implementation.

2.2. Annals of FinFET

The research on multi-gate (MG) MOSFET was initiated in the late eighties. In 1987, the first research work on MG transistors was disseminated by Hieda et al.

(Hieda et al., 1987). He explained that a FD body of silicon-based transistor ameliorates the switching speed because of the lower body bias effect. DELTA which was considered as the beginning of FinFET structure, was fabricated by Hisamato et al. in 1989 (Hisamoto et al., 1989). It was a DG SOI structure. Fig. 2.1 exhibits how FinFETs outperform planar structured MOSFETs in terms of short-channel performance. In this study the channel length was indicated as (L_{EFF}).

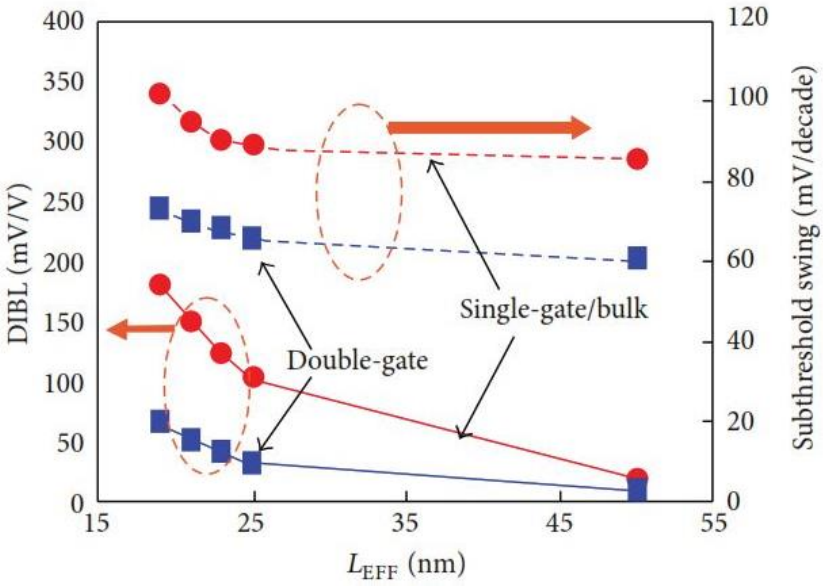


Fig.2.1: DIBL and SS with alteration of L_{EFF} for DG and bulk silicon nFET's (Nowak et al., 2004)

The revolution of FinFET application started in 20th century. In 2003, Nowak et al. released the first outline of a ring oscillator using FinFET (Nowak et al., 2003). Static random access memory (SRAM) cells and a 20 MB SRAM array using FinFET were announced in 2002 and 2004, respectively. Guillorn et al. published the first 4-stage inverter elicited from FinFET (Guillorn et al., 2008).

2.3 Structure of FinFET

Numerous articles have discussed symmetric and asymmetric FinFET structures and their application in digital and analogue circuits (Bhoj & Jha, 2013; Bhoj & Joshi, 2011; Bhoj, Joshi, & Jha, 2012; Goel, Gupta, & Roy, 2010; Sachid & Hu, 2012). The vertical channel of the FinFET is known as the fin, which has a

significant contribution in determining the channel width of the FinFET. The construction can improve gate control over the channel charge by adding more fins. The H_{fin} also determines the stability of the structure. It was reported that small H_{fin} provides better flexibility than the long fin structure (Collaert, Demand, et al., 2005; Rainey, Fried, Ieong, Kedzierski, & Nowak, 2002). The fabrication of a high aspect $\left(\frac{H_{fin}}{W_{fin}}\right)$ ratio is challenging which is required to reduce the SCE such as SS. SS increases with the increment of H_{fin} when W_{fin} is quite significant. The 3-D structure of FinFET provides better electrostatic control as well as it reduces the overall transistor footprint and 'Fin-Effect' $\left(\frac{W_{eff}}{Finpitch}\right)$. The basic and the multi FinFET architecture are displayed in Fig.2.2 and Fig.2.3 respectively.

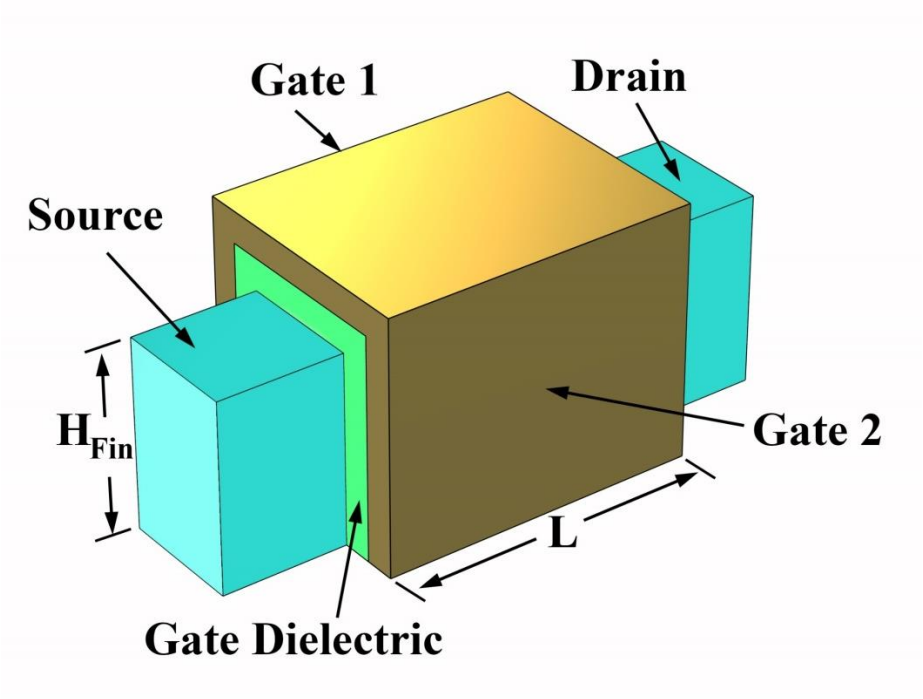


Fig.2.2: Schematic of basic FinFET architecture (Bhattacharya & Jha, 2014)

In Fig.2.3 CGP, L_S and L_{Gate} stand for contacted gate pitch (CGP) spacer length and gate length respectively. Fin pitch can be understood as the distance between the

centreline's fins. Fin pitch is scaled down to diminish the parasitic capacitance and amplify the fin effect and in brief, enhance the drive current.

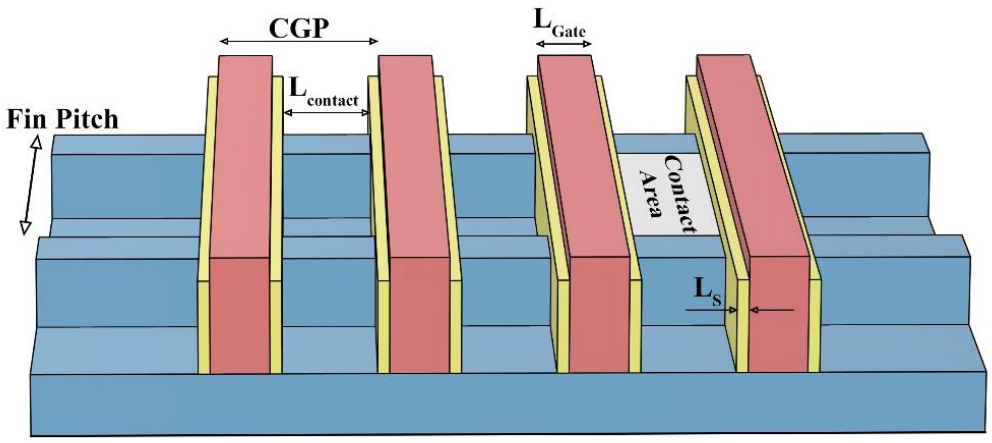


Fig.2.3: Schematic of multi FinFET architecture (Ali Razavieh, Zeitzoff, & Nowak, 2019)

In Fig.2.4, it is shown that during the five years of FinFET production, the transistor count per die area increases quadratically with CGP (just like a planar).

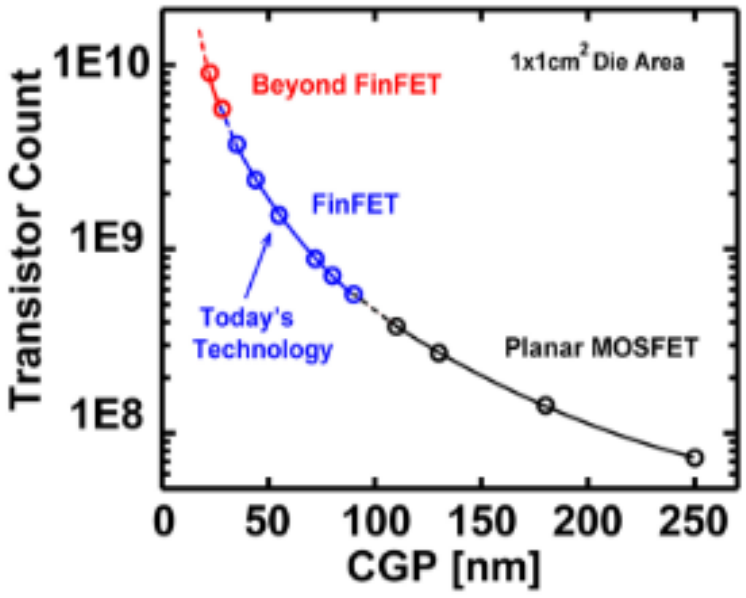


Fig.2.4: Transformation of planar technology to FinFET technology CGP (Ali Razavieh et al., 2019)

2.4. Fabrication Challenges

The jump from planar to FinFET device, impacts some significant aspects of device technology. Some important aspects are described in the following sections.

2.4.1 Fin patterning

Compared to its planar predecessor, the patterning of the fin and gate requires considerably tighter process control. FinFETs are prone to a number of significant physical fluctuations because of their tiny size and lithographic restrictions, including changes in fin thickness, gate length, gate underlap and t_{ox}. Electrical device characteristics like V_T, ON and OFF current can change due to these fluctuations, known as process variations. Depending on the fabrication method, these process variations can be uncorrelated or correlated, inter-die or intra-die. They result in mismatched device strengths and lower the overall die. Despite of all these complexities, it will provide better stability, i.e., it can be made smaller without losing performance, hence higher density. It offers lower leakage current, therefore, lower power consumption.

2.4.2. Fin shape

The gate oxide on the sidewalls of the FinFET may not be uniform. The fin's line-edge roughness (LER) determines the nonuniformity level. LER also brings on the changes in the fin thickness. The first high-performance logic device based on this technology is Intel's 22 nm node central processing unit (CPU). This CPU has FinFETs with sidewalls tilted at about 8^0 from vertical. It was reported that the fins with a lower aspect ratio (height: width) provides high mechanical stability and hence, are less exposed to damage processing (Li & Hwang, 2007). Several studies have been reported on the non-rectangular-shaped FinFET (Abd El Hamid, Guitart, Kilchytska, Flandre, & Iñiguez, 2007; Kloes, Weidemann, Goebel, & Bosworth, 2008; Song, Yu, Yuan, & Taur, 2009; Tsormpatzoglou, Dimitriadis, Clerc, Pananakakis, & Ghibaudo, 2008; Yesayan, Prégaldiny, Chevillon, Lallement, & Sallese, 2011). Wu et al. looked into the influence of nonvertical side walls with fin heights ranging from 30 nm to 70 nm (X. Wu, Chan, & Chan, 2004). A study on fin width's effect on V_T was examined

by Giacomini et al.(Giacomini & Martino, 2008). Buhler et al. looked at how the trapezoidal cross-section affects the analogue parameters' of FinFET (Bühler, Giacomini, Pavanello, & Martino, 2009). The development of trapezoidal FinFET (TZ-FinFET), the μ and the sub-band energy were described by Stanojevic et al. (Stanojević, Karner, & Kosina, 2013). Gaynor et al. inspected the impression of the cross-sectional shape on the gate leakage current (Gaynor & Hassoun, 2014). The numerical descriptions of such nonvertical side wall FinFETs were also presented in order to analyse their electrical characteristics (Giacomini & Martino, 2008; Li & Hwang, 2007). A Triangular FinFET (TI-FinFET) was also suggested that offers quick switching and less leakage current (Banerjee & Pradhan, 2019). It is reported that 22 nm TI-FinFET provides up to 70% less leakage current than the Rectangular FinFET (RE-FinFET) (K. Wu, Ding, & Chiang, 2013).

2.4.3. Gate length scaling

Electrostatic is the most important scaling constituent of CMOS technology as it imposes a direct limit on gate length $\left(L_{gate}\right)$ scaling and indirectly on the power supply voltage, hence, device performance. The scaling trends of L_{gate} and W_{fin} with respect to CGP are shown in Fig.2.5. W_{fin} also plays a major role in L_{gate} scaling.

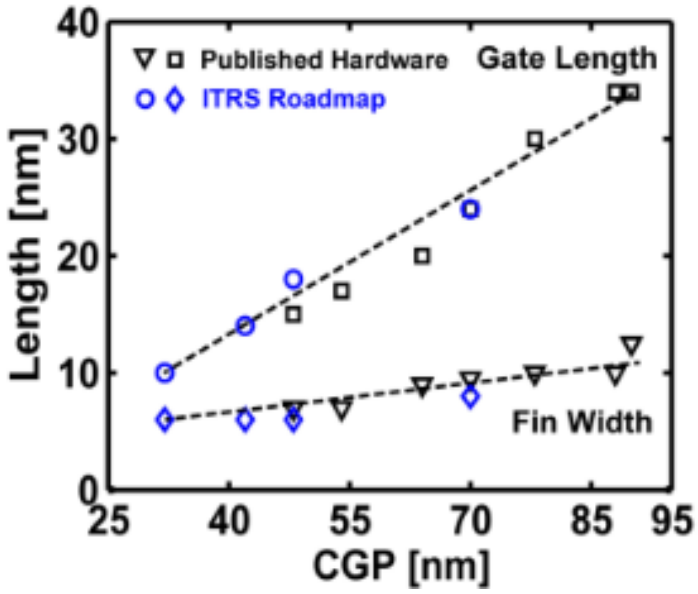


Fig.2.5: Scaling pattern of gate-length and W_{fin} Vs CGP for several FinFET technologies **(Ali Razavieh et al., 2019)**

Performance degradation can be visualised if W_{fin} is below 5 nm (Chang et al., 2011). Additionally, the presence of QM confinement increases V_T . Despite the ITRS guideline's projections, experimental data from FinFET shows that SS exhibits an upward leaning with miniaturization. The graph is given in Fig.2.6. This trend indicates that SCEs may suffer as a result of greater L_{gate} scaling.

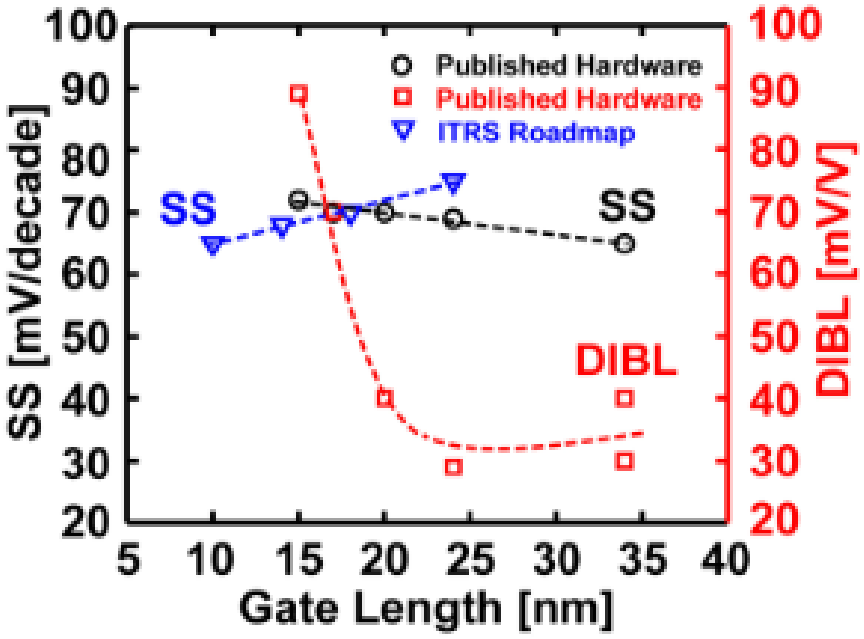


Fig.2.6: Current trends of *SS* ***Vs CGP are likened to ITRS Roadmap specify amplified SCEs in FinFETs. Experimental DIBL data likewise follows the trend (A Razavieh, Zeitzoff, Brown, Karve, & Nowak, 2017)***.

2.4.4. Doping

Normally, an undoped channel is preferred for FinFET (J.-P. Colinge, 2008). However, a lightly doped channel is chosen for better leakage current control. Doping is carried out via implantation. The requirement of a high doping agent density in the source, as well as drain area, causes the increment of series resistance. The enhancement of the electron scattering in the small channel may be the reason of enhancement the series resistance. This will damage the fin geometry. To address this issue, an in-situ epitaxial growth approach may be implemented at the drain and also in source area.

2.4.5. Orientation of fins

Fin orientation in the <100> direction causes current to flow on <110> sidewall surfaces direction. The movement of electrons in the <110 > direction is slower than <100> in the planar device. While in FinFET, the situation is the opposite. The quantum confinement effect results in improved μ in the <110> direction (C. Young et al., 2011). In some circumstances, the uniform epitaxial growth on <100> fin surfaces may be preferable to grow diamond-shaped structures on <110> walls.

2.4.6. Reliability

FD FinFETs have less transverse field, which upgrade TDDB and the positive bias temperature instability (PBTI) of n-channel MOS (NMOS). FinFET-based 22 nm technology node improves overall reliability than the 32 nm planar technology node. Whereas p-type MOS (PMOS) technology seems unchanged with respect to TDDB and PBTI (Ramey et al., 2013).

2.4.7. Parasitic capacitance

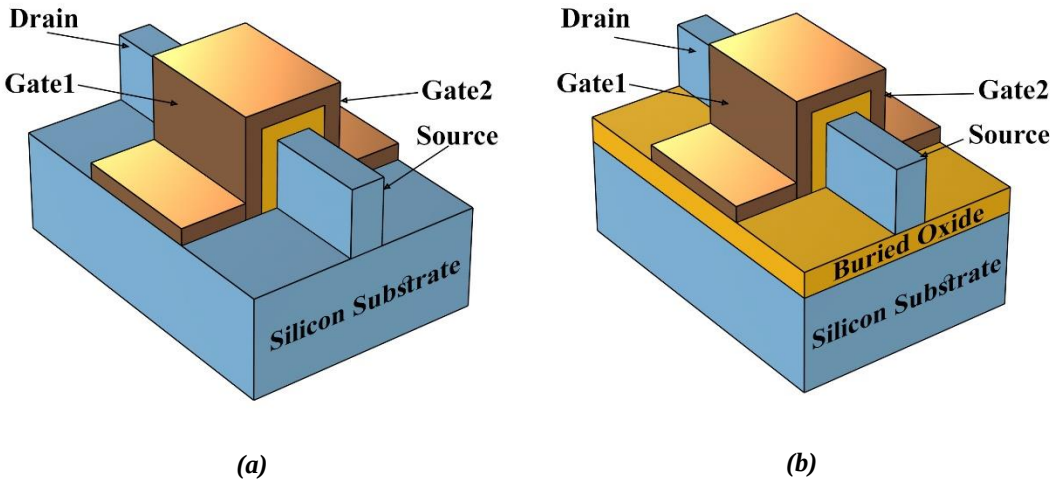
The disadvantages of FinFET architectures include higher parasitic capacitances than planar structures. The parasitic capacitance of FinFETs is decreased by increasing H_{fin} and decreasing fin pitch (Guillorn et al., 2008; Kang et al., 2013). The conformal mapping technique was used to model parasitic capacitances analytically (Agrawal & Fossum, 2010; Bansal, Paul, & Roy, 2005; J.-P. Colinge, 2008; Sharma, Dasgupta, & Kartikeyan, 2017; W. Wu & Chan, 2007). Smith modelled the capacitance of the ultra-scaled FinFET (Smit et al., 2006).

2.5. Review of FinFET

Due to the difficulties in planar technologies, an acceptable gate to channel control multi-gate FinFET devices are in recent trends. This technology allows extending the gate scaling beyond the planar transistor limits offers better SCEs. In this section, an attempt has been carried out to uncover different aspects of FinFET.

2.5.1. SOI and Bulk FinFET

Even though FinFETs on SOI wafers are widely employed, FinFETs are also fabricated on ordinary bulk wafers. FinFETs implementation on the bulk wafer is manifested in Fig.2.7(a). The same for the SOI wafer is rendered in Fig.2.7(b). In contrast to bulk FinFETs, Fins in SOI-FinFETs are corporeally isolated and share a common Si substrate or bulk.



(a) ***(b)***

Fig.2.7: Schematic diagram of (a) Bulk FinFET (b) SOI FinFET (Bhattacharya & Jha, 2014)

In 2002, design factors for the FinFET were examined using analytical modeling and 3-D simulation (Pei, Kedzierski, Oldiges, Ieong, & Kan, 2002). Reduced silicon H_{fin} or thickness can effectively manage the SCE of the FinFET. To understand the subthreshold nature, the target equation was designed with the help of 3-D Laplace's equation for the FD fins made of silicon. The V_T curtailment and SS were computed analytically in the neighbourhood of the subthreshold with the help of the 3-D electrostatic potential. The ratio of actual L and the natural length (λ) affects V_T in an exponentially declining manner. Comparisons were made between the natural lengths of single-gate FD SOI-MOSFETs, DG MOSFETs, rectangle surrounding-gate (SR) MOSFETs, and FinFETs (Pei et al., 2002).

Compared to SOI FinFET, implementing FinFET structures in the bulk wafers of silicon is particularly appealing in light of its budget friendly technology and compatibility with normal bulk CMOS. A numerical device simulator in 3-D was used

to study SOI and bulk FinFET. Poljak et al. confirmed that bulk FinFET has a comparable or superior subthreshold performance over SOI FinFET when the source/drain-to-body junctions were narrower than the gate-bottom (Poljak, Jovanović, & Suligoj, 2009). W_{fin} scaling to suppress SCEs could be hassle-free by decreasing the source/drain junction depth. Additionally, ON-state performance was investigated, and the enhanced conduction increased conduction at the edges of silicon-oxide interfaces was used to explain the variation of I_d between SOI and bulk FinFET for high levels body doping. Bulk FinFET features can be enhanced without increasing the complexity or cost of the manufacturing process by maintaining low body doping and perpetuate the junctions shallower than the gate-bottom (Poljak et al., 2009).

In another work, a concept of ground plane FinFET was proposed by Saremi et at. (Saremi, Afzali-Kusha, & Mohammadi, 2012). The ground plane lowers the DIBL by minimizing the coupling of the electric field between the source and drain. Few device properties of the suggested structure were compared to those of bulk FinFET and SOI-FinFET architectures to evaluate their performance. In addition, SOI-FinFET and bulk FinFET structures, as well as the different attributes of SRAM cells based on the recommended device structure, were contrasted.

A TCAD-based design technology co-optimization (DTCO) method presented by Wang et al. for 14 nm SOI FinFET-based SRAM (Wang et al., 2016). This method used an advanced variability-aware compact modeling methodology that completely accounted for the effects of process and lithography simulations on the layout of 6T-SRAM. The creation of the variability-aware compact model considers practical double patterning gates and fins and their effects. Finally, the effects of both local statistical variability and global process-induced variability were assessed at the transistor and SRAM levels.

A GaAs SOI FinFET was suggested by Saha et al. (Saha, Bhowmick, & Baishya, 2018). The proposed GaAs FinFET and traditional Si FinFET were compared in the study. According to the findings, ON/OFF current and channel potential both rise as dielectric permittivity rises. According to TCAD data, SS, DIBL, and ΔV_T

improved as dielectric permittivity increased. Gate capacitance and intrinsic delay were controlled by nature of the dielectric materials, and these effects grow with increased dielectric permittivity. A proposed FinFET was used to create a digital CMOS inverter, and the influence of high-k on its delay parameter was also calculated. Results indicate that the average delay grows as dielectric permittivity rises.

Nam et al. (Nam, Shin, & Park, 2018) used TCAD simulation to determine the implications of work function variation (WFV) in high-k/metal-gate (HK/MG) FinFET and FD-SOI MOSFET. For this study, they used titanium nitride (TiN), tungsten nitride (WN), tantalum nitride (TaN), and molybdenum nitride (MoN) as different gate materials with the number of grain orientations 2, 4, 3, and 2, respectively. In order to change the ratio of average grain size to gate area (RGG) value without changing the device characteristics, the TCAD simulations used four different average grain sizes i.e., 5, 10, 15, and 20 nm. It was reported that WFV-induced threshold-voltage variation (WFV-induced σV_T) was decreased by approximately 30% due to the effect of an extended gate area (EGA). Continuing the previous study, they concluded that EGA effect could be maximized by up to ~30% with the increase of work function standard deviation probability. Therefore, to reduce the WFV-induced σV_T in HK/MG CMOS technology, new metal-gate material must be developed with the following characteristics:

1) Higher standard deviation of probability for all grains and
2) Lower standard deviation of WF values for all grains.

Another study examined the efficacy of every potential fin shape in a 16 nm bulk FinFET device from a low-power design perspective, emphasizing the energy-saving trend. g_m, TGF, ON/OFF current ratio, SS, DIBL and power consumption measured the devices' performance (Mangesh, Chopra, Saini, & Saini, 2019). Applying n and p-FinFET devices with fully matching current-voltage characteristics confirmed the viability of designing low-power systems with the optimised round fin shape. This paper also examined possible applications that could successfully match modern system design and control engineering breakthroughs while optimizing power and scalability. The capacitive effects, SS, and average I_d deviation demonstrate the

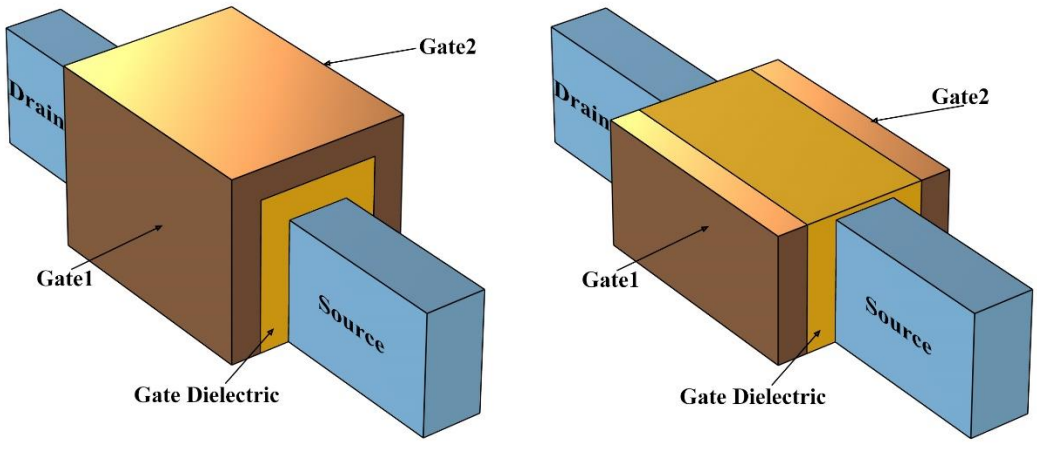
device's suitability for the use in applications that require faster switching. They proposed that the device was suitable for biomedical applications because of its thermal stability, scaled device performance, optimal power requirement, and drain current sensitivity.

2.5.2. Shorted-Gate and Independent-Gate FinFET

There are two significant FinFET categories based on the type of gate:

- Shorted-Gate (SG) and
- Independent-Gate (IG) FinFET.

IG-FinFET is a 4-terminal device and the gates are isolated from each other. In contrast, in SG-FinFET the back and front gates are shorted, which makes it a 3-terminal device. The structures of the two different FinFETs are depicted in Fig.2.8(a) and Fig.2.8(b). Comparatively, SG-FinFET provides a larger ON current than IG-FinFET as the channel is under the control of two gates. Whereas, IG-FinFET offers the flexibility of modulating V_T of the front gate by applying a different potential at the back gate terminal. However, because of the implementation of two distinct gate contacts, IG-FinFET suffers from a large area penalty.



(a) *(b)*

Fig.2.8: Anatomy of (a) SG-FinFET (b) IG-FinFET (Bhattacharya & Jha, 2014)

SG-FinFET can be further classified on the basis of symmetricity. However, the work functions of the back and front gates lead to asymmetric gate-work function (ASG) FinFET (Li & Hwang, 2007). Short channel behaviour is particularly promising

for ASG FinFET structures. Other than the gate work-function asymmetry, Goel et al. proposed asymmetric drain-spacer-extended (ADSE) FinFET, which is immune to SCEs but at the expense of the escalated layout area (Goel et al., 2010). The construction of ADSE FinFET is given in Fig.2.9. In this figure L_{SP} indicates spacer thickness and the increment of the spacer due to gate underlap is indicated by ΔL_{SP}. L_{ov} indicates the gate-source overlap. Gate length is indicated by L_G. L_{CH} is the channel length. The gate-drain underlap is indicated by L_{un}. According to Goel's study, T_{si} indicates silicon body thickness and t_{ox} is gate oxide thickness in Fig.2.9.

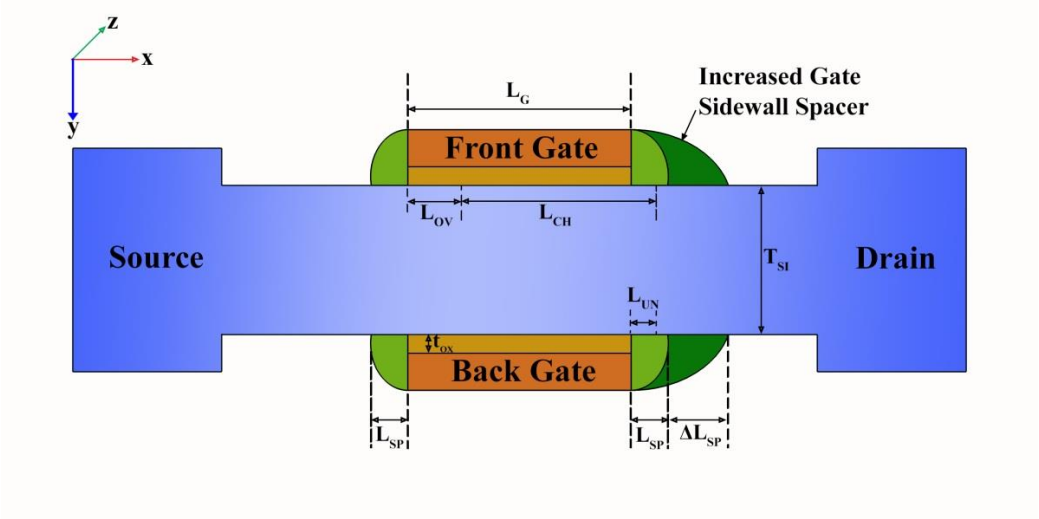


Fig.2.9: Cross-sectional view of ADSE FinFET (Goel et al., 2010)

Depending on the t_{ox}, FinFET can be again classified as DG-FinFET and TG-FinFET. The journey of the FinFET starts from the development of DG-FET.

2.5.3. Double-Gate FinFET

DG FinFET has a thick insulator layer on top surface of the fin. It deactivates the top gate. DG-FinFET's effective channel/fin width $\left(W_{eff}\right)$ is equal to (Lim & Fossum, 1983)

$$W_{eff} = 2No.H_{fin} \tag{2.1}$$

Here, *No.* indicate the total number of fins.

A core model for DG-FETs has been developed through numerous attempts. Some important models are the constant μ model (Zhu, Zhou, Chandrasekaran, Rustagi, & See, 2007; Z Zhu et al., 2007), charge sheet model (Mohan V Dunga et al., 2006; Pei, Ni, Kammula, Minch, & Kan, 2003), velocity saturation model based on the Caughey-Thomas model (Caughey & Thomas, 1967) etc.

The anatomy of the DG-FinFET is shown in Fig.2.10.

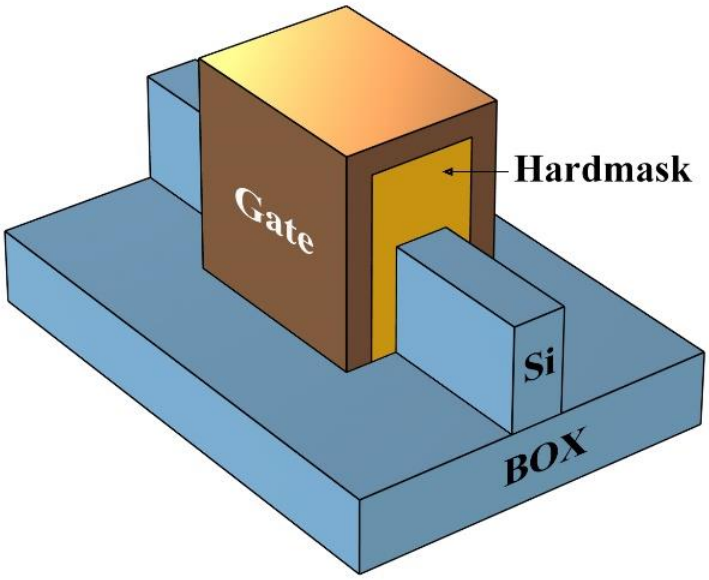


Fig.2.10: Anatomy of DG-FinFET (Maurya & Bhowmick, 2021)

3-D simulations were done on the impacts of DG-FinFETs with nonrectangular fin cross-sections (X. Wu et al., 2004). The inclination of the sidewalls reduces the SCE immunity such as DIBL and *SS* for a particular top-fin width, which is determined by the photolithography stage. Additionally, nonrectangular fin design causes current crowding and nonuniform flow in the vertical direction. The nonlinear dependency of ON current with fin heights was noticed in addition to the non-uniform series resistance in the H_{fin} direction. This work classified the effects of inclination angles nonvertical sidewalls. The device's performance at various fin heights was characterized by various inclination angles mandated by the processing method. They also concluded that H_{fin} must be restricted by available technology (X. Wu et al., 2004).

Due to higher SS, reduced SCEs, better μ and driving current, DG devices with ultra-thin bodies were most favourable for miniaturing into the sub-20 nm regime. The FinFET device structure is most suitable with current industry norms. How to build a source/drain junction in the fin region of a FinFET and how to design metrology tools to quantify it are two challenging fabrication concerns. This study explored the difficulties of imbedding ultra-thin fins and monitor the concentration of fin doping (Pham, Larson, & Yang, 2006). According to Pham. D et al. the best dopant distribution in the fin requires a high angle of implantation at a specific energy. Fin doping measuring metrology was created using Raman microscopy. By facilitating junction diffusion under the gate and reducing current dispersion, a gate-source/drain underlap FinFET architecture was investigated for the purpose of making a feasibility study of FinFET junction formation. Optimal characteristics and robust process variation was exhibited by simulation (Pham et al., 2006).

Lo et al. in 2007 presented a model for Φ of a symmetric DG MOSFET (S.-C. Lo, Li, & Yu, 2007). To approximate the potential distribution in the silicon film of a DG MOSFET in several operating areas, including depletion, weak inversion, and strong inversion, an approximate one-dimensional closed approach was developed. A QM correction formulation was included for the mathematical simulation of DG MOSFETs in the microscopic scale. The V_T model of undoped symmetric DG MOSFET was proposed by Abd El Hamid et al., and it was based on 2-D Poisson equation (Abd El Hamid, Guitart, & Iñíguez, 2007).

According to the 2008 Semiconductor Industry Association International Technology Roadmap for Semiconductors, DG-FinFET with high-k (ZrO_2) was designed by Nirmal, D., & Kumar, P. V (Nirmal & Kumar, 2011). According to their hypothesis, DG-FinFET-based CMOS with a 10 nm gate length was built to give impressive performance with good trade-offs between speed and power consumption. The TCAD simulation was used to confirm the model. The V_T was 0.653 V and the leakage current of 9.47×10^{-14} A was obtained for the proposed device. They claimed that future high-speed logic applications would be benefited from discussed structure, which would also boost storage capacity (Nirmal & Kumar, 2011).

In 2019, a heterojunction, DG tunnel FinFET structure (having source overlap region) was proposed by N. P. Maity et al. (Maity, Maity, & Baishya, 2019). The 2-D Poisson's equation and inversion charge density were solved to model the Φ of the structure. The g_m change approach was used to extract V_T. The results depicted that the Φ rises while employing high-k dielectric material (HfO_2) because of the impacts of the fringing field from the bottom of the gate terminal. They got V_T of 0.55 V with I_{ON}/I_{OFF} above 10^8 at $v_d = 0.5$ V. The analytical predictions were well-matched with the TCAD simulation.

2.5.4. Triple-Gate FinFET

The structural layout of TG and DG-FinFETs is nearly identical, except that however, the t_{ox} is uniform for all the three gates in TG-FinFET. So, the device is dominated by the three gates. Therefore, W_{eff} of TG-FinFET will become,

$$W_{eff} = 2H_{fin} + W_{fin} \tag{2.2}$$

The constructions of TG-FinFET is exhibited in Fig.2.11.

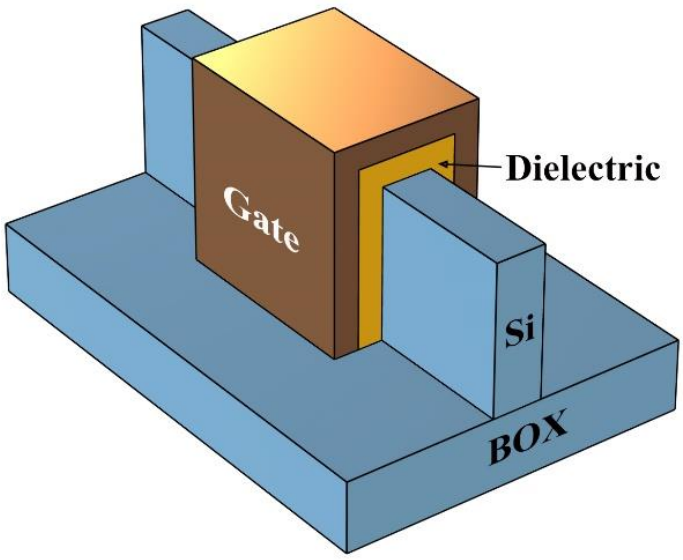


Fig.2.11: Anatomy of TG-FinFET (Maurya & Bhowmick, 2021)

Jin et al. developed a mathematical model for V_T (Jin, Zeng, Ma, & Barlage, 2007). This model for TG Si MOSFET device was based on 3-D Poisson's equation and solved with eight boundary conditions. The DESSIS from the Sentaurus simulator is used to verify the analytical results.

The subthreshold drain and gate leakage currents were examined for TG-FinFETs with a v_d of 1 V. The W_{fin} and gate length were used to assess the drain and gate leakage currents. Due to the SCEs, the evaluated subthreshold I_d in broad FinFETs is significantly higher than the gate tunnelling current. The significance of the trap-assisted sidewall-gate edge tunnelling current on the drain leakage current was established by A. Tsormpatzoglou et al. in thin FinFETs with negligible SCEs. The increased sidewall-gate interface trap density was more than the top-gate interface trap density and linked to this leakage current pattern with decreasing W_{fin}. The investigated devices with $H_{fin} = 65$ nm had a gate length that ranged from 50 nm to 910 nm, and support fin widths 25 nm, 55 nm, 125 nm, and 875 nm. As a result, the current devices were compliant with ITRS for high performance (HP) and low operating power (LOP) technologies (Tsormpatzoglou, Dimitriadis, et al., 2009).

A charge-based compact capacitance model was used to describe the capacitance-voltage properties of undoped or weakly doped ultra-scaled TG-FinFET (Nikolaos Fasarakis et al., 2012). All trans-capacitances were analytically derived by I_d continuity and Ward–Dutton linear-charge-partition method. The derived capacitance model was valid from the linear region to the saturation and the subthreshold region through the strong inversion domain. 3-D numerical simulations over a wide variety of device dimensions were used to validate the gate and source trans capacitances. This small model is highly helpful for circuit designers since the parameters employed in the capacitance model may be utilized to precisely anticipate the transfer as well as output characteristics of a given transistor. It was reported that in comparison with DG-FinFETs, TG-FinFET has a lower gate to source capacitance (Anil, Henson, Biesemans, & Collaert, 2003; Lin et al., 2010).

2.5.5. Multi-Gate FinFET

A unified analytic drain-current model for different types of MG MOSFETs, such as TG, quadruple-gate (QG), Omega-gate and Pi-gate MOSFETs, was described in another study by Yu and his companions (Bo Yu, Song, Yuan, Lu, & Taur, 2008). Their previously developed potential models for highly symmetric DG and SR MOSFETs served as the basis for this unified model. The inversion charge in the subthreshold region of MG MOSFETs is a linear function of the silicon cross-sectional area (volume inversion), but the inversion charge above the threshold condition is a linear function of gated perimeter of the silicon body. They developed the QG-MOSFET model in terms of SR-MOSFET. By combining DG MOSFET and QG-MOSFET linearly, the additional MG MOSFET models were created. The models were validated using numerical simulations.

For analysing the electrical properties in contemporary nanoscale DG and TG FinFET devices, Tsormpatzoglou et al. created a new Y-based methodology (Tsormpatzoglou et al., 2012). This model use I_d which includes the LambertW function in the linear region and converts the nonlinear Y-function to the linear function of a long channel conventional MOSFET. This Y-function can quickly evaluate V_T , μ, mobility attenuation coefficients and series resistance conventionally, as the associated curves were linear and simple to extrapolate. Both simulated and experimental results confirmed the high accuracy of the current methods for collecting the electrical parameters.

Two comprehensive compact models based on Φ were created to develop MG transistors for IC designs. The BSIM-CMG (common-multi-gate) model, which was established to simulate, all-around-gate, TG, and DG FinFET, was the first compact model for the FinFET that was accepted by the industry. The independent-multi-gate BSIM-IMG (independent-multi-gate) model, which captures the dynamic V_T adjustment with back gate bias, was created for independent DG with ultrathin body (UTB) transistors. A Poisson-carrier transport approach was first used to derive the fundamental models beginning with long-channel devices. The outcomes of rudimentary models and numerical device simulators (two-dimensional) were in agreement. The models considered all of the significant real-device effect such as

SCEs, parasitic parameters, mobility degradation and QM confinement effects. Fabricated silicon-based data from various technologies were used to validate BSIM-CMG and BSIM-IMG. The created design also need to pass the quality control tests to be placed before the production level (Paydavosi et al., 2013).

A unified FinFET compact model presented by Duarte et al. (Duarte, Paydavosi, Venugopalan, Sachid, & Hu, 2013). described the device with intricate fin cross-sections. The proposed model successfully predicted the current-voltage properties of several FinFET topologies, including DG, Cylindrical Gate-All-Around (Cy-GAA), and Rectangular Gate-All-Around (RE-GAA) FinFETs. Trapezoidal TG (TZ-TG) FinFETs were also accurately modelled for the first time. SCEs were also examined and the TCAD simulation outcome validated the analytical model.

A 3-D analytical modeling of SOI MG FinFETs was described, including GAA, TG, and DG-FinFETs (Vadthiya Narendar & Mishra, 2015). The superposition approach was used with the proper boundary conditions and effective dimensions, to obtain the channel potential from each FinFET's 3-D Poisson equation. The analytically modelled data agreed with all the structures' numerically simulated data. Variations in fin thickness have been used to examine how the gate-stack (GS) high-k gate dielectrics affect the SCEs of all the devices discussed above. They discussed how high-k materials affect the electrical parameters of all FinFET devices. In high-k dielectrics, μ degradation due to remote coulomb scattering (RCS) and remote phonon scattering (RPS) is a significant problem. By sandwiching fixed-thickness interfacial-layer (IL) and high-k dielectric materials between the metal gate and semiconductor, the μ degradation issue in GS high-k dielectrics has been managed. In all FinFETs, the GS high-k dielectrics effectively suppress the SCEs. At $H_{fin} = 25\,\text{nm}$, $W_{fin} = 6\,\text{nm}$, gate length = 20nm and EOT = 1.1nm, all FinFETs exhibited their optimal performance.

Chopade, S. S. & Padole, D. V. studied the features of TG and DG FinFET (Chopade & Padole, 2017). It displayed the shift in V_T brought on by depletion charges. The influences of the channel depletion charge close to the source/drain and substrate interface were considered while modeling I_d equation. The drain ON and

OFF current was examined as a function of the number of fins and the thickness of the fins, i.e., the study was related to multi-fin FinFET devices. It also analyzed the corner effect and suggested that a rounded corner can diminish the corner effect as well as the leakage current. They concluded that I_d increases with the number of fins without growing the SCEs. The TCAD simulations verified the analytical model.

2.5.6. Symmetric high-k Spacer hybrid FinFET

The innovative advantages of symmetric high-k spacer (SHS) hybrid FinFET over traditional FinFET were assessed by Pradhan, K.P., & Sahu, P. K. (Pradhan & Sahu, 2016) . The 2-D UTB, 3-D FinFET, and high-k spacer are three important and cutting-edge technologies combined in the SHS hybrid FinFET to improve device performance. This study introduced the SHS hybrid FinFET for the first time and suggested that this would enhance device performance. The anatomy of hybrid FinFET is given in Fig.2.12.

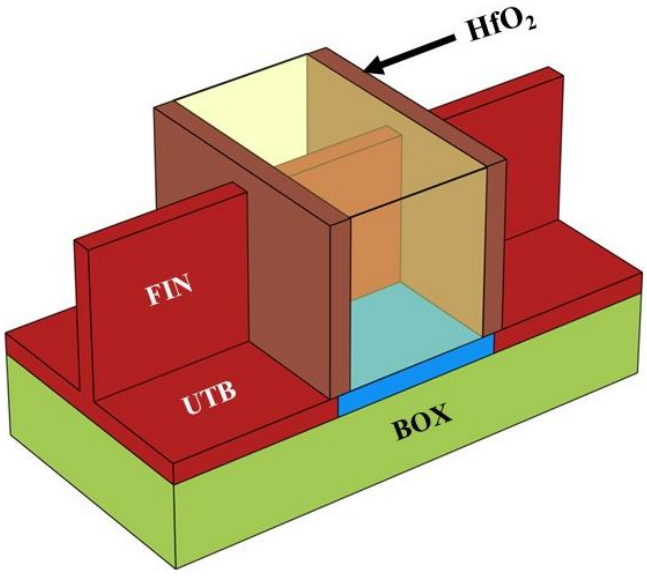


Fig.2.12: Anatomy of SHS hybrid FinFET (Pradhan & Sahu, 2016)

By varying the high-k spacer length (from 1 to 5 nm) in the hybrid FinFET ($L = 20\,\text{nm}$), several parameters including SS, ON-OFF current ratio, g_m, TGF, gain, total gate capacitance and cut-off frequency were sensibly detected. 3-D device simulation proved that the recommended device was more effective at suppressing SCEs and predicted a larger drive current than a traditional FinFET.

2.5.7. Quantum FinFET

Devices with tiny geometries heavily rely on QME. The energy gap widens and electrons move into the first sub-band above the conduction band as the carrier energy quantisation is sparked by structural confinement.

ATLAS Silvaco device simulator was used by Boukortt et al. (Boukortt, Hadri, Patanè, Caddemi, & Crupi, 2017). To analyse the characteristics of n-channel FinFET. The quantum Bohm potential model was included to support quantum mechanical confinement. The impact of the L and the channel doping density on FinFET characteristics, was also discussed. They recommended ZrO_2 as an alternative to SiO_2.

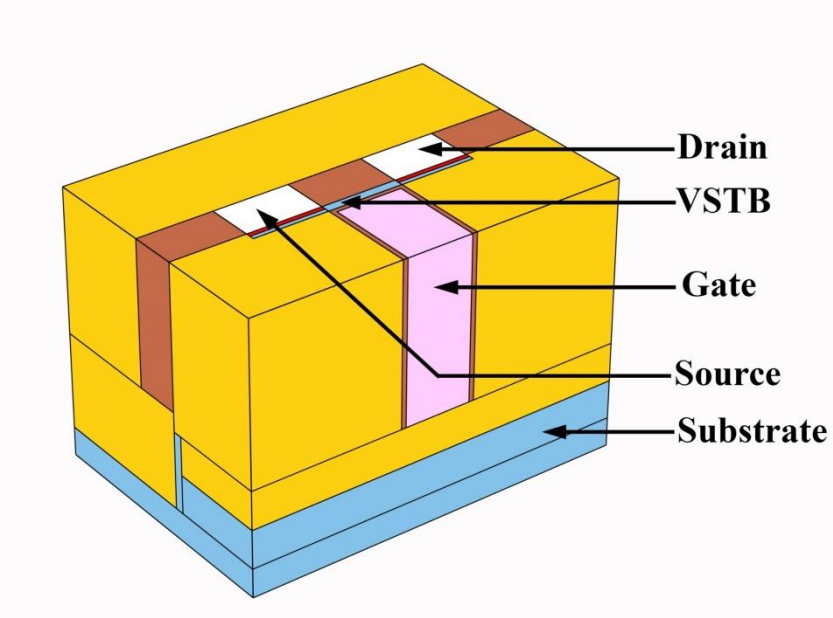


Fig.2.13: Anatomy of QFinFET (Maity, Maity, Maity, & Baishya, 2019)

The quantum FinFET (QFinFET) is another variation of the FinFET. It was first reported by Viktor Koldiaev and Rimma Pirogova (Pirogova, Wolf, & Koldiaev, 2016). A low doped vertical super-thin body (VSTB) was the main feature of this architecture. This device designed on a dielectric wall. A single gate was designed on one side of the fin and source and drain that are 2-D self-aligned were designed on the other side. The STI (shallow trench isolation) wall was vertically etched to form holes which were filled with high-doped crystalline or polysilicon material that has been properly doped with silicides, metal contacts. This creates the source terminal and

drain terminal. The gate was attached to the bulk wafer at its bottom with isolation on the channel, gate dielectric, and top part. The anatomy of the QFinFET is depicted in Fig. 2.13.

A comparative study between QFinFET and TG-FinFET was reported by N. P. Maity et al.(Maity, Maity, Maity, et al., 2019). The gate dielectric stack, which donates to an EOT = 0.86nm was maintained throughout the investigation, and consisted of SiO_2 layer with a thickness of 0.5nm and HfO_2 with a thickness of 2nm. They concluded the QFinFET could perform better when the physical parameters of the devices were scaled down to the atomic level. It is undeniably true that the QFinFET can transcend the constraints placed on TG-FinFET devices and it might be considered the next generation of FinFET components.

2.5.8. Multiple fin FinFET

Multiple fins constructed FinFET (M-FinFET), is a promising semiconductor device for future CMOS technology development. Das et al. (R. R. Das, Maity, Chowdhury, & Chakraborty, 2021) performed a thorough examination of such device features and a stress analysis of the suggested device structure for the first time. The structure of M-FinFET is discussed in Fig.2.3. This study introduced a novel M-FinFET structure based on GaAs that could perform better than existing FinFET structures when compared to their existing counterparts. In addition, researchers gave an idea to relate the device's performance with different electrical properties, such as electron density, electron velocity, and μ. For various gate lengths and in the presence or absence of the stress effect, many significant electrical characteristics of the device, such as the ON current, V_T, sub-threshold swing, switching ratio, and major RF/analogue parameters, were evaluated. Results indicate that adding stress to M-FinFET increased ON current by 159.2%, device efficiency by 49.36%, and intrinsic gain by 17.23%, which are very beneficial for low power applications. In addition, the relationship between linearity and stress effect was examined.

2.5.9. FinFET with different fin shape

The importance of the fin shape is discussed in section 2.4.2. The device's performance influenced by the fin shape, W_{fin} and H_{fin} . Using the superposition method, Yang et al. arrived at an analytical solution to Poisson's equation in 3-D space for the doped FinFET (W. Yang, Yu, & Tian, 2007). The expression for the minimum channel potential was further simplified using the evanescent-mode approach. They provided geometrical properties of the device also suggested an empirical equation to forecast the SS value.

The proposed study of Subramanian et al. highlighted the effect of the W_{fin}, a crucial geometrical component of FinFET devices (V. Subramanian et al., 2007). The Figures of Merit (FOM) of transistors in the near-threshold region (such as V_T, SS, and DIBL), linear region (μ, series resistance, 1/f noise), and saturation region (normalized transconductance) were analysed as a function of W_{fin} based on static and low-frequency measurements on n-FinFETs (C-V, I-V, and 1/f noise). They stated that the interaction between the back and top gates was strongly impacted by W_{fin} in the region close to the threshold. Whereas in the region above the threshold, the parasitic source/drain resistance which influences the other strong inversion parameters, was seen to be most significantly impacted by W_{fin}. When W_{fin} is lessened, the back-gate coupling coefficient falls, making the front gate V_T unresponsive to the back bias. The fin widths between 25 nm to 75 nm produce a small front-gate coupling coefficient (0.01) that leads to a nearly perfect SS of the long channel. Though the series resistance value extracted in the neighbourhood of saturation is larger, but greater for different W_{fin}, signifying further deterioration of the device performance. The series resistance takes out in the linear region, on the other hand, exhibits an inverse power law dependence with W_{fin} and an exponent nearly equal to two. It was discovered that the series resistance has a significant impact on the FOMs, making de-embedding necessary for the precise exploration of intrinsic transistor FOMs. μ of electrons was strongly controlled by the W_{fin}, and peak of μ was reduced by up to 50% in the case of narrow width FinFETs. The transconductance-to-current ratio was poorly correlated with narrow W_{fin}. The narrow fins caused an increment of low-frequency noise,

suggesting that the fins' sidewalls have a higher interface trap density than the top surface. Last but not least, they suggested that the selective epitaxial growth (SEG) technique effectively lowered the parasitic source/drain resistance and the outcome is increased g_m and drive current, particularly for small fin widths. Though, this advantage is somewhat offset by increased (10%) parasitic capacitances caused by the spacer's coupling to the gate and source/drain.

Instead of the rectangle intended by design, the trapezium shape is frequently used to mimic the FinFET cross-sectional geometry. The frequent vertical width fluctuations brought on by the etching method may result in sloped sidewalls. Therefore, there is a wide range of variations in the inclination angles. The device's electrical properties could significantly change due to these geometric variances. Through 3-D numerical modeling, the impact of inclination angle of the FinFET sidewall was examined on several important parameters like V_T, g_d, g_m, gate capacitance, intrinsic voltage gains and unit-gain frequency for analogue designs. Changes in g_d and g_m have an impact on the intrinsic gain. The findings established that the g_d mostly depends on the average W_{fin} and feebly relies on the sidewall inclination angle, whereas the g_m primarily depends on the sidewall inclination angle (θ_i) and the fixed average W_{fin}. g_m deteriorates when the fin top is narrow than the fin base. The simulation findings also showed that higher voltage gains might be achieved with smaller average fin widths and θ_i which is equivalent to inverted trapezoids, that is, when the top of the fin is larger than the base of the fin. The overall gate capacitances exhibited sidewall angle-dependent behaviour as well. Lower unit gain frequency was achieved for larger inverted shape trapezium. The W_{fin} and cross-sectional design influence the V_T (Bühler et al., 2009).

The electrical parameters of rectangular and trapezoidal TG bulk FinFETs for 20 nm gate length was examined using a 3-D numerical device simulator (Gaurav, Gill, & Kaur, 2015). A reduction in SCEs, such as leakage current, DIBL, and SS, was seen when the shape of the fins was changed from rectangular to trapezoidal.

Researchers also examined at the effects of changing the device's fin shape from rectangular to trapezoidal on performance (Gaurav et al., 2015).

Zhihao Yu paid attention to the effect of the fin shape (Z. Yu, Chang, Wang, He, & Huang, 2015). The proposed two-incline-angle explanation of the fin shape was straightforward and quantitative. Using this approach, the control capabilities of four common fins (trapezoidal, rectangular, convex, and concave) on the fictitious silicon limiting process node (sub-10 nm) were evaluated. Their effects on FinFETs' characteristics were also explored in detail. The findings indicated that the rectangle shape fin was superior in respect of analogue and digital qualities, whereas the trapezoidal one is preferred in the low-power application fields due to its low V_T . They did not understand the relationship between fin shape and its frequency characteristic. A ratio between the W_{eff} and the channel cross-section area was revealed by a thorough analysis. The suggested factor can objectively assess the impact of fins, both those with regular shapes and those with irregular shapes. This study provides design guidelines for nanoscale silicon FinFETs and alternative FinFETs made of advanced materials.

Electrical characteristic clarification and simulation were studied to examine the effects of width quantization and stressing-induced device degradation on high-k/metal TG n/p-type FinFETs (W.-K. Yeh et al., 2016). The experiment was conducted on trapezoidal shape Si-FinFET by Yeh et al. Due to a larger inversion carrier density in the centre of the channel, the experimental results for n-type FinFETs demonstrated that the thinner bottom width device works with greater reliability under hot carrier injection (HCI) stress. Because of the larger electric field within the Si-fin and the higher energy of the inversion holes, the thinner bottom width of p-type FinFETs under negative stressing voltage exhibited more severe degradation on I_d and SS with the increment of the stressing voltage. In contrast, the thicker bottom device exhibited better reliability under negative bias temperature instability (NBTI) stress and almost insensitive to stressing voltage. Sentaurus Structure Editor was used to extract the electrical parameters of the device.

2.5.10. Capacitive and Resistive study of FinFET

C_{ox} is the most important parameter for any kind of FET. It mainly affects the I_d and the speed of the device. Other than C_{ox}, fringing capacitance, parasitic capacitance, resistance also have an impact on the device performance. Using numerical modeling, Trivedi et al. first described the impact of the gate fringing field in the DG MOSFET on total gate capacitances (Trivedi, Fossum, & Chowdhury, 2004).

Wu, W., & Chan, M. S., examined the parasitic components that depend on the geometry of multi-fin DG-FinFETs (W. Wu & Chan, 2007). A conformal mapping technique is used to model overlap capacitance and parasitic fringing capacitance as functions of the gate shape parameters. A physical model of gate resistance was also described, along with couplings between source/drain and gates caused by parasitic capacitive forces. In-depth research was carried out on the influence of geometrical parameters on FinFET design for various device configurations.

To improve device performance, a group of researchers have concentrated on the incorporation of materials with greater dielectric constants (high-k). The potential benefits of high-k materials are to provide a thinner oxide layer, large gate capacitance and high ON current. Additionally, the parasitic gate-source/drain outer-fringe capacitance is decreased due to the high-k dielectric's greater physical thickness (Manoj & Rao, 2007).

FinFETs at the 22 nm node have a higher fringe capacitance $\left(C_{fr}\right)$ than equivalent planar MOSFETs, according to Manoj et al. report (Manoj, Sachid, Yuan, Chang, & Rao, 2009). C_{fr}, which affects the circuit delay in digital applications, was reported to rise with the application of the high-k spacers.

The physical properties of FinFET were examined by Nezafat et al. (Nezafat, Zeynali, & Masti, 2014). Tiber CAD software's semi-classical electron transfer approach based on drift-diffusion supposition was employed for the investigation. According to simulations, output resistance was negative and this negative resistance can be employed in the oscillator.

A negative capacitance FinFET (NC-FinFET) was created by involving a high-quality epitaxial bismuth ferrite ($BiFeO_3$) ferroelectric capacitor in the gate terminal of both n-type and p-type FinFETs (Khan, Radhakrishna, Chatterjee, Salahuddin, & Antoniadis, 2016). Both devices provide very sharp SS of 8.5-50 mV/decade. Khan et al. quantitatively matched the experimental value of NC-FinFET transfer characteristics with the self-consistent simulation technique based on the BSIM-CMG model and the Landau-Devonshire formalism.

A comparative study between p-channel gate-source/drain under lapped silicon FinFET with HfO_2 high-k spacer and SiO_2 low-k spacer was analysed by Sachid et al. (Sachid, Chen, & Hu, 2016) The experimental findings indicated that owing to better series resistance in the underlap regions and the capacitance coupling between the gate and the underlap areas, decreases in the case of the HfO_2 spacer structure. Due to enhancement of electric field in gate fringe of the HfO_2 spacer structure, it was observed that the g_m and I_d have increased almost three times than the SiO_2 spacer structure in the saturation region. The high-k spacer additionally raised the barrier height in the off-state, lowering DIBL and SS, especially for short channel devices.

Based upon a complete intrinsic-extrinsic model for symmetric doped DG MOSFETs, Avila et al. (Avila et al., 2016). inspected the effect of gate resistance of FinFETs on the performance of inverters and ring oscillators. The performance of circuits with single-finger and multi-finger configurations was compared to examine the effect of the extrinsic gate resistance. It was demonstrated that the multi-finger configuration decreases intrinsic gate resistance that enhances the propagation latency when the overall number of fins remains same. Additionally, they reported that source/drain fin extension and fin spacing were crucial factors in enhancing the performance of digital circuits. They concluded that for digital circuits based on TG-FinFETs must incorporate the extrinsic gate resistance in the analytical model to mature exact design methodologies.

To calculate the bias-dependent inner fringe capacitance in nonplanar DG-FinFET structures with doping-regulated source/drain and gate underlap, for sub-20-nm node, Sharma et al.(Sharma et al., 2017) offered a new mathematical approach

established on successive conformal mapping. 3-D devices made on bulk oxide, gate-source/drain extension with inhomogeneous doping gradients, and spacers were taken into account by the model. For different fin widths and oxide thicknesses, the percentage fluctuation of inner fringe capacitance with respect to underlap length was investigated.

2.5.11. Fabrication of FinFET

Fabrication challenges such as fin patterning, doping, gate engineering, fin orientation have been discussed in section 2.4. The following studies are presented in relation to fabrication challenges:

When it comes to scaling and manufacturing, FinFET and its derivatives are excellent, despite the fact that there are only a few competitors for the innovative "backbone" device contenders in the post-planar CMOS era. In his paper, Bin Yud et al. discussed the design complications, difficulties related to fabrication along with performance issues and integration problems of DG-FinFETs with aggressively reduced physical gate lengths to 10nm and W_{fin} to 12nm (Bin Yu et al., 2002). Devices having wide range of gate lengths showed excellent short-channel performance. The manufactured p-channel FinFET's hole μ was significantly inflated than that of a conventional planar MOSFET because of the orientation of the <110> channel crystal. The FinFET having holes as the majority carrier (p-channel) has an unprecedented g_m at 105 nm gate length. Additionally, they discussed the CMOS FinFET inverter circuit (Bin Yu et al., 2002).

A DG device with a 30 nm gate length with reduced parasite series resistance was manufactured by Kedzierski et al. (Kedzierski et al., 2003). To reduce parasitic resistance in FinFETs, angled extension implants and selective silicon epitaxy were studied in detail. These two methods are allowed to manufacture high-performance devices with ON-currents at par with those of fully optimized bulk silicon technologies. An in-depth discussion was given regarding the impact of short channels and fin thickness on device resistance.

Hydrogen annealing was used to improve the electrical properties of the FinFET (W. Xiong et al., 2004). Prior to gate oxidation, the silicon fins' edges were rounded off during the FinFET fabrication process, and the surface plane of the fin sidewalls was smoothened. This process significantly enhances the leakage of charges through the gate terminal while also narrowing the fins, which lowers the V_T and improves the features of DIBL. After rounding the edges via the processes like hydrogen annealing, the leakage current turns down by up to fourth order in magnitude. In addition, a 50% drop in DIBL was reported by Xiong et al. as a result of the narrowing of the fins (W. Xiong et al., 2004).

The critical dimension (CD) of IC has decreased due to CMOS scaling. Si-based technologies compose a sizeable portion of the line CD with LER at sub-45 nm nodes and this is an achievable and practical FinFET design. In these circumstances, knowing the effect of LER on FinFET performance was essential for satisfying numerous device standards. Baravelli et al. investigated the impact of LER on the functionality of FinFETs using statistical device simulations (Baravelli et al., 2007). Comparing the respective weightage of fin and gate-LER. Under DC and transient operations, fin-LER was demonstrated to reduce FinFET matching performance. It was demonstrated that fin-LER would predominate the intra-bit-cell stochastic mismatch in FinFET static random-access memory at the low standby power (LSTP)-32 nm node by combining the simulation results developed with experimental data. A comparative study was given between the electrical performance of resist-defined fin (RDF) and spacer-defined fin (SDF) patterning approaches. It was established that the spacer-defined approach could increase FinFET matching performance by 90% with respect to RDF patterning.

Hayashida et al. discussed a relative study on the electrical attributes of stacked-gate FinFETs employing ON current of n+-poly-Si/PVD-TiN and μ for various fin heights (Hayashida et al., 2012). The diagram of the aforesaid structure is depicted in Fig.2.14.

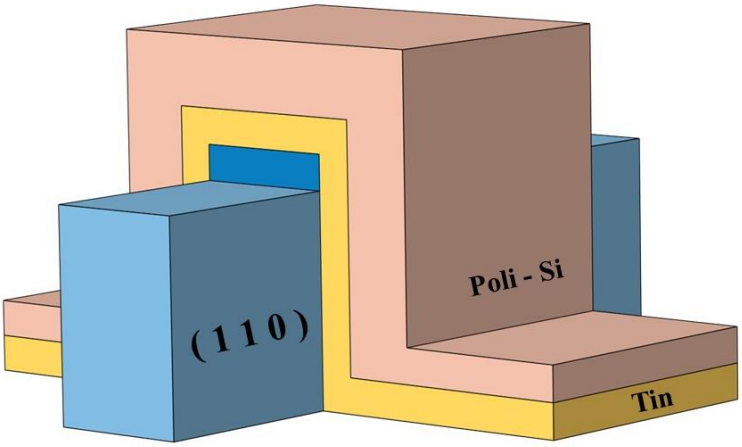


Fig.2.14: Anatomy of stacked-gate FinFET

Due to greater tensile stress, devices with taller fins had better μ. However, the ON current for devices having taller fins got worse when gate length shrinks, most likely due to having high valued parasitic resistance $\left(R_p\right)$. Furthermore, due to poor etching on the fin sidewall, V_T variance has been increased as the H_{fin} got raised. They concluded that to take advantage of the HP of tall FinFET, process technologies resulting lowering of R_p and etching technology that produces smooth, precise profiles, were the most important criteria.

The impact of gate engineering (with high-k dielectrics) was analysed by Nirmal et al. elucidating the performance of FinFET in system-on-chip applications (Nirmal, Vijayakumar, Thomas, Jebalin, & Mohankumar, 2013). The gate technology of dual-material (DM-FinFET) and the Sentaurus simulator were used to analyse g_m, TGF, DIBL, intrinsic gain, output resistance and intrinsic gate capacitances. They showed that optimizing fin doping, gate work function and W_{fin} can improve the SCEs. A 3% increase in g_m and an enhanced I_d are both exhibited by this device. Compared to traditional devices, the ZrO_2-based device shows an exponential decrease of DIBL by 75%.

Lu et al. considered the device physics of SiGe FinFET (D. Lu et al., 2014). They also introduced process integration and device modeling. It is an established fact that germanium (Ge) exhibits more hole μ than silicon. In SiGe epitaxy layers, lattice

mismatch strain significantly increases hole velocities. Uniaxial stress is additionally advantageous for device performance. When SiGe film is etched into stripes, biaxial tension automatically transforms to uniaxial stress. Furthermore, the SiGe-channel Ge content can be changed to modulate the device V_T . The hindrances like removal of interface trap states occurring at the gate-dielectric interface, n-type dopant quick diffusion and critical thickness are main challenges in fabrication of SiGe film.

Using digital etching and precision dry etching, the first sub-10 nm InGaAs FinFETs were created by Vardi, A., Zhao, X., & del Alamo, J. A. (Vardi, Zhao, & del Alamo, 2015). W_{fin} in the sub-10 nm range provides V_T , which is extremely sensitive to the W_{fin}. Compared to Si-based devices, this was greatly improved since InGaAs has low effective electron mass. According to 2-D Poisson-Schrodinger simulations, quantization effects are responsible for this phenomenon. They further demonstrated that V_T variation at similar dimensions was greatly reduced in the quantum regime when sidewall slopes are lower than 85^0.

Using a template-growth technique, Chen et al. (M.-L. Chen et al., 2020) described how various types of mono-layered 2-D crystals were isolated in a vertical method. This leads to the creation of FinFETs with one atomic layer fin and the ON/OFF current ratios around 10^7. They achieved a 300mV per decade SS for transitional metal dichalcogenide monolayer (TMD ML) FinFETs. COMSOL Multiphysics model was used to simulate 4 nm gate length and $W_{fin} = 0.65\,\text{nm}$ ML FinFET. The group also fabricated TMD fin-array ML-FinFET with a minimum pitch of 50 nm with different fin spacing. They suggested that the ML-Fin arrays might be the foundation for upcoming ICs.

Trench ferroelectric FinFET (trench-Fe-FinFET), were fabricated and then described by Yan et al. (S.-C. Yan et al., 2022). After defining the fin shape, an extra etching was used to create the trench structure channel. The anatomy of the trench-Fe-FinFET is given in Fig.2.15.

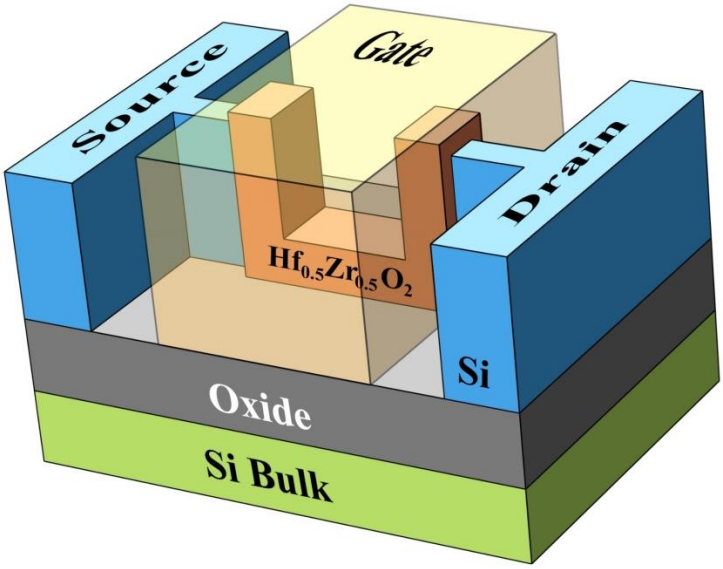


Fig.2.15: Anatomy of trench-Fe-FinFET

The electrical properties of the Fe-FinFETs were enhanced by adding the trench structures. Furthermore, SCEs were prevented by completely encircling the trench channel with the gate electrodes. The fabricated trench Fe-FinFET featured a steep minimum *SS* of 35.4 mV/dec in the forward sweep and a larger ON-OFF current ratio of $4.1x10^7$ than a standard Fe-FinFET. The constructed trench Fe-FinFET also had the flexibility to GIDL and a very low DIBL value of 4.47 mV/dec. The experimental findings were confirmed through a TCAD simulation. Trench Fe-FinFET fabrication techniques are amicable with those, generally used to make Si-CMOS electronics. As a result, the trench Fe-FinFET is a encouraging contender for 3-D stacked ICs and ultralow-power applications.

2.5.12. Application of germanium in FinFET

Ge n-channel FinFET operated in enhancement model was fabricated on a 300 mm Si wafer by van Dal et al. (van Dal et al., 2015). The device had trap density (D_{it}) below $2x10^{11}$ $eV^{-1}cm^{-2}$ and contact resistivity (ρ) $2x10^{-7}$ Ω cm^2. They proposed a circular transmission line ρ-extraction model that express the parasitic metal resistance. They have reported that, with 40 nm-gate-length FinFET, ON current is 50

A/m and OFF current is 100 nA/m, *SS* is around 124 mV/decade, and a peak g_m is 310 μS/μm, at $v_d = 0.5$ V.

To ensure the transistor is working under the ideal conditions, it is essential to identify its precise device parameter. The study conducted by Othman, N. A. F. and his companions, applied the Taguchi approach to design the device parameter of a Ge p-FinFET (Othman, Azhari, Hatta, & Soin, 2016). The Sentaurus Simulator was employed as the simulation and analysis tool for this work. Orthogonal arrays, the signal-to-noise ratio, and Pareto analysis of variance were used as the quality criterion of selections in the Taguchi technique to find the best set of variables for reliable device performance. The width, height, and length of the fin and its circumference at the top, were considered in the experimental design. Using these methods, the ON and OFF current were taken into account. Pareto analysis of variance and Taguchi's robust performance signal-to-noise ratio were used to combine parameters to produce a combination with a high ON-current and a low OFF-current. The best ON-current performance for p-FinFET is observed at values of 1.8847mA for fins with lengths of 8 nm, heights of 35nm, and widths of 7nm. On the other hand, a fin with dimensions of 15 nm in length, 25nm in height, and 2 nm in width can lead to the best OFF-current performance with a value of 26.7nA.

Thermoelectric measurements were used to examine the properties of thermal conductivity (k_c) at various operating temperatures (T), material thicknesses (t), and impurity concentrations (N). A simulation model was constructed to examine the self-heating effect. The constructed finite-element model allowed the researchers to precisely and methodically study the self-heating effect on the CMOS logic transistors from 20 to 5 nm technology nodes. As predicted by simulation, the Si FinFET device's thermal parameters were in good agreement with the experimental findings. It was reported that the Si FinFET device with 14/16nm technology node supported a maximum chip temperature of 170°C. The relationship between various physical parameters such as gate lengths, fin heights, fin pitches, and fin widths with the self-heating effect was studied for Si FinFET devices. It was also reported that due to the weak thermal conductivity and thermal properties of these high μ materials, the

operating chip temperature in the Ge and III-V (InAs) FinFET devices was more than it was in the Si FinFET device. It was therefore determined that these high μ materials were challenging to use in the scaled technology node devices of the next generation unless these devices function at the ultralow bias voltage (0.5V for InAs and 0.8V for Ge) (Liao, Hsieh, & Lee, 2017).

2.5.13. Application of FinFET

FinFET has been successfully implemented in SRAM, ring oscillator which have already been discussed in this review section. The other important application of FinFET in radio-frequency identification (RFID) and biomedical sector are conferred below.

Srinivasulu et al. suggested a T-flip-flop and Miller encoder system for RFID applications at ultra-high and super-high frequencies using FinFETs (Srinivasulu, Sravanthi, Sarada, & Pal, 2018). Miller encoders are utilized in RFID, optical domain, and magnetic recording. By setting up the model specifications of a 20 nm FinFET (obtained from open source) on the Cadence platform with a +0.4V supply rail at frequencies of 1, 2, and 10GHz, the performance of the suggested circuit was evaluated.

Inexact computation can be utilized for applications where performance and precision are less crucial. When power and speed are more important than precision, inexact multipliers are the preferred option. CMOS and FinFET based on two different multiplier designs were reported for this operation (Senthil Kumar & Ravindrakumar, 2019) Leakage current was decreased by the suggested FinFET-based multiplier circuit, which ultimately lowers power consumption. The proposed multiplier circuits' performance was improved by 40.61 %. A Multiply-Accumulate unit (MAC) based on FinFET will be suggested for future use in biomedical applications**.**

2.6. Summary

This chapter discusses the history, structural configuration and fabrication challenges of the FinFET. The manufacturing challenges such as doping, parasitic capacitance, fringing capacitance fin orientation, and shaping of fins are also

canvassed. It includes a compact literature review of FinFET over two decades. From 2002 to 2022 the major research works on modeling, fabrication techniques and the application of FinFET are summarized in detail. This study gives a vivid idea of the advantages of FinFET technology. Various reported research works explain the device's performance in terms of number of gates and different fin materials such as Si, Ge, InGaAs, InAs, GaAs, and SiGe. Hydrogen annealing, high-k spacer, SEG are suggested to refine the electrical properties. The application of high-k materials as a gate insulator is the most popular issue in semiconductor technology. According to literature, ZrO_2 and HfO_2 are the utmost encouraging high-k materials used in this technology. In light of this high-k material, the SCEs, namely, DIBL, SS, ON-OFF current ratio and GIDL have been discussed. Poisson's equation, Laplace equation are solved to model the electrical characteristics of the device. The conformal mapping technique is reported to model the parasitic capacitance. Researchers also suggest the modeling and improvement techniques of parasitic resistance. The influence of H_{fin} and W_{fin} on the electrical parameters are analysed by a few researchers. DESSIS form Sentaurus, ATLAS, Tiber CAD, and various well-accepted simulating tools are employed to verify the analytical models. The applications of the FinFET such as SRAM, ring oscillator, T-flipflop, and Miller encoders for RFID are also included in this review. Therefore, the FinFET technology has been established as a striking option for upcoming technology nodes. But the accurate modeling of electrical characteristics, including Φ, V_T, I_d, and trans-capacitance in short channel FinFET devices, still suffer from significant hurdles. FinFET has a 3-D structure; hence the solution of the complex 3-D Poisson's equation is the foremost hurdle to finding Φ the primary parameter for modeling any semiconductor device. Here, TG-FinFET is considered as the combination DG symmetric and asymmetric structure, i.e., 2-D structure. Therefore, the electrical characteristics and SCEs must be modelled more precisely to overcome the challenges of the current scenario and inspire to formulate the present research work.

CHAPTER - 3

Surface Potential and Electric Field

3.1. Introduction

Potential distribution in each point of the silicon channel is a technique to address all functionality of the transistor. The modeling of TG-FinFET based on the potential distribution faces two challenges:

1. Getting an exact picture of the coupling between the gates.
2. Estimation of the behaviour of the FinFET due to miniaturization.

The TG-FinFET is a combination of the symmetric and asymmetric DG-FinFETs. The parallel gates of the silicon fin form the symmetric DG-FinFET. In contrast, the top and bottom gates form the asymmetric DG-FinFET. The coupling between the gates in DG-FinFET produces maximum potential at the middle of the channel. So far, three approaches have been used to solve Poisson's formula of electrostatic potential in the multi-gated device. The Poisson's equation in the 2-D device such as DG-FinFET can be indicated as $\Phi(x, y)$. Several techniques are used to find out the variance of the potential along the channel.

In the first approach, the potential $\Phi(x, y)$ is represented by the product of $\Phi(x, y) = \Phi(x)\Phi(y)$ and then solved the Poisson's equation is solved in individual axis (Frank, Taur, & Wong, 1998; X. Liang & Taur, 2004). Fourier series is used to express the solution of the differential equations. The low-class series coefficients

provide an inaccurate solution whereas, large-class coefficients result in non-analytical and time-consuming solutions.

Gauss's law and special parameters are applied in the 2nd approach, to find out the electric field in the vertical axis. The results give the potential distribution at the boundary of the back and top gate (Green & Fossum, 1993; Z.-H. Liu et al., 1993). In the 3rd approach, a parabolic potential function is considered in the vertical axis to solve Poisson's equation and in this case, the solutions exclusively describe the potential dispersal at the top and back-gate boundaries (Chiang, 2004; J. Fossum et al., 2004; P. C. Yeh & Fossum, 1995; K. K. Young, 1989).

The Φ is modelled in the weak inversion condition. The undoped or a little doped channel is taken to reduce the haphazard dopant fluctuation. The Φ of the TG-FinFET is formulated by unfolding the 2-D Poisson's equation independently for two DG-FinFETs and then combining the solutions using the perimeter-weighted sum approach. This model is examined for two gate oxide materials namely SiO_2 and HfO_2. The model is inspected by varying the device geometry and it is confirmed with the TCAD simulation.

The schematic diagram of TG-FinFET is given in Fig.3.1.

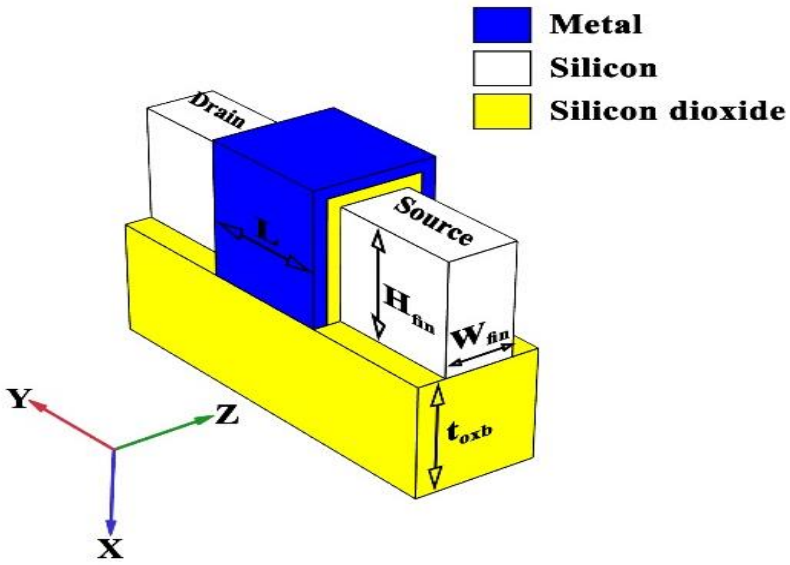
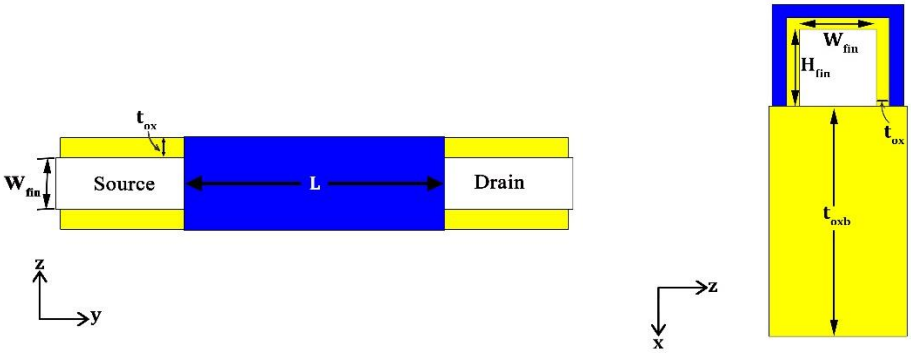


Fig.3.1: Structure of TG-FinFET

The bottom oxide thickness is indicated by t_{oxb} and it is considered as 100nm to ignore the effect of the back gate. The device is surrounded by the three gate electrodes with uniform t_{ox}.

The 2-D cross-sectional view of TG-FinFET in $(y-z)$ plane and $(x-z)$ plane is shown in Fig.3.2.



(a) (b)

Fig.3.2: Cross-sectional view of TG-FinFET along (a) y-z plane (b) x-z plane

3.2. Analytical Model of Surface Potential

As TG-FinFET is a combination of asymmetric and symmetric DG-FinFET. Thereby, Φ for symmetric DG-FinFET and asymmetric DG-FinFET are individually calculated and then merged to get the Φ of the TG-FinFET. The calculations are explained in the following sections-

3.2.1 Surface potential model for symmetric DG-FinFET

The symmetric DG-FinFET lies in the $y-z$ direction. The Φ is modelled in the ideal condition; hence, interface charge density and flat band voltage (v_{fb}) are considered to be zero. According to Poisson's equation, in a weak inversion condition, the potential distribution equation is (Tsormpatzoglou et al., 2007)

$$\frac{\partial^2\Phi(y,z)}{\partial y^2}+\frac{\partial^2\Phi(y,z)}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}} \tag{3.1}$$

here ε_{si} indicates permittivity of the material silicon. A parabolic equation is used to solve the aforesaid equation. Conferring with (K. K. Young, 1989) the distribution of potential is in the z axis, hence, the associated equation is represented as,

$$\Phi(y,z) = A_0(y) + A_1(y)z + A_2(y)z^2 \tag{3.2}$$

Because of the symmetric design, potential at the front-interface $(\Phi(y,0))$ and back-interface $(\Phi(y,W_{fin}))$ are assumed to be the same i.e., $\Phi_s(y) = \Phi(y,0) = \Phi(y,W_{\text{fin}})$. The coefficients A_0, A_1 and A_2 are the function of y . Using Gauss's formula, at channel and oxide interface the electric field's boundary conditions can be expressed as,

$$\frac{d\Phi(y,z)}{dz} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \left\{ \frac{\Phi_s(y) - v_g'}{t_{ox}} \right\} \text{ at } z = 0 \tag{3.3}$$

$$\frac{d\Phi(y,z)}{dz} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \left\{ \frac{v_g' - \Phi_s(y)}{t_{ox}} \right\} \text{ at } z = W_{fin} \tag{3.4}$$

Here, $v_g' = v_g - v_{fb}$, and the work function difference of metal-semiconductor is symbolized by ϕ_{ms} . To simplify the mathematical calculation the ϕ_{ms} is supposed to be zero. Therefore, in the ideal oxide semiconductor interface, the v_{fb} and the interface charge density both are also presumed to be zero. $v_{th} = \frac{KT}{q}$ is defined as the thermal voltage, v_g is applied at the side gates of the TG-FinFET and the insulator's permittivity is indicated by ε_{ox}. Putting $z = 0$ in equation (3.2), $\Phi_s = A_0$. Now, differentiating equation (3.2) with respect to z , will result,

$$\frac{d\Phi}{dz} = A_1 + 2A_2 z \tag{3.5}$$

Applying boundary condition (equation (3.3)), the equation (3.5) can be inscribed as,

$$A_1 = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right) \times \left(\frac{\Phi_s(y) - v_g'}{t_{ox}}\right) \tag{3.6}$$

Using the equation (3.4) and (3.6) A_2 can be calculated as,

$$A_2 = \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right) \times \left(\frac{v_g' - \Phi_s}{t_{ox} W_{fin}}\right) \tag{3.7}$$

Hence, using the value of A_0, A_1 and A_2 in equation (3.2), the equation reduces to

$$\Phi(y,z) = \Phi_s + \left\{\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\Phi_s(y) - v_g'}{t_{ox}}\right)\right\} z + \left\{\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{v_g' - \Phi_s(y)}{t_{ox} W_{fin}}\right)\right\} z^2 \tag{3.8}$$

Now, considering $a = \varepsilon_{ox}/\varepsilon_{si} t_{ox}$, $b = -\left(\varepsilon_{ox} v_g' / \varepsilon_{si} t_{ox}\right)$, $c = -\left(\varepsilon_{ox}/W_{fin} t_{ox} \varepsilon_{si}\right)$, $d = \left(\varepsilon_{ox} v_g' / W_{fin} t_{ox} \varepsilon_{si}\right)$ and $e_1 = qN_A/\varepsilon_{si}$, equation (3.8) reduces to

$$\Phi(y,z) = \Phi_s(y) + \left\{a\Phi_s(y) + b\right\} z + \left\{c\Phi_s(y) + d\right\} z^2 \tag{3.9}$$

Double differentiation of equation (3.9) with respect to z results equation (3.10) which gives,

$$\frac{\partial^2 \Phi(y,z)}{\partial z^2} = 2\left\{c\Phi_s(y) + d\right\} \tag{3.10}$$

Likewise, double differentiation of equation (3.9) with respect to y gives,

$$\frac{\partial^2 \Phi(y,z)}{\partial y^2} = \left(1 + az + cz^2\right)\left(\frac{d^2\Phi_s}{dy^2}\right) \tag{3.11}$$

Now, using the equation (3.10) and (3.11), Poisson's equation (3.1) will become,

$$\left(1 + az + cz^2\right)\frac{d^2\Phi_s}{dy^2} + 2\left(c\Phi_s + d\right) = e_1$$

$$\text{or, } \frac{d^2\Phi_s}{dy^2} + \left(\frac{2c}{1 + az + cz^2}\right)\Phi_s = \left(\frac{e_1}{1 + az + cz^2}\right) - \left(\frac{2d}{1 + az + cz^2}\right) \tag{3.12}$$

Let, $\alpha = -\left\{2c/\left(1+az+cz^2\right)\right\}$ and $\beta = \left\{e_1/\left(1+az+cz^2\right)\right\} - \left\{2d/\left(1+az+cz^2\right)\right\}$.

Hence, equation (3.12) can be written as,

$$\frac{d^2\Phi_s}{dy^2} - \alpha\Phi_s = \beta \tag{3.13}$$

Using the values of a, c, d and e_1, the values of α and β will be,

$$\alpha = \left\{2\varepsilon_{ox}/\left(W_{fin}t_{ox}\varepsilon_{si} + \varepsilon_{ox}W_{fin}z - \varepsilon_{ox}z^2\right)\right\} \tag{3.14}$$

and

$$\beta = \left\{\left(qN_AW_{fin}t_{ox} - 2\varepsilon_{ox}v_g^{'}\right)/\left(W_{fin}t_{ox}\varepsilon_{si} + \varepsilon_{ox}W_{fin}z - \varepsilon_{ox}z^2\right)\right\} \tag{3.15}$$

Now, to solve the equation (3.13), let us consider $\Phi_s = e^{my}$,

$$\therefore \frac{d^2\Phi_s}{dy^2} = m^2e^{my} \tag{3.16}$$

Therefore, the auxiliary equation will be,

$$(m^2 - \alpha)e^{my} = 0 \tag{3.17}$$

As $e^{my} \neq 0$, therefore, $m = \pm\sqrt{\alpha}$. Hence, the complementary solution of equation (3.16) is,

$$\Phi_s = BB_1e^{y\sqrt{\alpha}} + BB_2e^{-y\sqrt{\alpha}} \tag{3.18}$$

Ignoring the higher order terms, particular integral of the equation (3.16) is given below:

$$\Phi_s(y) = \frac{\beta}{D^2 - \alpha} = -\frac{\beta}{\alpha}\left(1 + \frac{D^2}{\alpha} + ...\right) = -\frac{\beta}{\alpha} \tag{3.19}$$

Using (3.18) and (3.19), the complete solution will be,

$$\Phi_s(y) = BB_1\left(e^{y\sqrt{\alpha}}\right) + BB_2\left(e^{-y\sqrt{\alpha}}\right) - \frac{\beta}{\alpha} \tag{3.20}$$

Appling the boundary conditions i.e., on $y = 0$, $\Phi_s = v_{bi}$ (built in potential) and on $y = L$, $\Phi_s = v_{bi} + v_d$ in equation (3.20), $\Phi_s(y)$ can be written as,

$$v_{bi} = BB_1 + BB_2 - \frac{\beta}{\alpha} \text{ ; at } y = 0$$

or, $$BB_1 + BB_2 = v_{bi} + \frac{\beta}{\alpha} \tag{3.21}$$

and at $y = L$,

$$v_{bi} + v_d = BB_1 e^{L\sqrt{\alpha}} + BB_2 e^{-L\sqrt{\alpha}} - \frac{\beta}{\alpha} \tag{3.22}$$

Let $aa_1 = v_{bi} + \frac{\beta}{\alpha}$, $aa_2 = v_{bi} + v_d + \frac{\beta}{\alpha}$, $aa_3 = e^{L\sqrt{\alpha}}$ and $aa_4 = e^{-L\sqrt{\alpha}}$. Hence, from equation (3.21), we can write, $BB_1 = aa_1 - BB_2$. Equation (3.22) can be written as,

$$aa_2 = aa_3 BB_1 + aa_4 BB_2 \tag{3.23}$$

Putting the value of BB_1, aa_2, aa_3 and aa_4 in equation (3.23), BB_2 will be,

$$BB_2 = \left(\frac{1}{1 - e^{2L\sqrt{\alpha}}}\right) \times \left\{ e^{L\sqrt{\alpha}}\left(v_{bi} + v_d + \frac{\beta}{\alpha}\right) - e^{2L\sqrt{\alpha}}\left(v_{bi} + \frac{\beta}{\alpha}\right)\right\} \tag{3.24}$$

Consequently,

$$BB_1 = \left(\frac{1}{1 - e^{2L\sqrt{\alpha}}}\right) \times \left\{ \left(v_{bi} + \frac{\beta}{\alpha}\right) - e^{L\sqrt{\alpha}}\left(v_{bi} + v_d + \frac{\beta}{\alpha}\right)\right\} \tag{3.25}$$

Now, using the values of BB_1, BB_2 and rearranging equation (3.20), $\Phi_s(y)$ will be,

$$\Phi_s(y) = \left(\frac{1}{e^{2L/\lambda_1} - 1}\right) \begin{Bmatrix} \left(v_{bi} + v_d - AA_1\right)\left(e^{(L+y)/\lambda_1} - e^{(L-y)/\lambda_1}\right) \\ + \left(v_{bi} - AA_1\right)\left(e^{(2L-y)/\lambda_1} - e^{y/\lambda_1}\right) + AA_1\left(e^{2L/\lambda_1} - 1\right) \end{Bmatrix} \tag{3.26}$$

where, $\lambda_1 = \frac{1}{\sqrt{\alpha}} = \sqrt{\frac{\left(\varepsilon_{si} W_{fin} t_{ox} + \varepsilon_{ox} W_{fin} z - \varepsilon_{ox} z^2\right)}{2\varepsilon_{ox}}}$ and

$$AA_1 = \frac{\beta}{\alpha} = \left\{ \frac{\left(qN_A W_{fin} t_{ox} - 2v_g^{'} \varepsilon_{ox}\right)\left(\varepsilon_{si} W_{fin} t_{ox} + \varepsilon_{ox} W_{fin} z - \varepsilon_{ox} z^2\right)}{2\varepsilon_{ox}\left(\varepsilon_{si} W_{fin} t_{ox} + \varepsilon_{ox} W_{fin} z - \varepsilon_{ox} z^2\right)} \right\}$$

At $z = 0$, $\lambda_1 = \sqrt{\left(\varepsilon_{si} W_{fin} t_{ox}\right) / 2\varepsilon_{ox}}$. Hence, the Φ at $z = 0$ will become $\Phi_s(y,0) = \Phi_s(y)$. Now, to obtain the variation of Φ along the z direction equation (3.8), is written as $\Phi(y,z) = \Phi_z$. Therefore, $\Phi_z = \Phi_s + \left(z \frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{\Phi_s - v_g^{'}}{t_{ox}}\right) + \left(z^2 \frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\left(\frac{v_g^{'} - \Phi_s}{W_{fin} t_{ox}}\right)$. Now, z is replaced by $\frac{W_{fin}}{n}$, where n is the integer number. Hence, the above equation will reduce to

$$\Phi_s = \left(\frac{\Phi_z}{1 + aa_5}\right) - \left(\frac{aa_6}{1 + aa_5}\right) v_g^{'} \tag{3.27}$$

where, $aa_5 = \left\{\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\left(\frac{W_{fin}}{n}\right)\right\} - \left\{\frac{\varepsilon_{ox}}{\varepsilon_{si} W_{fin} t_{ox}}\left(\frac{W_{fin}}{n}\right)^2\right\} = \left(\frac{\varepsilon_{ox} W_{fin}}{\varepsilon_{si} t_{ox} n^2}\right)(n-1)$ (3.28)

$$aa_6 = \left\{\frac{\varepsilon_{ox}}{\varepsilon_{si} W_{fin} t_{ox}}\left(\frac{W_{fin}}{n}\right)^2\right\} - \left\{\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\left(\frac{W_{fin}}{n}\right)\right\} = \left(\frac{\varepsilon_{ox} W_{fin}}{n^2 \varepsilon_{si} t_{ox}}\right)(1-n) \tag{3.29}$$

Let, $\frac{1}{1 + aa_5} = aa_7$ and $aa_8 = \left(\frac{aa_6}{1 + aa_5}\right)$. Hence, (3.27) can be written as,

$$\Phi_s(y) = \Phi_s = aa_7 \Phi_z(y) - aa_8 v_g^{'} \tag{3.30}$$

Now putting the value of $\Phi_s(y)$ in equation (3.13), will give,

$$aa_7\left(\frac{d^2 \Phi_z}{dy^2}\right) - \alpha aa_7 \Phi_z - \alpha aa_8 v_g^{'} = \beta \tag{3.31}$$

Therefore,

$$\frac{d^2\Phi_z}{dy^2} - \alpha\Phi_z = \frac{\beta + \alpha a a_8 v_g'}{a a_7} \tag{3.32}$$

Let, at $z = W_{fin}/n$, $\beta' = \left(\beta + \alpha a a_8 v_g'\right)/a a_7$ and α becomes α', it will be,

$$\alpha' = \frac{2\varepsilon_{ox}}{W_{fin} t_{ox} \varepsilon_{si} + \varepsilon_{ox}\left(\frac{W_{fin}^2}{n}\right) - \varepsilon_{ox}\left(\frac{W_{fin}}{n}\right)^2} \tag{3.33}$$

Let,

$$\lambda_2 = \frac{1}{\sqrt{\alpha'}} = \sqrt{\frac{1}{2\varepsilon_{ox}}\left\{\varepsilon_{si} W_{fin} t_{ox} + \varepsilon_{ox}\left(\frac{W_{fin}^{\ 2}}{n}\right) - \varepsilon_{ox}\left(\frac{W_{fin}}{n}\right)^2\right\}} \tag{3.34}$$

and

$$AA_2 = \frac{\beta'}{\alpha'} = -\frac{1}{2 a a_7 \varepsilon_{ox}}\left\{2\varepsilon_{ox}\left(1 - a a_8\right) v_g' - q N_A W_{fin} t_{ox}\right\} \tag{3.35}$$

Now, to get the distribution of the Φ in terms of z, n is substituted by $\frac{W_{fin}}{z}$, in that case, λ_2 is replaced by λ_{sym} and AA_2 is replaced by A_{sym}. Therefore,

$$A_{sym} = -\left\{v_g' - \left\{\left(\frac{qN_A}{2\varepsilon_{ox}\varepsilon_{si}}\right)\left\{\varepsilon_{si} t_{ox} W_{fin} + \varepsilon_{ox}\left(W_{fin} - z\right) z\right\}\right\}\right\} \tag{3.36}$$

and

$$\lambda_{sym} = \left\{\left(\frac{\varepsilon_{si} W_{fin} t_{ox}}{2\varepsilon_{ox}}\right)\left(1 + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\right) z - \left(\frac{\varepsilon_{ox}}{\varepsilon_{si} W_{fin} t_{ox}}\right) z^2\right)\right\}^{1/2} \tag{3.37}$$

Therefore, the symmetric DG-FinFET's Φ will become,

$$\Phi\left(\mathrm{y},\mathrm{z}\right)=\Phi_{sym}=\left(\frac{1}{e^{2L/\lambda_{sym}}-1}\right)\begin{Bmatrix}\left(v_{bi}+v_d-A_{sym}\right)\left(e^{(L+y)/\lambda_{sym}}-e^{(L-y)/\lambda_{sym}}\right)\\+\left(v_{bi}-A_{sym}\right)\left(e^{(2L-y)/\lambda_{sym}}-e^{y/\lambda_{sym}}\right)+A_{sym}\left(e^{2L/\lambda_{sym}}-1\right)\end{Bmatrix} \tag{3.38}$$

SCEs is measured by λ_{sym} which is the λ of the symmetric device. This also affects the subthreshold current and above-threshold current because of the additional potential created within the silicon layer by the SCEs. In the long channel device, the potential is considered to be constant throughout the channel and it is equal to A_{sym} for symmetric DG-FinFET. Therefore, the extra potential for symmetrical device $\left(\Delta\Phi_{sym}\right)$ due to the SCEs can be written as,

$$\Delta\Phi_{sym}=\Phi_{sym}(y,z)-A_{sym} \tag{3.39}$$

Now, if we replace $\Phi_{sym}(y,z)$ by equation (3.38), then the $\Delta\Phi_{sym}$ will be,

$$\Delta\Phi\left(\mathrm{y},\mathrm{z}\right)=\Delta\Phi_{sym}=\left(\frac{1}{e^{2L/\lambda_{sym}}-1}\right)\begin{Bmatrix}\left(v_{bi}+v_d-A_{sym}\right)\left(e^{(L+y)/\lambda_{sym}}-e^{(L-y)/\lambda_{sym}}\right)\\+\left(v_{bi}-A_{sym}\right)\left(e^{(2L-y)/\lambda_{sym}}-e^{y/\lambda_{sym}}\right)\end{Bmatrix} \tag{3.40}$$

3.2.2 Surface potential model for asymmetric DG-FinFET

The asymmetrical structure of DG-FinFET is oriented on the x, y plane, consist of a top and back gate. In connection with of asymmetric DG-FinFET, the top and the back gate are at different potentials. The back gate potential is v_{sub} . Therefore, using the similar kind of parabolic function as used for symmetric DG-FinFET, the potential distribution in the x direction will be,

$$\Phi(x,y)=P_0\left(y\right)+P_1\left(y\right)x+P_2\left(y\right)x^2 \tag{3.41}$$

Assuming that, $\Phi\left(x,y\right)=\Phi\left(0,y\right)=\Phi_{sf}\left(y\right)$ and $\Phi\left(x,y\right)=\Phi\left(H_{fin},y\right)=\Phi_{sb}\left(y\right)$ on $x=H_{fin}$, therefore, the boundary conditions will become,

$$\frac{d\Phi(x,y)}{dx}=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\times\left\{\frac{\Phi_{sf}(y)-v_g^{'}}{t_{ox}}\right\}\text{ at }x=0 \tag{3.42}$$

$$\frac{d\Phi(x,y)}{dx}=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\times\left\{\frac{v_{sub}-\Phi_{sb}(y)}{t_{oxb}}\right\}\text{at }x=H_{fin} \tag{3.43}$$

Applying the boundary conditions and equation (3.41) return $\Phi(x,y)=\Phi_{sf}(y)=P_0$.

The differentiation of equation (3.41) with respect to x gives,

$$\frac{d\Phi(x,y)}{dx}=P_1+2P_2x \tag{3.44}$$

In the above equation, $\frac{d\Phi(x,y)}{dx}$ is replaced by equation (3.42), hence,

$$P_1=\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\frac{\Phi_{sf}(y)-v_g^{'}}{t_{ox}}=bb_1\Phi_{sf}(y)-bb_2 \tag{3.45}$$

where, $bb_1=\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}$ and $bb_2=\frac{\varepsilon_{ox}v_g^{'}}{\varepsilon_{si}t_{ox}}$. Similarly, at $x=H_{fin}$, we can get P_2 as,

$$P_2=\frac{1}{2H_{fin}}\left\{(bb_3+bb_2)-bb_4\Phi_{sb}(y)-bb_1\Phi_{sf}(y)\right\} \tag{3.46}$$

where, $bb_3=\frac{\varepsilon_{ox}v_{sub}}{\varepsilon_{si}t_{oxb}}$ and $bb_4=\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxb}}$. At $x=H_{fin}$, $\Phi(x,y)=\Phi(H_{fin},y)=\Phi_{sb}(y)$.

Consequently,

$$\Phi_{sb}=bb_5\Phi_{sf}+bb_6 \tag{3.47}$$

where, $bb_5=\frac{2+bb_1H_{fin}}{2+bb_4H_{fin}}$ and $bb_6=\frac{H_{fin}(bb_3-bb_2)}{2+H_{fin}bb_4}$.

Now, the double derivative of equation (3.41) with respect to x, provides,

$$\frac{\delta^2\Phi(x,y)}{\delta x^2}=\frac{1}{H_{fin}}\left[(bb_3+bb_2)-(bb_1+bb_4bb_5)\Phi_{sf}(y)-bb_4bb_6\right] \tag{3.48}$$

Likewise, the 2nd order derivative of equation (3.41) with respect to y, will give,

$$\frac{\partial^2\Phi(x,y)}{\partial y^2}=\left(1+bb_1x-\frac{bb_1x^2}{2H_{fin}}-\frac{bb_4bb_5x^2}{2H_{fin}}\right)\frac{\partial^2\Phi_{sf}}{\partial y^2}=bb_7\frac{\partial^2\Phi_{sf}}{\partial y^2} \tag{3.49}$$

where, $bb_7=\left(1+bb_1x-\frac{bb_1x^2}{2H_{fin}}-\frac{bb_4bb_5x^2}{2H_{fin}}\right)$. Hence, the Poisson's equation will be,

$$\frac{\partial^2\Phi_{sf}}{\partial y^2}-\frac{(bb_1+bb_4bb_5)}{bb_7H_{fin}}\Phi_{sf}=\frac{qN_A}{bb_7\varepsilon_{si}}-\frac{(bb_3+bb_2)}{bb_7H_{fin}}+\frac{bb_4bb_6}{bb_7H_{fin}}$$

or, $$\frac{\partial^2\Phi_{sf}}{\partial y^2}-\delta\Phi_{sf}=\theta \tag{3.50}$$

Let, $\delta=\frac{bb_4bb_5+bb_1}{H_{fin}bb_7}$. Now using the values of bb_5, bb_4, bb_1, bb_7, the precise value of δ as,

$$\delta=\frac{2\varepsilon_{ox}\left\{\varepsilon_{si}(t_{ox}+t_{oxb})+\varepsilon_{ox}H_{fin}\right\}}{2\varepsilon_{si}^2t_{oxb}t_{ox}H_{fin}+\varepsilon_{ox}^2H_{fin}(H_{fin}-x)x+\varepsilon_{ox}\varepsilon_{si}\left\{\begin{matrix}t_{oxb}(2H_{fin}-x)x\\+t_{ox}(H_{fin}^2-x^2)\end{matrix}\right\}} \tag{3.51}$$

Similarly, let, $\theta=\frac{qN_A}{\varepsilon_{si}bb_7}-\frac{bb_3+bb_2}{bb_7H_{fin}}+\frac{bb_4bb_6}{bb_7H_{fin}}$. Using the values of the constants, θ will be,

$$\theta=\frac{\begin{matrix}2\left(\frac{qN_A}{\varepsilon_{si}}\right)H_{fin}+\left(\frac{qN_A}{\varepsilon_{si}}\right)H_{fin}^2\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxb}}\right)-2\left(\frac{\varepsilon_{ox}v_{sub}}{\varepsilon_{si}t_{oxb}}\right)-2\left(\frac{\varepsilon_{ox}v_g'}{\varepsilon_{si}t_{ox}}\right)\\-2H_{fin}\left(\frac{\varepsilon_{ox}v_g'}{\varepsilon_{si}t_{ox}}\right)\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxb}}\right)\end{matrix}}{\begin{matrix}2H_{fin}+H_{fin}^2\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxb}}\right)+2\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)H_{fin}x+H_{fin}^2\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxb}}\right)\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)x\\-\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxb}}\right)x^2-\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)H_{fin}x^2-\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)x^2\end{matrix}}$$

$$\text{or, } \theta = \frac{-\varepsilon_{ox} H_{fin}\left(2\varepsilon_{ox} v_g^{'} - bb_8\right) - 2\varepsilon_{si}\left\{\varepsilon_{ox}\left(t_{oxb} v_g^{'} + t_{ox} v_{sub}\right) - bb_8 t_{oxb}\right\}}{bb_9 + \varepsilon_{ox}^2 H_{fin}\left(H_{fin} - x\right)x + \varepsilon_{ox}\varepsilon_{si}\left\{t_{oxb}\left(2H_{fin} - x\right)x + t_{ox}\left(H_{fin}^2 - x^2\right)\right\}} \quad (3.52)$$

Here, $bb_8 = qN_A t_{ox} H_{fin}$ and $bb_9 = 2\varepsilon_{si}^2 t_{oxb} t_{ox} H_{fin}$. Now, let us consider $\Phi_{sf} = e^{my}$ and the equation (3.50) will be solved as,

$$\therefore \frac{d^2\Phi_s}{dy^2} = m^2 e^{my} \quad (3.53)$$

Hence, the auxiliary equation will be,

$$(m^2 - \alpha)e^{my} = 0 \quad (3.54)$$

As $e^{my} \neq 0$, therefore, $m = \pm\sqrt{\delta}$. Hence, the complementary solution of equation (3.54) is,

$$\Phi_{sf} = C_1 e^{y\sqrt{\delta}} + C_2 e^{-y\sqrt{\delta}} \quad (3.55)$$

Overlooking the higher-order terms, a particular integral of the equation (3.50) is given below:

$$\Phi_{sf}(y) = \frac{\theta}{D^2 - \delta} = -\frac{\theta}{\delta}\left(1 + \frac{D^2}{\delta} + ...\right) = -\frac{\theta}{\delta} \quad (3.56)$$

Using (3.55) and (3.56), the complete solution will be,

$$\Phi_{sf}\left(y\right) = C_1\left(e^{y\sqrt{\alpha}}\right) + C_2\left(e^{-y\sqrt{\alpha}}\right) - \frac{\theta}{\delta} \quad (3.57)$$

Now, the boundary conditions are used to calculate C_1 and C_2. By, keeping the similarity with the symmetric FinFET, the asymmetric FinFET's Φ will become,

$$\Phi_{sf}\left(y\right) = \left\{\frac{1}{e^{2L\sqrt{\delta}} - 1}\right\} \times \left\{\begin{array}{l} \left(v_{bi} + v_d + \frac{\theta}{\delta}\right)\left(e^{(L+y)\sqrt{\delta}} - e^{(L-y)\sqrt{\delta}}\right) \\ + \left(v_{bi} + \frac{\theta}{\delta}\right)\left(e^{(2L-y)\sqrt{\delta}} - e^{y\sqrt{\delta}}\right) - \frac{\theta}{\delta}\left(e^{2L\sqrt{\delta}} - 1\right) \end{array}\right\} \quad (3.58)$$

The distribution of Φ in the x direction is represented by Φ_x which can be obtained by putting the values of P_0, P_1 and P_2 in equation (3.41) and it will be,

$$\Phi_x = \Phi_{sf} + x\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\frac{\Phi_{sf} - v_g^{'}}{t_{ox}} + \frac{x^2}{2H_{fin}}\left\{\left(bb_2 + bb_3\right) - bb_4\Phi_{sb} - bb_1\Phi_{sf}\right\} \tag{3.59}$$

Now, by replacing the value of Φ_{sb} from equation (3.47), we can write,

$$\Phi_x = \Phi_{sf}\left(1 + x\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}} - bb_4bb_5\frac{x^2}{2H_{fin}} - bb_1\frac{x^2}{2H_{fin}}\right) - \left\{\begin{matrix} x\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)v_g^{'} - \frac{x^2}{2H_{fin}} \\ \left(bb_2 + bb_3 - bb_4bb_6\right)\end{matrix}\right\}$$

Hence, from the above equation Φ_{sf} can be written as follows-

$$\Phi_{sf} = \frac{\Phi_x}{bb_{11}} + \frac{bb_{10}}{bb_{11}} \tag{3.60}$$

Here, $bb_{10} = \left\{x\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)v_g^{'} - \frac{x^2}{2H_{fin}}\left(bb_2 + bb_3 - bb_4bb_6\right)\right\}$

and $bb_{11} = 1 + x\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right) - bb_4bb_5\left(\frac{x^2}{2H_{fin}}\right) - bb_1\left(\frac{x^2}{2H_{fin}}\right)$

Now, x is replaced by H_{fin}/n, thereby the above constants are reduced to,

$$bb_{10} = \left\{\frac{H_{fin}}{n}\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)v_g^{'} - \frac{H_{fin}}{2n^2}\left(bb_2 + bb_3 - bb_4bb_6\right)\right\}$$

and $bb_{11} = 1 + \frac{H_{fin}}{n}\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right) - \frac{H_{fin}}{2n^2}\left(bb_4bb_5 + bb_1\right)$

Applying the value of Φ_{sf} in the equation (3.50), will result,

$$\frac{d^2\Phi_x}{dy^2} - \delta\Phi_x = \theta_1 \tag{3.61}$$

where, $\theta_1 = bb_{11}\theta + bb_{10}\delta$. θ_1 is obtained by replacing n by H_{fin}/x and using the values of the constants. Finally, A_{asym} is calculated by θ_1/δ. Therefore, A_{asym} becomes,

$$A_{asym} = \frac{\theta_1}{\delta} = \frac{\varepsilon_{si}\left(\varepsilon_{ox}t_{oxb}v_g^{'} + \varepsilon_{ox}t_{ox}v_{sub} - qN_A t_{oxb}t_{ox}H_{fin}\right)}{\varepsilon_{ox}\left\{\varepsilon_{si}\left(t_{oxb}+t_{ox}\right)+\varepsilon_{ox}H_{fin}\right\}}$$
$$-\frac{qN_A\varepsilon_{ox}H_{fin}x\left(H_{fin}-x\right)}{2\varepsilon_{si}\left\{\varepsilon_{si}\left(t_{oxb}+t_{ox}\right)+\varepsilon_{ox}H_{fin}\right\}} \qquad (3.62)$$
$$+\frac{2\varepsilon_{ox}H_{fin}v_g^{'} - 2\varepsilon_{ox}x\left(v_g^{'}-v_{sub}\right) - qN_A t_{oxb}x\left(2H_{fin}-x\right) - qN_A t_{ox}\left(H_{fin}^2 - x^2\right)}{2\left\{\varepsilon_{si}\left(t_{oxb}+t_{ox}\right)+\varepsilon_{ox}H_{fin}\right\}}$$

and $\lambda_{asym} = \sqrt{1/\delta}$ is,

$$\lambda_{asym} = \sqrt{\frac{2\varepsilon_{si}^2 t_{oxb}t_{ox}H_{fin} + \varepsilon_{ox}^2 H_{fin}\left(H_{fin}-x\right)x + \varepsilon_{ox}\varepsilon_{si}\left\{\begin{matrix} t_{oxb}\left(2H_{fin}-x\right)x \\ +t_{ox}\left(H_{fin}^2 - x^2\right)\end{matrix}\right\}}{2\varepsilon_{ox}\left\{\varepsilon_{si}\left(t_{ox}+t_{oxb}\right)+\varepsilon_{ox}H_{fin}\right\}}} \qquad (3.63)$$

The preceding equation is simplified using a few arithmetic steps and λ_{asym} will finally be,

$$\lambda_{asym} = \left\{\frac{\varepsilon_{si}t_{ox}H_{fin}}{2\varepsilon_{ox}} \times \left\{\begin{matrix} \dfrac{2\varepsilon_{si}t_{oxb}+\varepsilon_{ox}H_{fin}}{\varepsilon_{si}\left(t_{ox}+t_{oxb}\right)+\varepsilon_{ox}H_{fin}} \\ +\left(\dfrac{x\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\right)\dfrac{\left(2\varepsilon_{si}t_{oxb}+\varepsilon_{ox}H_{fin}\right)}{\varepsilon_{si}\left[\left(t_{ox}+t_{oxb}\right)+\varepsilon_{ox}H_{fin}\right]} - \dfrac{\varepsilon_{ox}x^2}{\varepsilon_{si}t_{ox}H_{fin}}\end{matrix}\right\}\right\}^{\frac{1}{2}} \qquad (3.64)$$

Therefore, Φ of the asymmetric DG-FinFET becomes,

$$\Phi\left(x,y\right) = \Phi_{asym} = \left\{\frac{1}{e^{2L/\lambda_{asym}}-1}\right\} \times$$
$$\left\{\begin{matrix} \left(v_{bi}+v_d-A_{asym}\right)\left(e^{(L+y)/\lambda_{asym}} - e^{(L-y)/\lambda_{asym}}\right) + \left(v_{bi}-A_{asym}\right) \\ \left(e^{(2L-y)/\lambda_{asym}} - e^{y/\lambda_{asym}}\right) + A_{asym}\left(e^{2L/\lambda_{asym}}-1\right)\end{matrix}\right\} \qquad (3.65)$$

Now, here λ_{asym} is the λ of the asymmetric device and this will also be a metric of SCEs in asymmetric DG-FinFET. Considering the similar trend as explained in symmetric DG-FinFET, the extra potential developed in the asymmetric DG-FinFET $\left(\Delta\Phi_{asym}\right)$ can be expressed as,

$$\Delta\Phi_{asym} = \Phi_{asym}(x,y) - A_{asym} \tag{3.66}$$

Here, λ_{asym} is considered to be the potential of the long channel asymmetric DG-FinFET and it is constant throughout the channel. $\Phi_{asym}\left(x,y\right)$ is replaced by equation (3.65), the expression for $\Delta\Phi_{asym}$ becomes,

$$\Delta\Phi_{asym} = \left\{\frac{1}{e^{2L/\lambda_{asym}}-1}\right\}\left\{\begin{array}{l}\left(v_{bi}+v_d-A_{asym}\right)\left(e^{(L+y)/\lambda_{asym}}-e^{(L-y)/\lambda_{asym}}\right)\\ +\left(v_{bi}-A_{asym}\right)\left(e^{(2L-y)/\lambda_{asym}}-e^{y/\lambda_{asym}}\right)\end{array}\right\} \tag{3.67}$$

3.2.3 Surface potential model for TG-FinFET

The Φ of the TG-FinFET is determined using the perimeter weighted sum approach, that was previously employed in surround gate MOSFET (C. P. Auth & Plummer, 1998). As a result, the TG-FinFET's potential distribution will be,

$$\Phi\left(x,y,z\right) = \Phi_{asym}\left(x,y\right)\times\left\{\frac{W_{fin}}{W_{fin}+2H_{fin}}\right\} + \Phi_{sym}\left(y,z\right)\times\left\{\frac{2H_{fin}}{W_{fin}+2H_{fin}}\right\} \tag{3.68}$$

In this instance, the width of the symmetric DG-FinFET is H_{fin} and its contribution to the total perimeter will be indicated by $\frac{2H_{fin}}{(2H_{fin}+W_{fin})}$. Similarly, the asymmetric DG-FinFET possess a width of W_{fin} contributes $\frac{W_{fin}}{(2H_{fin}+W_{fin})}$ to the total perimeter. The crystal orientation of the top channel and side walls has a sever effect the μ and it has been modelled by perimeter weighted sum method. This model has also been validated by experimental result (Collaert, Dixit, et al., 2005).

To avoid the interaction among the side gates and the bottom gate which are at a different potential, the bottom oxide t_{oxb} is taken as 100 nm i.e., $t_{oxb} > L$. According to Colinge's (Jean-Pierre Colinge, 2004) conclusion the physical length of SR a device with square section may be calculated by dividing the physical length of the 2G device by the square root of 2. As a result, both DG-FinFETs' the natural lengths are reduced by a factor of square root of 2 to generate the λ of the TG-FinFET. So, the improved natural lengths are given below:

$$\lambda_{sym} = \sqrt{\left(\frac{\varepsilon_{si} W_{fin} t_{ox}}{4}\right) \times \left\{\frac{1}{\varepsilon_{ox}} + \frac{z}{\varepsilon_{si} t_{ox}} - \frac{z^2}{\varepsilon_{si} W_{fin} t_{ox}}\right\}} \tag{3.69}$$

$$\lambda_{asym} = \left\{\frac{\varepsilon_{si} t_{ox} H_{fin}}{4\varepsilon_{ox}} \times \left\{\begin{array}{l} \dfrac{2\varepsilon_{si} t_{oxb} + \varepsilon_{ox} H_{fin}}{\varepsilon_{si}\left(t_{ox} + t_{oxb}\right) + \varepsilon_{ox} H_{fin}} + \\ \dfrac{x\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} \dfrac{\left(2\varepsilon_{si} t_{oxb} + \varepsilon_{ox} H_{fin}\right)}{\varepsilon_{si}\left[\left(t_{ox} + t_{oxb}\right) + \varepsilon_{ox} H_{fin}\right]} - \dfrac{\varepsilon_{ox} x^2}{\varepsilon_{si} t_{ox} H_{fin}} \end{array}\right\}\right\}^{\frac{1}{2}} \tag{3.70}$$

Now from equations (3.69) and (3.70), it can be observed that in both the cases, the natural lengths are the function of channel depth and geometric characteristics of the FET. Hence for TG-FinFET, an extra potential $\left(\Delta\Phi_m\right)$developed in the channel can also be calculated by combining both DG-FinFETs' extra potential employing the perimeter-weighted sum method. The calculation is given below:

$$\Delta\Phi_m = \frac{W_{fin}}{W_{fin} + 2H_{fin}} \Delta\Phi_{sym} + \frac{2H_{fin}}{W_{fin} + 2H_{fin}} \Delta\Phi_{asym}$$

$$\Delta\Phi_m = \frac{W_{fin}}{W_{fin}+2H_{fin}}\left(\frac{1}{e^{2L/\lambda_{asym}}-1}\right)\left\{\begin{matrix}\left(v_{bi}+v_d-A_{asym}\right)\left(\begin{matrix}e^{(L+y)/\lambda_{asym}}\\-e^{(L-y)/\lambda_{asym}}\end{matrix}\right)\\+\left(v_{bi}-A_{asym}\right)\left(\begin{matrix}e^{(2L-y)/\lambda_{asym}}\\-e^{y/\lambda_{asym}}\end{matrix}\right)\end{matrix}\right\}$$

or,

$$+\frac{2H_{fin}}{W_{fin}+2H_{fin}}\left(\frac{1}{e^{2L/\lambda_{sym}}-1}\right)\left\{\begin{matrix}\left(v_{bi}+v_d-A_{sym}\right)\left(\begin{matrix}e^{(L+y)/\lambda_{sym}}\\-e^{(L-y)/\lambda_{sym}}\end{matrix}\right)\\+\left(v_{bi}-A_{sym}\right)\left(\begin{matrix}e^{(2L-y)/\lambda_{sym}}\\-e^{y/\lambda_{sym}}\end{matrix}\right)\end{matrix}\right\} \quad (3.71)$$

3.2.4 Electric field model for TG-FinFET

The electric field within the channel is deduced by differentiating $\Phi(x,y,z)$ prescribed in equation (3.68) with respect to y. Hence, the E will become $E=\frac{d\Phi}{dy}$. Initially, the electric field was calculated separately for symmetric DG-FinFET $\left(E_{sym}\right)$ and asymmetric DG-FinFET $\left(E_{asym}\right)$. The E of TG-FinFET was calculated by merging the E_{sym} and E_{asym} using perimeter-weighted sum method.

The E_{sym} is obtainable by differentiating $\Phi(y,z)$ of equation (3.38) with respect to y and it becomes,

$$E_{sym}=\frac{\delta\phi(z,y)}{\delta y}=\frac{1}{e^{\frac{2L}{\lambda_{sym}}}}\left[\begin{matrix}\frac{\left(v_{bi}+v_d-A_{sym}\right)}{\lambda_{sym}}\left(e^{\left(\frac{L+y}{\lambda_{sym}}\right)}+e^{\left(\frac{L-y}{\lambda_{sym}}\right)}\right)-\\\frac{\left(v_{bi}-A_{sym}\right)}{\lambda_{sym}}\left(e^{\left(\frac{2L-y}{\lambda_{sym}}\right)}+e^{\left(\frac{y}{\lambda_{sym}}\right)}\right)\end{matrix}\right] \quad (3.72)$$

Similarly, the E_{asym} will become,

$$E_{asym}=\frac{1}{e^{\frac{2L}{\lambda_{asym}}}}\left[\frac{\left(v_{bi}+v_d-A_{asym}\right)}{\lambda_{asym}}\left(\begin{matrix}e^{\left(\frac{L+y}{\lambda_{asym}}\right)}\\+e^{\left(\frac{L-y}{\lambda_{asym}}\right)}\end{matrix}\right)-\frac{\left(v_{bi}-A_{asym}\right)}{\lambda_{asym}}\left(\begin{matrix}e^{\left(\frac{2L-y}{\lambda_{asym}}\right)}\\+e^{\left(\frac{y}{\lambda_{asym}}\right)}\end{matrix}\right)\right] \quad (3.73)$$

Hence, E can be written as,

$$E = E_{asym}(x,y)\left\{\frac{W_{fin}}{W_{fin}+2H_{fin}}\right\}+E_{sym}(z,y)\left\{\frac{2H_{fin}}{W_{fin}+2H_{fin}}\right\} \qquad (3.74)$$

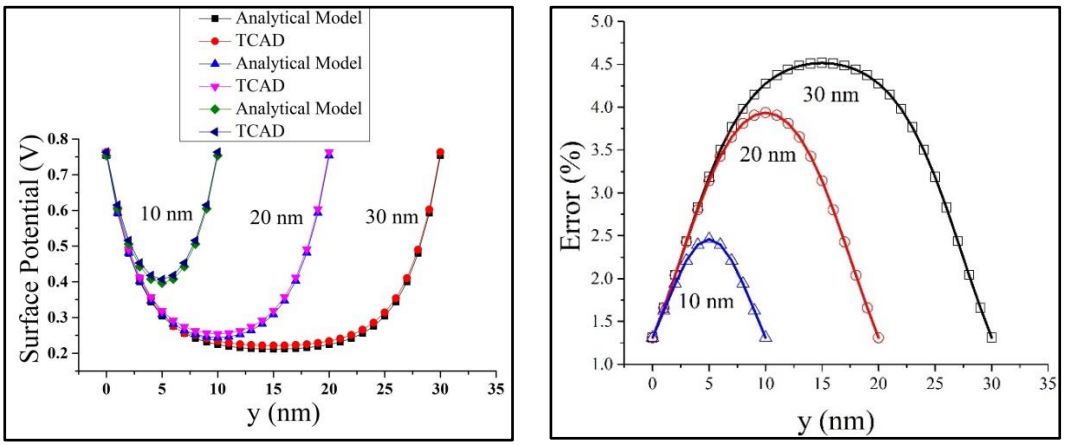
3.3. Results and Discussions

The channel's doping concentration is kept low to circumvent random dopant variation. To avoid the bottom gate interaction with the side gates, t_{oxb} is taken bigger than the channel thickness.

Table 3.1: Design Parameter Values for Surface Potential

SI.	Design Parameters	Value
01.	$N_A \rightarrow$ Body doping concentration	$10^{21}m^{-3}$
02.	$N_D \rightarrow$ Source/ Drain doping concentration	$10^{25}m^{-3}$
03.	$t_{ox} \rightarrow$ Gate oxide thickness	1nm
04.	$t_{oxb} \rightarrow$ Bottom oxide thickness..	100nm
05.	$v_g \rightarrow$ Gate voltage	0.2V
06.	$v_d \rightarrow$ Drain Voltage	0V
07.	$\varepsilon_{si} \rightarrow$ Permittivity of Silicon	11.7
08.	$\varepsilon_{ox} \rightarrow$ Permittivity of Oxide (SiO_2/HfO_2)	3.9/22
09.	$x \rightarrow$ Coordinate of x-axis	0 nm
10.	$z \rightarrow$ Coordinate of z-axis	0 nm

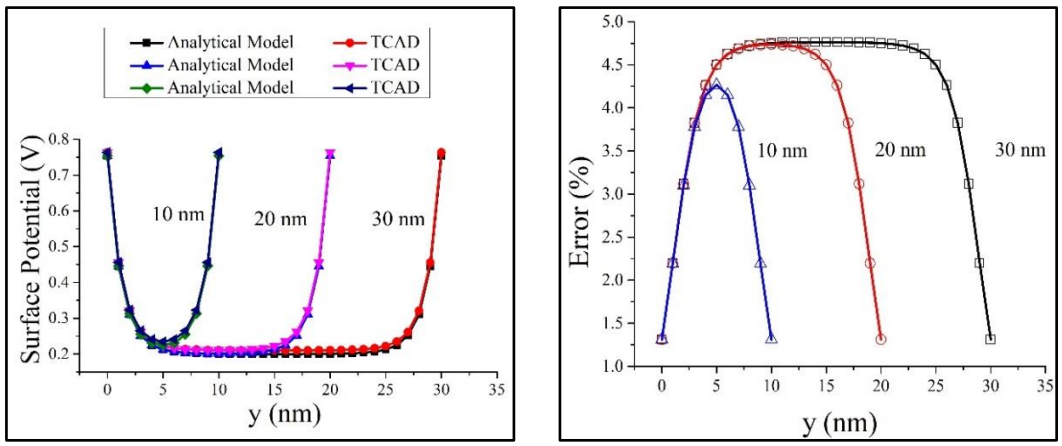
Fig. 3.3(a) and 3.4(a) show the fluctuation of Φ with channel lengths for SiO_2 and HfO_2, respectively. In both circumstances, the minima of Φ rises with the decrement of the channel length. Hence, the source to channel barrier height decreases, decreasing V_T. Channel lengthwise percentage error of Φ for both dielectrics is publicized in Fig. 3.3(b) and Fig. 3.4(b).



(a) **(b)**

Fig.3.3: At three different channel lengths for SiO_2 (a) Change of Φ along the channel (b) Percentage error along channel

Minimum error is observed at $L = 10$ nm for both oxide materials. For these experiments, the W_{fin} and H_{fin} are considered as 5nm and 20nm, respectively.



(a) **(b)**

Fig.3.4: At three different channel lengths for HfO_2 (a) Change of Φ along the channel length (b) Percentage error along the channel

The assessment of the Φ for two dielectrics at $L = 10$ nm has been given in Fig. 3.5. The structure of the fin is same as the previous experiments. It can be detected that the minimum value of the Φ decreases for high-k dielectric material.

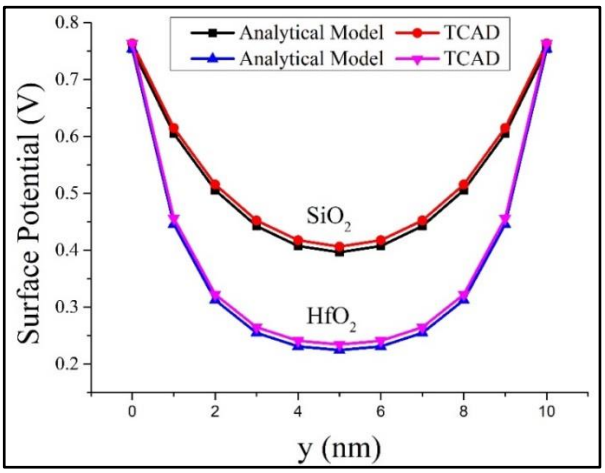
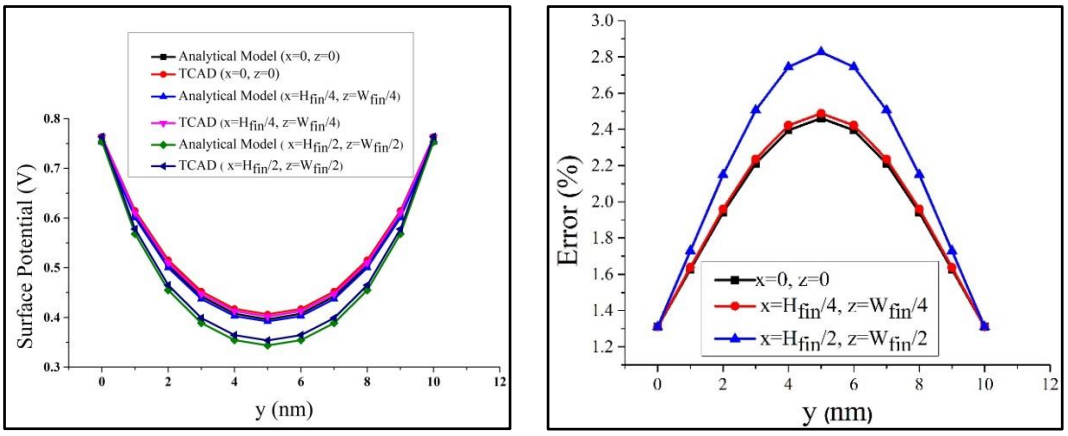


Fig.3.5: Comparison of Φ along the channel for SiO_2 and HfO_2

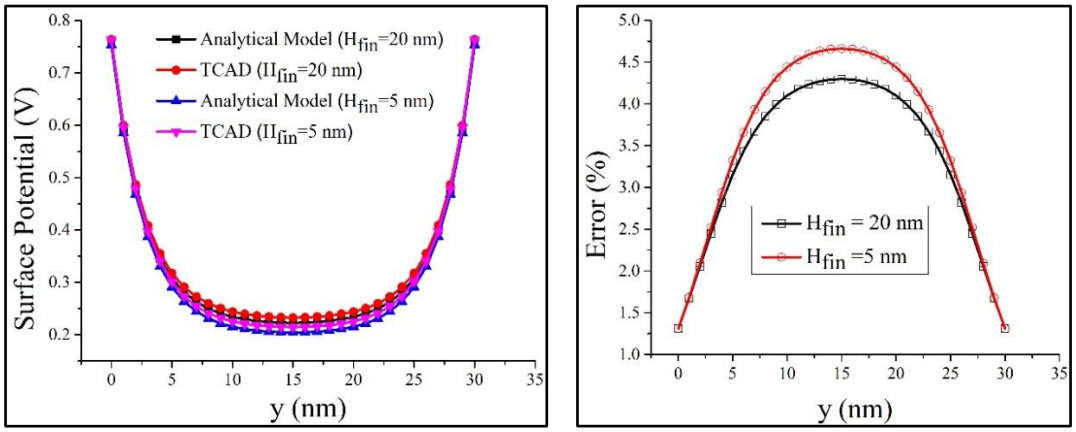
According to (Pei et al., 2002), the leakiest path of the TG-FinFET is found out at the centre of the fin. This is supported by Fig. 3.6(a), which reveals the position of the minimum potential at $x = \frac{H_{fin}}{2}$, $z = \frac{W_{fin}}{2}$. The fin with 5nm width, 20nm height and $L = 10$ nm was considered. The study was conducted on three different locations in the channel. Percentage error is portrayed in Fig.3.6 (b).



(a) **(b)**

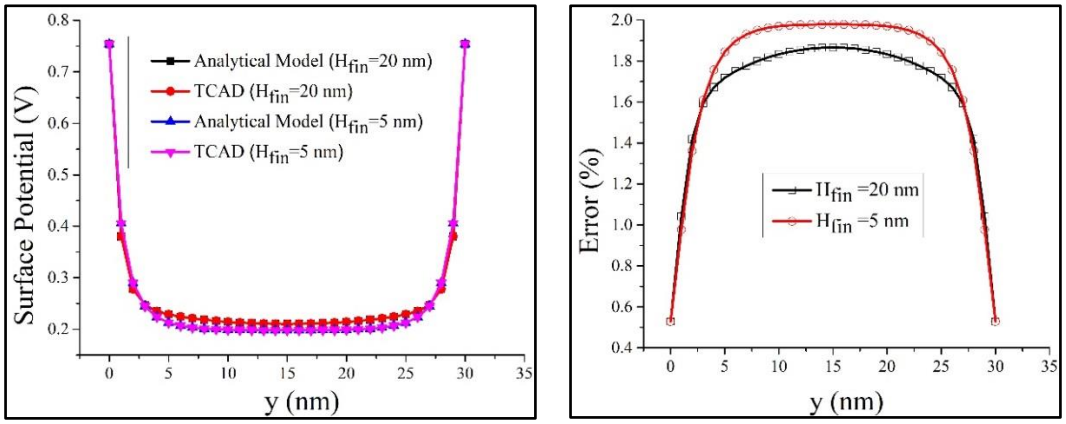
Fig.3.6 At different channel location for SiO_2 (a) Change of Φ along the channel (b) Percentage error of Φ along the channel

The plots of Φ with fin heights as a parameter are shown in Figs. 3.7(a) and 3.8(a) for two gate oxides. The percentage inaccuracy of Φ with relation to H_{fin} is shown in Figures 3.7(b) and 3.8(b). The fin is 5 nm wide.



(a) **(b)**

Fig.3.7: At two fin height for SiO_2 (a) Change of Φ along the channel (b) Percentage error along the channel

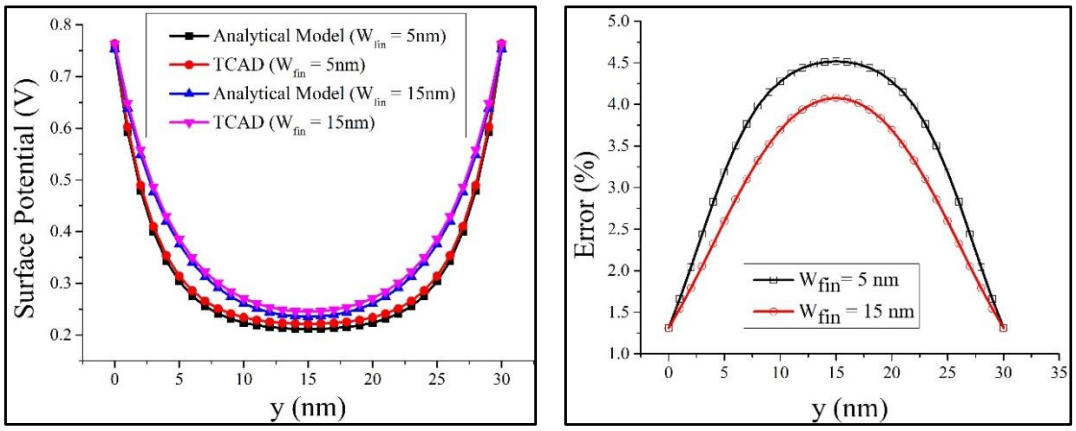


(a) **(b)**

Fig.3.8: At two fin height for HfO_2 (a) Change of Φ along the channel length (b) Percentage error along the channel

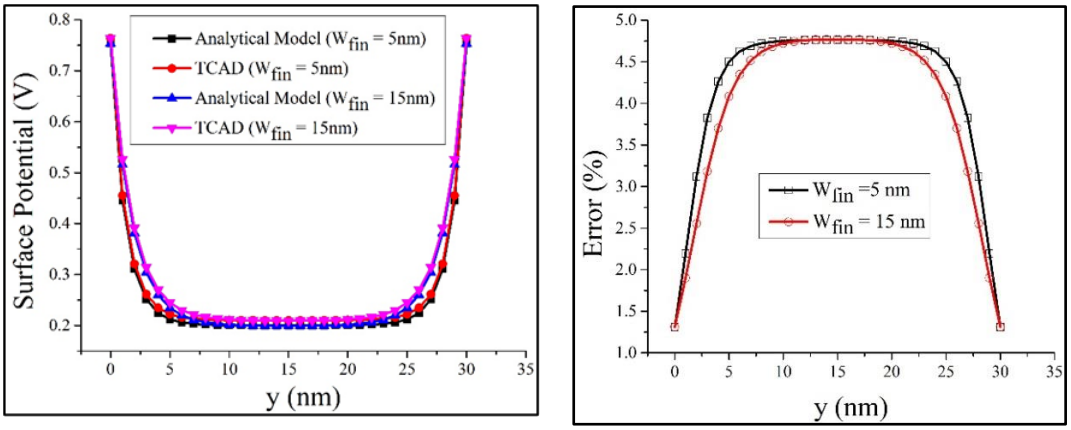
Fig. 3.9(a) and Fig. 3.10(a) illustrate Φ graphs for different fin widths for the dielectric materials SiO_2 and HfO_2, respectively. Fig. 3.9(b) and Fig. 3.10(b) display percentage error of Φ in the y direction for SiO_2 and HfO_2 respectively. The H_{fin} is 20 nm. The percentage errors for both SiO_2 and HfO_2 grow as H_{fin} and W_{fin} decrease. In the case of HfO_2, the average percentage error is less than 2% when measured with

respect to H_{fin} and around 4% when calculated in terms of W_{fin}. It is significant to note that the L in both trials is maintained at 30nm.



(a) **(b)**

Fig.3.9: For two fin widths for SiO_2 (a) Change of Φ along the channel (b) Percentage error of Φ along the channel



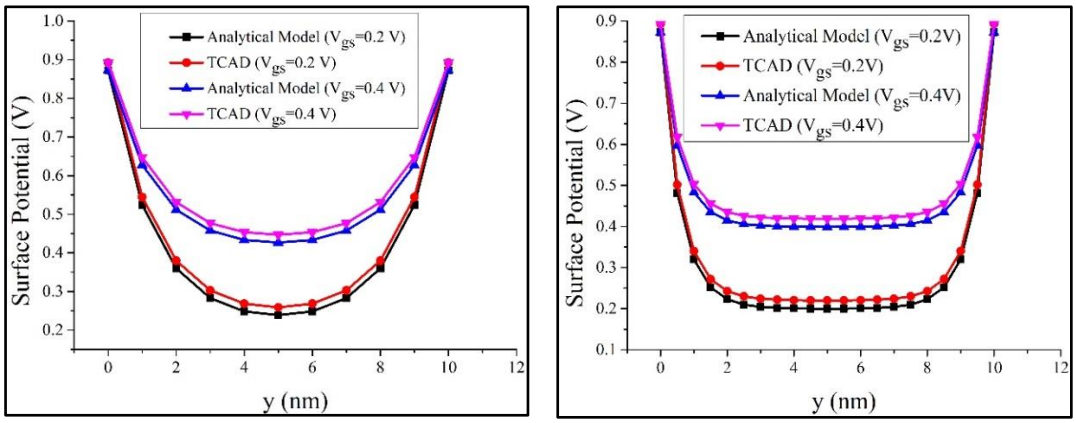
(a) **(b)**

Fig.3.10: For two fin widths for HfO_2 (a) Change of Φ along the channel (b) Percentage error of Φ along the channel

After investigating the fluctuation of Φ with physical parameters of the device, the variation of Φ with electrical parameters is explored in the next section. Therefore, in the following section, the physical parameters such as L, H_{fin} and W_{fin} are kept constants. Here, L is kept at 10 nm, H_{fin} and W_{fin} are considered to be 2 nm.

Fig.3.11 demonstrate the fluctuation of Φ with the variation of v_g for both gate dielectrics. The Φ increase with the increase of gate-to-source voltage. A

comparative study of Φ between two gate dielectrics at $v_g = 0.4\,\text{V}$ has been shown in Fig.3.12.



(a) **(b)**

Fig.3.11: For two gate voltages Change of Φ along the channel length for (a) SiO_2 (b) HfO_2

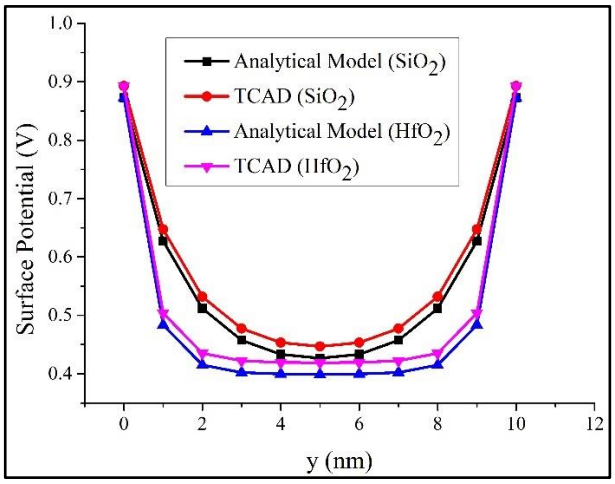


Fig.3.12: Comparison of Φ profile for two separate dielectric materials

From the boundary conditions, it can be stated that Φ is equivalent to v_{bi} at source end and Φ is equal to the summation of $(v_{bi} + v_d)$ at the drain end. These phenomena can be substantiated from Fig.3.13(a) and Fig.3.13 (b) for SiO_2 and HfO_2 respectively. The Φ for two dielectric materials at $v_d = 0.25\,\text{V}$ is compared in Fig.3.14.

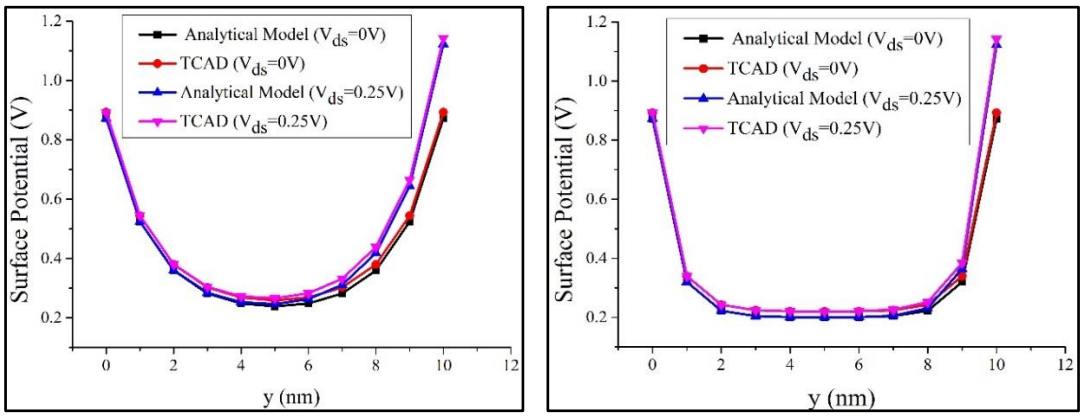


Fig.3.13: For two drain voltages the change of Φ along the channel for (a) SiO_2 (b) HfO_2

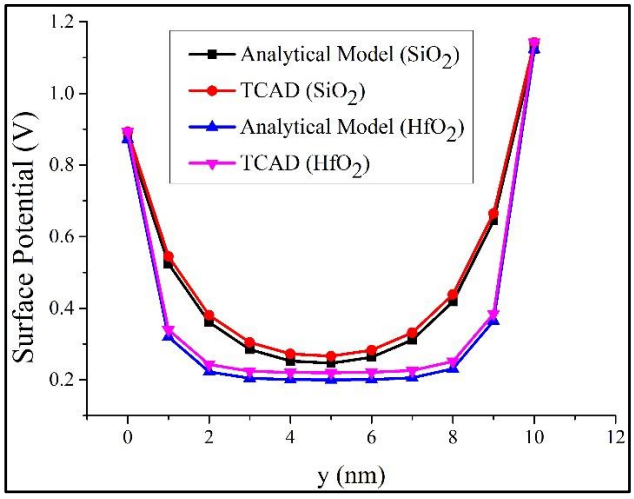
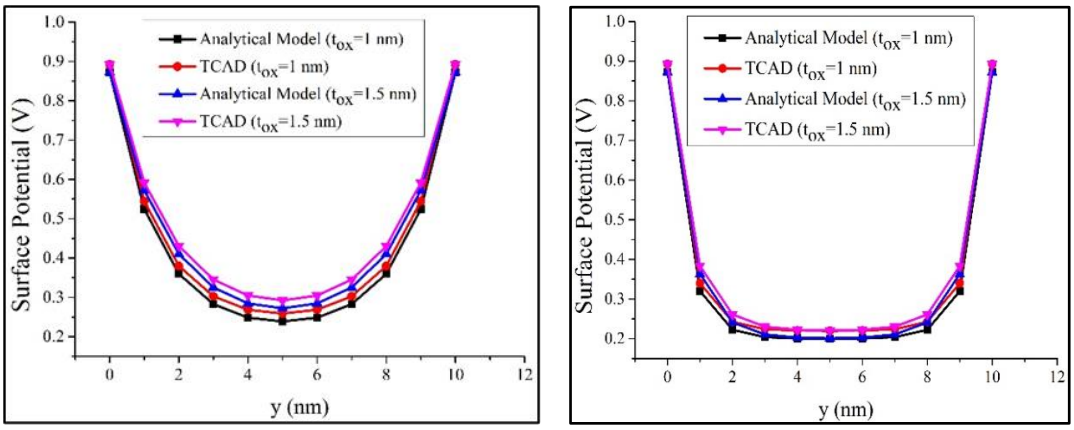


Fig.3.14: Comparison of Φ along the channel for two dielectric materials

As Φ is proportional to the thickness of the gate oxide layer; therefore, Φ increases with the increment of the t_{ox}. Fig.3.15(a) and Fig.3.15(b) are presented to verify the above statement. But the same variation is negligible for HfO_2 material. The comparison is shown in Fig.3.16. It was done for $t_{ox} = 1.5\,\text{nm}$.



(a) **(b)**

Fig.3.15: For two oxide thickness change of Φ down the channel length for (a) SiO_2 (b) HfO_2

The Φ 's lowest value rises as the doping concentration source and/or drain rises. It is established from Fig.3.17(a) and Fig.3.17(b). However, the minimum value's variance is relatively small in both cases. Fig 3.18 depicts a comparison of Φ between two insulating materials and for this experiment $N_D = 10^{22}$ m^{-3}.

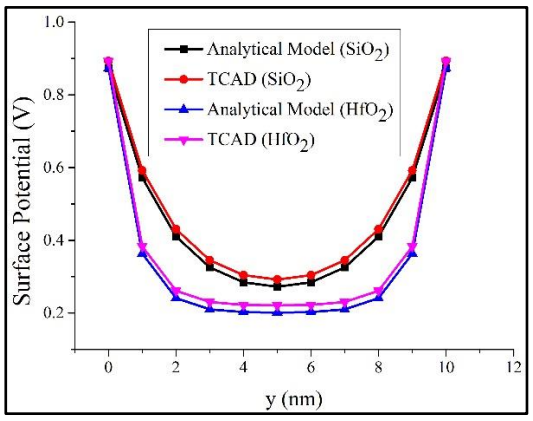
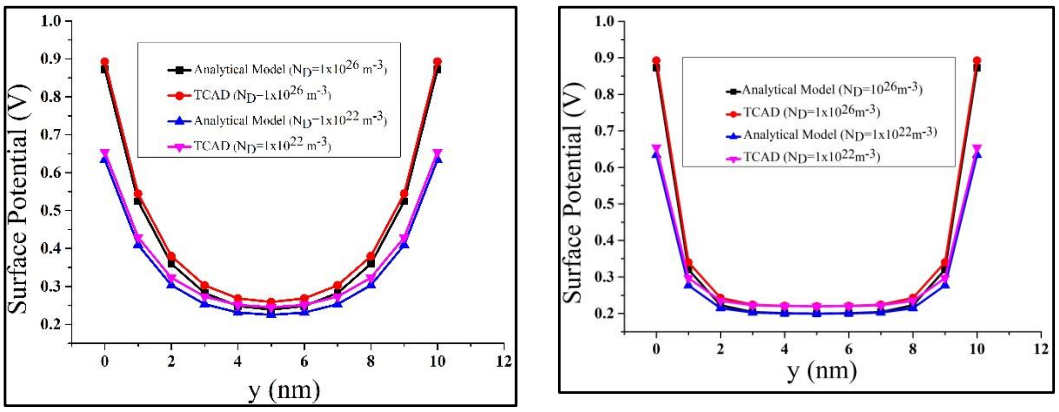


Fig.3.16: Comparison of Φ profiles for different dielectric materials



(a) **(b)**

Fig.3.17: At two source/drain doping concentrations change of Φ along the channel for (a) SiO_2 (b) HfO_2

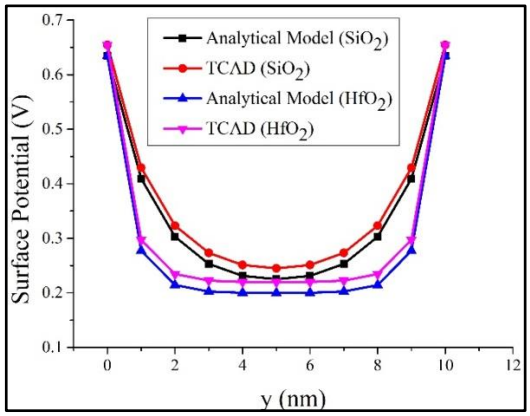
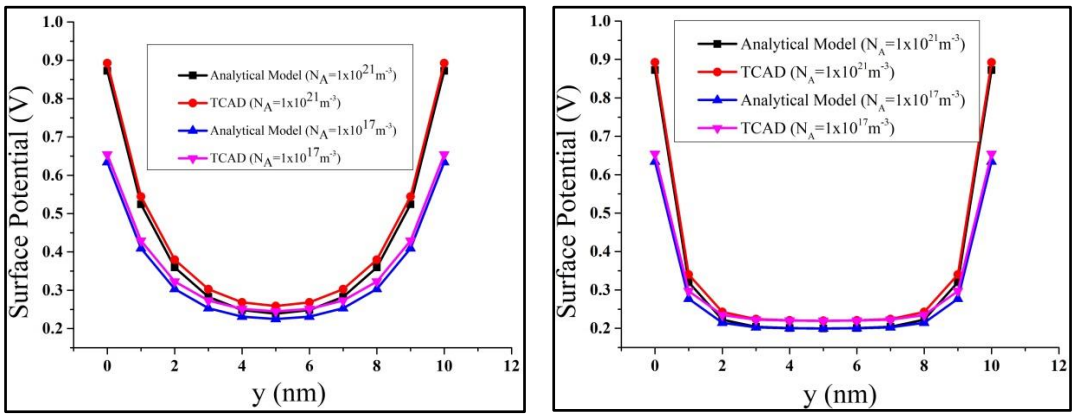


Fig.3.18: Comparison of Φ profiles for different dielectric materials

It is well known that at inversion condition, the Φ is twice of the fermi potential $\left(\Phi_f\right)$, hence the Φ is proportional to the substrate concentration. This effect can be visualized from Fig.3.19(a) and Fig.3.19(b). However, the increase is negligible in this situation as well. Fig.3.20 depicts the comparison between the two dielectrics. The comparison was done at $N_A = 10^{17}$ m^{-3}.



(a) **(b)**

Fig.3.19: At two substrate doping concentrations, change of Φ along the channel for (a) SiO_2 (b) HfO_2

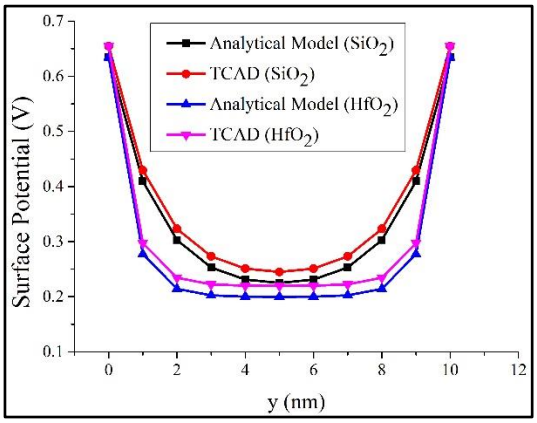


Fig.3.20: Comparative study of change of Φ down the channel length for SiO_2 and HfO_2

Fig.3.21 demonstrates a comparison of the E for two distinct dielectric materials. E at the drain terminal is significantly greater than at the source terminal, and it is much E higher in case of HfO_2.

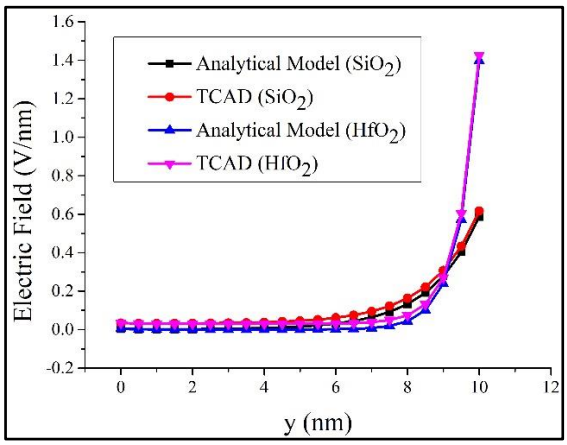


Fig.3.21: Comparison of Electric Field for SiO_2 and HfO_2

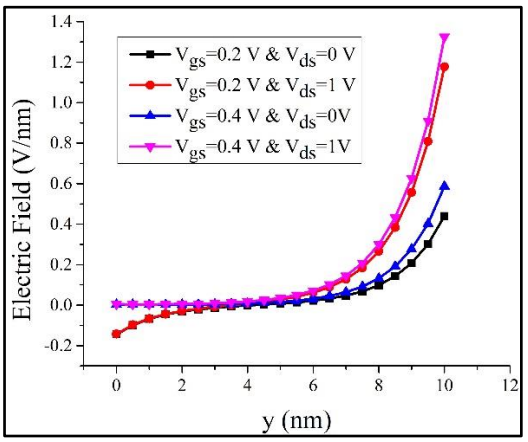


Fig.3.22: Electric field along the channel for SiO_2 at two gate voltages and two drain voltages

Fig.3.22 shows the plot of E in the channel caused by changes in the drain and gate voltages for SiO_2. The E is strongest at the drain, and it grows as the drain and gate voltages grow.

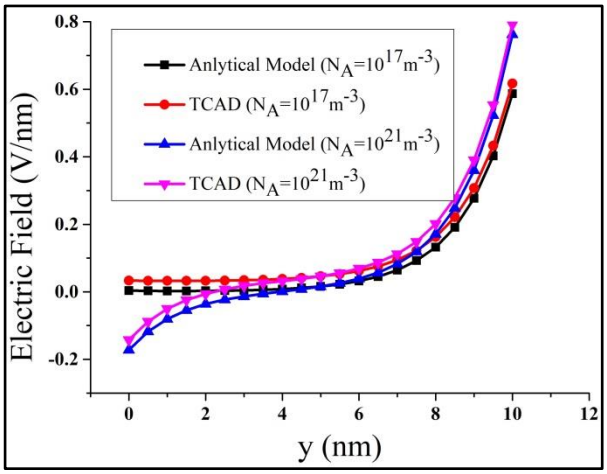


Fig.3.23: The electric field along the channel lengths for SiO_2 at two channel doping concentration

The impact of doping concentration of the channel on the E (at values of 10^{17} m^{-3} and 10^{21} m^{-3}) is also investigated and displayed in Fig.23. The E rises with the increase in channel doping concentration, according to Takagi et al. 1994 (Takagi, Toriumi, Iwase, & Tango, 1994). As a result, surface scattering can forecast a decrease in μ.

ATLAS, a frequently used TCAD tool deeply rooted to the theories of physics, is used to simulate the model. The v_{fb} and interface charge density are set to zero to remove the complexity of the mathematical model. However, due to the Si/SiO_2 boundary's non-idealities, such as interface traps, ionic mobile charges, fixed oxide charges, and oxide trap charges, v_{fb} is changed (Maity, Maity, Thapa, & Baishya, 2014). The existence of the fixed and positive interface charge density, according to (Jean & Wu, 1997), raises Φ. Due to the inclusion of all aforesaid nonidealities, the simulation model should predict more accurate results. The correlation between simulation and analytical results is determined using Pearson's product-moment correlation and it is close to 1 for most of the cases. An impressive harmony exists between the mathematics and TCAD simulation encourage the further modeling of the device.

3.4 Summary

The TG-FinFET structure has been divided into symmetric and asymmetric DG-FinFET. The 2-D Poisson's equation is used to calculate the Φ of asymmetric and symmetric DG-FinFETs. The perimeter-weighted approach combines these two to provide the TG-FinFET's potential distribution. Hence, Φ of the 3-D device was achieved by circumventing the complex 3-D Poisson's equation. Therefore, this approach is both cost-effective and time-efficient while also providing a thorough grasp of the device's underlying physics. The same model has also been used to explore the effect of HfO_2 on Φ. The investigation was performed for dissimilar channel lengths, fin heights and fin widths. The L was altered from lowest 10 nm to highest 30 nm. The minimum value of Φ rises as the L reduces, implying that the channel to source barrier height decreases, which in turn indicate the fall of V_T. For both dielectric materials, the maximum least Φ has been obtained at $L = 10$ nm. The range of W_{fin} was kept in between 2nm to 15nm. H_{fin} has been also changed, ranging from 2nm to 20nm. H_{fin} has a noticeable effect on the Φ for SiO_2.The same is true for the W_{fin} or thickness of the fin. But the variation was is prominent for HfO_2. For both

dielectric materials, the potential was always found in the range of 10^{-1}V. Theoretically, the v_d minimum potential was obtained at $x = \frac{H_{fin}}{2}$, $y = \frac{W_{fin}}{2}$ and it has also been verified by the TCAD simulation. The model-driven device performance at different doping concentrations, v_d , v_g and t_{ox} were analysed and closely approximated to the simulation results.

The extra potential, which is a measure of SCE has been formulated analytically. Therefore, it can be concluded that the potential distribution along the different positions of the channel is impeccably described by the analytical model and supported by the simulation. As the nonidealities are not included in the model, the differences between the two methodologies, i.e., analytical and simulation, have been reflected in graphs, but the percentages of errors are within 5%, indicating that the analytical model and the TCAD simulation are in good agreement. This demonstrates the effectiveness of the analytical model.

CHAPTER - 4

Threshold Voltage

4.1. Introduction

The V_T is one of the most critical characteristics related to the MOSFET device. It is the minimum amount of v_g required to form the inversion layer between source and drain. Various methods are available for extracting V_T. In a sufficiently doped transistor, inversion layer exists near the oxide semiconductor interface and Φ controls the entire device operation. On the other hand, in the undoped substrate, the gate field penetrates in the middle of the body and as a result, the thickness of the inversion layer is much larger than the doped bulk transistor. Hence, V_T must be redefined and constructed on the charge per unit area of the body (Q. Chen, Harrell, & Meindl, 2003; Ray & Mahapatra, 2008). The terminology V_T, in this case, is expounded as a voltage at the gate terminal for which an inversion sheet charge density (Q_{inv}) will be equal to critical threshold charge density (Q_{th}) and is sufficient for detecting the turn-on condition. A few important V_T extraction methods are discussed below:

Constant current is a popular method of extracting V_T (Liou, Ortiz-Condez, & Sanchez, 1997). In this method, $\log(I_d)$ is plotted against v_g with a constant v_d, as shown in Fig.4.1. V_T is extracted from the graph. In this technique, the v_g is assumed

to be V_T at which I_d attains a user-specific or process-specific value. This is the easy and convenient method of obtaining V_T in the linear as well as in saturation region. But the selection of the specific current value is the most challenging issue of this scheme (Liou et al., 1997; Ortiz-Conde et al., 1997).

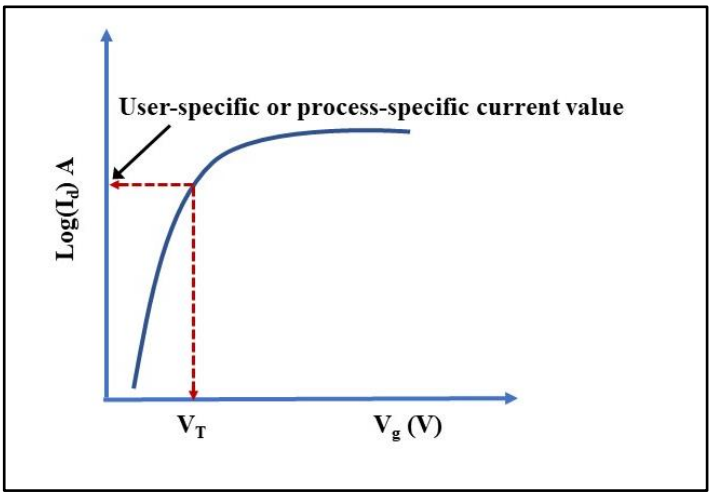


Fig.4.1: Extraction of V_T using constant current method

The linear-extrapolation is another prominent V_T extraction approach (Liou et al., 1997). Because of the presence of series resistance and degradation of μ, the transfer characteristic loses its linear nature for v_g exceeding V_T. Finding out the maximum slope point on the transfer characteristics is the first step of this method. Then a straight line is fitted to that point and interpolated the line to the voltage coordinate, i.e., $I_d = 0$ A. The straight line's intersection with the v_g axis is used to quantify V_T. The resistances of the source and drain influence the maximum slope point. Therefore, V_T is also strongly inclined by these resistances. This is the main disadvantage of the linear extrapolation method. Extraction of V_T using linear extrapolation method is given in Fig.4.2.

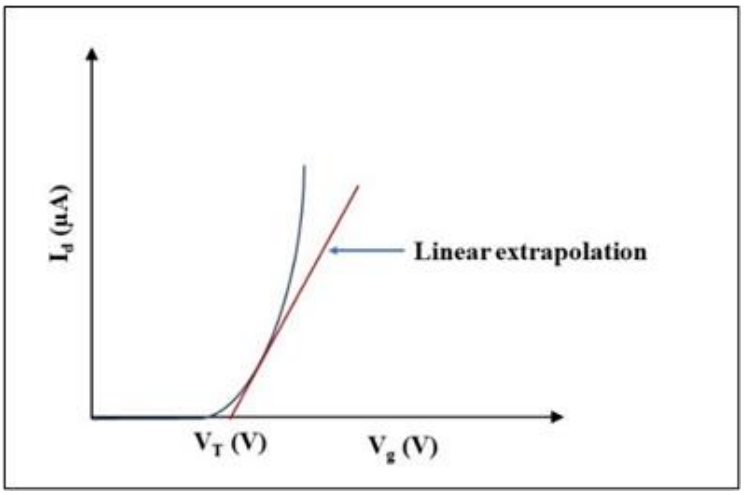


Fig.4.2: Extraction of V_T using the linear extrapolation method

To avoid the dependency of these resistances, the second derivative technique is applied to measure the V_T (Zhou, Lim, & Lim, 1999). In this technique, the v_g is considered as V_T at which g_m reaches its highest value (i.e., $\frac{dI_d^2}{dv_g^2} = 0$).

Current to square root of the Transconductance ratio (CsrTR) method was created by Ray & Mahaptra (Ray & Mahapatra, 2008) and Ghibaudo (Ghibaudo, 1988) independently. It has shown that the function $\sqrt[2]{\frac{I_d}{g_m}}$ don't seem dependent on parasitic series resistance if the μ degradation is insignificant (Ray & Mahapatra, 2008). Ghibaudo, on the other hand, demonstrated that under the low parasitic series resistance, the function $\sqrt[2]{\frac{I_d}{g_m}}$ would not be dependent on μ degradation (Ghibaudo, 1988). Fikry et.al. (Fikry, Ghibaudo, Haddara, Cristoloveanu, & Dutoit, 1995) demonstrated in 1995 that the function $\sqrt[2]{\frac{I_d}{g_m}}$ is independent of the effects of velocity saturation, parasitic series resistance, and μ degradation. The CsrTR method, also known as "the modified Y function method," has recently been enhanced for the

application of more advanced devices (Jomaah, Fadlallah, & Ghibaudo, 2011; N. Subramanian, Ghibaudo, & Mouis, 2010).

The mechanism of quasi-constant-current (Z. Yan & Deen, 1991) was developed using the notion of I_d in the subthreshold realm. In this region, the minimum amount of v_g required to attain Φ is double of the bulk potential and is defined as V_T. Apart from the hassles of determining V_T, such a process is only valid where the electrical features are poorly defined, such as in the subthreshold area, in contrast to the strong inversion zone.

In this study, the charge sheet approximation is used to model the V_T. Here V_T is the v_g at which the Q_{inv} attains Q_{th} (Chindalore et al., 1997). This method is analogous to the constant I_d model, a well-accepted model, in experimental measurement and numerical simulation.

4.2. Analytical Model of Threshold Voltage

To model V_T of the TG-FinFET, it is initially divided into DG-symmetric and DG-asymmetric FinFET. The V_T of a device like DG-FinFET can be estimated using the inversion charge method, i.e., the minimum amount of v_g at which $Q_{inv} = Q_{th}$. The V_T of symmetric DG-FinFET and asymmetric DG-FinFET are assimilated by the perimeter-weighted sum method to obtain the V_T of TG-FinFET.

4.2.1 Threshold voltage for symmetrical FinFET

The inversion charge sheet density at the virtual cathode position is denoted as,

$$Q_{inv\_sym} = \left(n_i W_{fin}\right) \times \left(\frac{1}{CF\_sym}\right) e^{v_g' / v_{th}} \tag{4.1}$$

CF_sym is the correction factor. In the long channel device CF_sym is a unit function. But, for the device, where $\frac{L}{W_{fin}} > 2$ it will become,

$$CF\_sym \cong \exp\left(-\left(\frac{\Delta\Phi_{sym}}{v_{th}}\right)\right) \tag{4.2}$$

From equation (3.40) $\Delta\Phi_{sym}$ at virtual cathode position can be written as,

$$\Delta\Phi_{sym} = \frac{1}{\left(e^{\frac{2L}{\lambda_{sym}}} - 1\right)}\left[\left(v_{bi} + v_d - v_g^{'}\right)\times\left(\begin{matrix} e^{\frac{(L+y_m)}{\lambda_{sym}}} \\ -e^{\frac{(L-y_m)}{\lambda_{sym}}} \end{matrix}\right) + \left(v_{bi} - v_g^{'}\right)\times\left(\begin{matrix} e^{\frac{(2L-y_m)}{\lambda_{sym}}} \\ -e^{\frac{y_m}{\lambda_{sym}}} \end{matrix}\right)\right] \tag{4.3}$$

Here, y_m is the virtual cathode position and it is defined as the channel position at which the potential is minimum. y_m can be calculated by setting the Φ derivative to zero. The detailed calculation is given below. Differentiating equation (3.38) with respect to y, it will become,

$$\frac{\delta\Phi(y,z)}{\delta y} = \frac{1}{e^{\frac{2L}{\lambda_{sym}}} - 1}\left[\begin{matrix} \frac{A_v}{\lambda_{sym}} e^{(L+y)/\lambda_{sym}} + \frac{A_v}{\lambda_{sym}} e^{(L-y)/\lambda_{sym}} - \frac{B_v}{\lambda_{sym}} e^{(2L-y)/\lambda_{sym}} \\ -\frac{B_v}{\lambda_{sym}} e^{y/\lambda_{sym}} \end{matrix}\right] \tag{4.4}$$

Here, $A_v = \left(v_{bi} + v_d - v_g^{'}\right)$ and $B_v = \left(v_{bi} - v_g^{'}\right)$. $\frac{\delta\Phi(y,z)}{\delta y}$ should be zero at virtual cathode position, i.e., $y = y_{\min}$. Hence, equation (4.4) can be written as,

$$0 = \frac{1}{e^{\frac{2L}{\lambda_{sym}}} - 1}\left[\frac{A_v}{\lambda_{sym}} e^{(L+y_{\min})/\lambda_{sym}} + \frac{A_v}{\lambda_{sym}} e^{(L-y_m)/\lambda_{sym}} - \frac{B_v}{\lambda_{sym}} e^{(2L-y_m)/\lambda_{sym}} - \frac{B_v}{\lambda_{sym}} e^{y_m/\lambda_{sym}}\right]$$

or, $$\frac{B_v}{\lambda_{sym}}\left[e^{(2L-y_m)/\lambda_{sym}} + e^{y_m/\lambda_{sym}}\right] = \frac{A_v}{\lambda_{sym}}\left[e^{(L+y_m)/\lambda_{sym}} + e^{(L-y_m)/\lambda_{sym}}\right]$$

$$\text{or, } e^{\left\{(L-2y_m)/\lambda_{sym}\right\}} = \frac{\left(v_{bi}-v_g^{'}\right)\left(e^{L/\lambda_{sym}}-1\right)+v_d e^{L/\lambda_{sym}}}{\left\{\left(v_{bi}-v_g^{'}\right)\left(e^{L/\lambda_{sym}}-1\right)-v_d\right\}} \tag{4.5}$$

Taking logarithm in both sides, equation (4.5) will be -

$$\frac{1}{\lambda_{sym}}\left(L-2y_m\right) = \ln\frac{\left(v_{bi}-v_g^{'}\right)\left(e^{L/\lambda_{sym}}-1\right)+v_d e^{L/\lambda_{sym}}}{\left\{\left(v_{bi}-v_g^{'}\right)\left(e^{L/\lambda_{sym}}-1\right)-v_d\right\}}$$

$$y_m = \frac{L}{2}-\frac{\lambda_{sym}}{2}\ln\frac{\left(v_{bi}-v_g^{'}\right)\left(e^{L/\lambda_{sym}}-1\right)+v_d e^{L/\lambda_{sym}}}{\left\{\left(v_{bi}-v_g^{'}\right)\left(e^{L/\lambda_{sym}}-1\right)-v_d\right\}} \tag{4.6}$$

Therefore, rewriting equation (4.3),

$$\Delta\Phi_{sym} = \left(v_{bi}+v_d-v_g^{'}\right)M_{1sym}+\left(v_{bi}-v_g^{'}\right)M_{2sym} \tag{4.7}$$

where, $M_{1sym} = \dfrac{e^{(L+y_m)/\lambda_{sym}}-e^{(L-y_m)/\lambda_{sym}}}{e^{2L/\lambda_{sym}}-1}$ and $M_{2sym} = \dfrac{e^{(2L-y_m)/\lambda_{sym}}-e^{y_m/\lambda_{sym}}}{e^{2L/\lambda_{sym}}-1}$. Hence, equation (4.1) will become,

$$\frac{Q_{inv\_sym}}{n_i W_{fin}} = \frac{1}{CF\_sym}e^{\frac{v_g^{'}}{v_{th}}}$$

Taking logarithm on both sides, the above equation will become,

$$\ln\left(\frac{Q_{inv\_sym}}{n_i W_{fin}}\right) = -\ln\left(CF\_sym\right)+\frac{v_g^{'}}{v_{th}} \tag{4.8}$$

Now, putting the value of CF_sym in equation (4.8), we can write,

$$\ln\left(\frac{Q_{inv\_sym}}{n_i W_{fin}}\right) = -\ln\left(e^{\frac{-\Delta\Phi_{sym}}{v_{th}}}\right) + \frac{v_g^{'}}{v_{th}}$$

$$\text{or, } \ln\left(\frac{Q_{inv\_sym}}{n_i W_{fin}}\right) = \frac{\Delta\Phi_{sym}}{v_{th}} + \frac{v_g^{'}}{v_{th}}$$

$$v_{th}\ln\left(\frac{Q_{inv\_sym}}{n_i W_{fin}}\right) = \left(v_{bi} + v_d - v_g^{'}\right)M_{1sym} + \left(v_{bi} - v_g^{'}\right)M_{2sym} + v_g^{'}$$

Putting $v_g^{'} = v_g - v_{fb}$, the above equation will be,

$$v_g = v_{fb} - \frac{\left(v_{bi} + v_d\right)M_{1sym} + v_{bi}M_{2sym}}{1-\left(M_{1sym} + M_{2sym}\right)} + \frac{v_{th}}{1-\left(M_{1sym} + M_{2sym}\right)}\ln\left(\frac{Q_{inv\_sym}}{n_i W_{fin}}\right) \quad (4.9)$$

From the definition of V_T, at $v_g = V_{T\_sym}$, $Q_{inv\_sym} = Q_{th\_sym}$, therefore, V_T of symmetric DG-FinFET will be,

$$V_{T\_sym} = v_{fb} - \frac{M_{1sym}\left(v_{bi} + v_d\right) + M_{2sym}v_{bi}}{1-\left(M_{1sym} + M_{2sym}\right)} + \frac{v_{th}}{1-\left(M_{1sym} + M_{2sym}\right)}\ln\left(\frac{Q_{th\_sym}}{n_i W_{fin}}\right) \quad (4.10)$$

4.2.2 Threshold voltage for asymmetrical FinFET

At the virtual cathode position, the inversion charge sheet density of the asymmetric DG-FinFET will be written as,

$$Q_{inv\_asym} = \left(n_i H_{fin}\right) \times \left(\frac{1}{CF\_asym}\right) e^{v_g^{'}/v_{th}} \quad (4.11)$$

CF_asym is the correction factor of asymmetric DG-FinFET and it will be,

$$CF_{\_asym} \cong \exp\left(-\left(\frac{\Delta\Phi_{asym}}{v_{th}}\right)\right) \quad (4.12)$$

The extra surface potential developed in the asymmetrical DG-FinFET can be written from equation (3.67) and keeping the similarity with the symmetric DG-FinFET, the excess surface potential at the virtual cathode position, will become,

$$\Delta\Phi_{asym} = \left(v_{bi} + v_d - v_g^{'}\right) M_{1asym} + \left(v_{bi} - v_g^{'}\right) M_{2asym} \tag{4.13}$$

where, $M_{1asym} = \dfrac{e^{(L+y_m)/\lambda_{asym}} - e^{(L-y_m)/\lambda_{asym}}}{e^{2L/\lambda_{asym}} - 1}$ and $M_{2asym} = \dfrac{e^{(2L-y_m)/\lambda_{asym}} - e^{y_m/\lambda_{asym}}}{e^{2L/\lambda_{asym}} - 1}$.

Therefore, from equation (4.11),

$$\frac{Q_{inv\_asym}}{n_i H_{fin}} = \frac{1}{CF_{\_asym}} e^{\frac{v_g^{'}}{v_{th}}} \tag{4.14}$$

Taking logarithm on both sides of equation (4.14),

$$\ln\left(\frac{Q_{inv\_asym}}{n_i H_{fin}}\right) = -\ln\left(CF_{\_asym}\right) + \frac{v_g^{'}}{v_{th}} \tag{4.15}$$

Using the value of $CF_{\_asym}$ in equation (4.15) will be,

$$\ln\left(\frac{Q_{inv\_asym}}{n_i H_{fin}}\right) = -\ln\left(e^{-\Delta\Phi_{asym}/v_{th}}\right) + \frac{v_g^{'}}{v_{th}}$$

or, $\ln\left(\dfrac{Q_{inv\_asym}}{n_i H_{fin}}\right) = \dfrac{\Delta\Phi_{asym}}{v_{th}} + \dfrac{v_g^{'}}{v_{th}}$

or, $v_{th} \ln\left(\dfrac{Q_{inv\_asym}}{n_i H_{fin}}\right) = \left(v_{bi} + v_d - v_g^{'}\right) M_{1asym} + \left(v_{bi} - v_g^{'}\right) M_{2asym} + v_g^{'}$ (4.16)

Putting $v_g^{'} = v_g - v_{fb}$, the above equation will be,

$$v_g = v_{fb} - \frac{\left(v_{bi} + v_d\right) M_{1asym} + v_{bi} M_{2asym}}{1 - \left(M_{1asym} + M_{2asym}\right)} + \frac{v_{th}}{1 - \left(M_{1asym} + M_{2aym}\right)} \ln\left(\frac{Q_{inv\_asym}}{n_i H_{fin}}\right) \tag{4.17}$$

In equation (4.17), put $v_g = V_{T\_asym}$, $Q_{inv\_asym} = Q_{th\_asym}$, therefore,

$$V_{T\_\text{asym}} = v_{fb} - \left[\frac{M_{1asym}\left(v_{bi}+v_d\right)+M_{2asym}v_{bi}}{1-\left(M_{1asym}+M_{2asym}\right)}\right] + \left[\frac{\dfrac{v_{th}}{1-\left(M_{1asym}+M_{2asym}\right)}}{\ln\left(\dfrac{Q_{th\_\text{asym}}}{n_i H_{fin}}\right)}\right] \tag{4.18}$$

4.2.3 Threshold voltage for TG-FinFET

At the leakiest path $\left(y_{\min}\right)$, the inversion charge per unit length along the channel of a TG-FinFET can be expressed as (Tsormpatzoglou et al., 2008)

$$Q_{inv\_TG} = n_i W_{fin} H_{fin}\left(\frac{1}{CF\_TG}\right)\exp\left(v_g^{'}/v_{th}\right) \tag{4.19}$$

Keeping similarity with DG-FinFET, the correction factor of TG-FinFET will become,

$$CF\_TG \cong \exp\left(-\frac{\Delta\Phi_m}{v_{th}}\right) \tag{4.20}$$

The excess potential created in TG-FinFET can be written from equation (3.71) at $\left(x_m, y_m, z_m\right)$ by the perimeter-weighted sum technique,

$$\begin{aligned}\Delta\Phi_m &= \frac{W_{fin}}{W_{fin}+2H_{fin}}\left\{\left(v_{bi}+v_d-v_g^{'}\right)M_{1asym}+\left(v_{bi}-v_g^{'}\right)M_{2asym}\right\}\\ &+\frac{2H_{fin}}{W_{fin}+2H_{fin}}\left\{\left(v_{bi}+v_d-v_g^{'}\right)M_{1sym}+\left(v_{bi}-v_g^{'}\right)M_{2sym}\right\}\end{aligned} \tag{4.21}$$

or,

$$\begin{aligned}\Delta\Phi_m &= \frac{W_{fin}}{W_{fin}+2H_{fin}}\left\{\left(v_{bi}+v_d\right)M_{1asym}+v_{bi}M_{2asym}-v_g^{'}\begin{pmatrix}M_{1asym}\\+M_{2asym}\end{pmatrix}\right\}\\ &+\frac{2H_{fin}}{W_{fin}+2H_{fin}}\left\{\left(v_{bi}+v_d\right)M_{1sym}+v_{bi}M_{2sym}-v_g^{'}\begin{pmatrix}M_{1sym}\\+M_{2sym}\end{pmatrix}\right\}\end{aligned} \tag{4.22}$$

At threshold condition $Q_{inv\_TG} = Q_{th\_TG}$. Therefore, equation (4.19) can be written as,

$$Q_{th\_TG} = n_i H_{fin} W_{fin} \left\{ \exp\left(\frac{\Delta\Phi_m}{v_{th}} \right) \right\} \exp\left(\frac{v_g'}{v_{th}} \right) \tag{4.23}$$

Substituting $\Delta\Phi_m$ in equation (4.23), it can be obtained,

$$Q_{th\_TG} = n_i H_{fin} W_{fin} \exp\left[\left(\frac{1}{v_{th}} \right) \left(\begin{array}{l} \dfrac{W_{fin}}{W_{fin}+2H_{fin}} \left\{ \begin{array}{l} (v_{bi}+v_d) M_{1asym} \\ +v_{bi} M_{2asym} \\ -v_g' \left(\begin{array}{l} M_{1asym} \\ +M_{2asym} \end{array} \right) \end{array} \right\} \\ + \dfrac{2H_{fin}}{W_{fin}+2H_{fin}} \left\{ \begin{array}{l} (v_{bi}+v_d) M_{1sym} \\ +v_{bi} M_{2sym} \\ -v_g' \left(\begin{array}{l} M_{1sym} \\ +M_{2sym} \end{array} \right) \end{array} \right\} \end{array} \right) \right] \exp\left(\frac{v_g'}{v_{th}} \right) \tag{4.24}$$

Taking logarithm in both sides, the equation (4.24) will be,

$$v_{th} \ln\left(\frac{Q_{th\_TG}}{n_i H_{fin} W_{fin}} \right) = (v_{bi}+v_d) \left\{ M_{1asym} \left(\frac{W_{fin}}{W_{fin}+2H_{fin}} \right) + M_{1sym} \left(\frac{2H_{fin}}{W_{fin}+2H_{fin}} \right) \right\}$$
$$+v_{bi} \left\{ M_{2asym} \left(\frac{W_{fin}}{W_{fin}+2H_{fin}} \right) + M_{2sym} \left(\frac{2H_{fin}}{W_{fin}+2H_{fin}} \right) \right\}$$
$$+v_g' \left\{ 1 - \left(\frac{W_{fin}}{W_{fin}+2H_{fin}} \right) \left(M_{1asym}+M_{2asym} \right) - \left(\frac{2H_{fin}}{W_{fin}+2H_{fin}} \right) \left(M_{1sym}+M_{2sym} \right) \right\}$$

$$v_{th} \ln\left(\frac{Q_{th\_TG}}{n_i H_{fin} W_{fin}} \right) = (v_{bi}+v_d) \frac{\left(\begin{array}{l} M_{1asym} W_{fin} \\ +2H_{fin} M_{1sym} \end{array} \right)}{W_{fin}+2H_{fin}} + v_{bi} \frac{\left(\begin{array}{l} W_{fin} M_{2asym} \\ +2H_{fin} M_{2sym} \end{array} \right)}{W_{fin}+2H_{fin}}$$

or,

$$+(v_g - v_{fb}) \left\{ \begin{array}{l} 1 - \dfrac{1}{W_{fin}+2H_{fin}} \left(W_{fin} M_{1asym} + W_{fin} M_{2asym} \right) - \\ \dfrac{1}{W_{fin}+2H_{fin}} \left(2H_{fin} M_{1sym} + 2H_{fin} M_{2sym} \right) \end{array} \right\} \tag{4.25}$$

Let, $M_{1TG} = \left(2H_{fin}M_{1sym} + W_{fin}M_{1asym}\right)/\left(W_{fin} + 2H_{fin}\right)$ and

$M_{2TG} = \left(2H_{fin}M_{2sym} + W_{fin}M_{2asym}\right)/\left(W_{fin} + 2H_{fin}\right)$. Hence, the equation (4.25) will be,

$$v_{th}\ln\left(\frac{Q_{th\_TG}}{n_i H_{fin} W_{fin}}\right) = \left(v_{bi} + v_d\right)M_{1TG} + v_{bi}M_{2TG}$$
$$-\left(v_g - v_{fb}\right)\left\{\begin{array}{l} 1 - \dfrac{1}{W_{fin} + 2H_{fin}}\left(W_{fin}M_{1asym} + 2H_{fin}M_{1sym}\right) - \\ \dfrac{1}{W_{fin} + 2H_{fin}}\left(W_{fin}M_{2asym} + 2H_{fin}M_{2sym}\right) \end{array}\right\}$$

or, $$v_{th}\ln\left(\frac{Q_{th\_TG}}{n_i H_{fin} W_{fin}}\right) = \left(v_{bi} + v_d\right)M_{1TG} + v_{bi}M_{2TG} - \left[\begin{array}{l} \left(v_g - v_{fb}\right) \\ \left\{1 - \left(M_{1TG} + M_{2TG}\right)\right\} \end{array}\right] \quad (4.26)$$

Therefore,

$$v_g = v_{fb} - \frac{\left(v_{bi} + v_d\right)M_{1TG} + v_{bi}M_{2TG}}{1 - \left(M_{1TG} + M_{2TG}\right)} + \frac{1}{1 - \left(M_{1TG} + M_{2TG}\right)}v_{th}\ln\left(\frac{Q_{th\_TG}}{n_i H_{fin} W_{fin}}\right) \quad (4.27)$$

Hence, form the definition of V_T, it will be,

$$V_T = v_{fb} - \frac{M_{1TG}\left(v_{bi} + v_d\right) + M_{2TG}v_{bi}}{1 - \left(M_{1TG} + M_{2TG}\right)} + \frac{v_{th}}{1 - \left(M_{1TG} + M_{2TG}\right)}\ln\left(\frac{Q_{th\_TG}}{n_i W_{fin} H_{fin}}\right) \quad (4.28)$$

In terms of DG-FinFET, the threshold inversion charge density in TG-FinFET can be stated as $Q_{th\_TG} = nH_{fin}Q_{th\_DG}$. Here n is the scaling factor, and 1.6 is chosen to best fit the simulation outcomes. Therefore, the equation (4.28) can be written as,

$$V_T = v_{fb} - \frac{M_{1TG}\left(v_{bi} + v_d\right) + M_{2TG}v_{bi}}{1 - \left(M_{1TG} + M_{2TG}\right)} + \frac{v_{th}}{1 - \left(M_{1TG} + M_{2TG}\right)}\ln\left(n\frac{Q_{th\_DG}}{n_i W_{fin}}\right) \quad (4.29)$$

Because of the aggressive miniaturization of the device size, painstaking QM corrections are required to increase the precision of the device modeling. A quantum well forms inside the channel of FinFET if the W_{fin} is shorter than 10nm. The charge

carriers of the well behave as a 2-D gas which can be explained by the quantum-mechanical method (Y Taur & Ning, 1998). Hence, carriers' energy will be quantized due to electrical or structural confinement. As a result of energy quantization, electrons will be in the first sub-band, i.e., above the bottom of the conduction band. In order to achieve the threshold condition, a little greater v_g is required. The increase in V_T due to QME is indicated as (Bhattacherjee & Biswas, 2007).

$$\Delta V_T^{QM} = \frac{1}{2qm^*}\left(\frac{h}{2W_{fin}}\right)^2 \tag{4.30}$$

According to (Yun et al., 2007), The TG-FinFET has a first sub-band energy that is twice as high as the DG- FinFET's. In light of this, the increase in V_T can be expressed as,

$$\Delta V_T^{QM} = \frac{o}{2qm^*}\left(\frac{h}{2W_{fin}}\right)^2 . \tag{4.31}$$

For square cross-sectioned TG-FinFET, o is chosen as 2.

The location of the charge distribution peak was observed to be higher than the peak suggested by classical mechanics. The peak was found out at 0.3-0.4 nm away from the oxide-semiconductor interface (Y Taur & Ning, 1998). As a result of the increased t_{ox}, electrostatic coupling between the channel and the gate will be reduced. This problem can be solved by taking into account the modified t_{ox} i.e., $\left(t_{ox}^{QM}\right)$ and following (Song, Yuan, Yu, Xiong, & Taur, 2010) it will be,

$$t_{ox}^{QM} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\kappa \tag{4.32}$$

κ was computed by Ohkura (Ohkura, 1990) from the average thickness of the inversion layer and arrived at 1.2 nm. The concept has been successfully used in the modeling of MOSFETs (Mukhopadhyay et al., 2008). Hence, in response of enhanced

t_{ox}, V_T enhances and the increment of V_T is indicated ΔV_{T_tox}. Therefore, including QME, the updated V_T will become,

$$V_{T\_QM} = V_T + \Delta V_T^{QM} + \Delta V_{T\_tox} \tag{4.33}$$

The ΔV_T is computed by subtracting the V_T of the long channel device from the short channel device. It is important to mention that M_{1TG} and M_{2TG} are tend to zero for long channel devices.

$$\Delta V_T = -\frac{M_{1TG}\left(v_{bi}+v_d\right)+M_{2TG}V_{bi}}{1-\left(M_{1TG}+M_{2TG}\right)} + \frac{v_{th}(M_{1TG}+M_{2TG})}{1-\left(M_{1TG}+M_{2TG}\right)}\ln\left(\frac{Q_{th\_TG}}{n_i W_{fin}}\right) + \left(\Delta V_T^{QM} + \Delta V_{T\_tox}\right) \tag{4.34}$$

The charge carrier density at minimum potential $\left(N_{\min}\right)$ determines the SS which gives (Tsormpatzoglou et al., 2007)

$$N_{\min} = n_i \exp\left(\frac{v_g^{'} + \Delta\Phi_m}{v_{th}}\right) \tag{4.35}$$

After putting $\Delta\Phi_m$, the differentiation of equation (4.35) with respect to $v_g^{'}$, will provide,

$$\frac{\delta \ln\left(\frac{N_{\min}}{n_i}\right)}{\delta v_g^{'}} = \frac{\left[1-M_{1TG}-M_{2TG}\right]}{v_{th}} \tag{4.36}$$

Therefore, SS can be expressed as,

$$SS = \frac{\delta v_g^{'}}{\delta \log I_d} \approx \ln(10)\frac{\delta v_g^{'}}{\delta \ln(N_{\min}/n_i)} \tag{4.37}$$

$$SS = \log(10)\frac{v_{th}}{\left[1-M_{1TG}-M_{2TG}\right]} \tag{4.38}$$

The SCE in short channel device refers to the lowering of the V_T with larger v_d . Therefore, DIBL coefficient can be obtained from the following equation (Reddy & Kumar, 2005)

$$DIBL = \frac{V_{T(\mathrm{V_d}=0.1V)} - V_{T(\mathrm{V_d}=1.1V)}}{1.1-0.1} \tag{4.39}$$

4.3. Results and Discussions

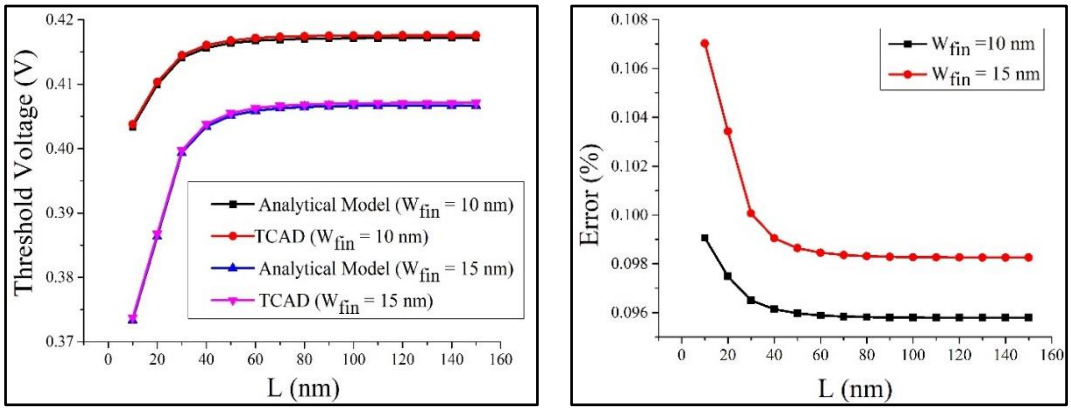
Here also, low channel doping concentration is taken to avoid random dopant fluctuation. The model is computed under ideal interface conditions, i.e. interface charge density is presumed zero. Table 4.1 lists the variables that are used in this investigation.

Table 4.1: Design Parameter Values for Threshold Voltage

SI.	Design Parameters	Value
01.	$N_A \rightarrow$ Uniform body doping concentration	10^{21} m^{-3}
02.	$N_D \rightarrow$ Source/ Drain doping concentration	10^{25} m^{-3}
03.	$t_{ox} \rightarrow$ Gate oxide thickness	1 nm
04.	$t_{oxb} \rightarrow$ Bottom oxide thickness	100 nm
05.	$v_{fb} \rightarrow$ Flat band voltage	0 V
06.	$\varepsilon_{si} \rightarrow$ Permittivity of Silicon	11.7
07.	$\varepsilon_{ox} \rightarrow$ Permittivity of Oxide (SiO_2/HfO_2)	3.9/22

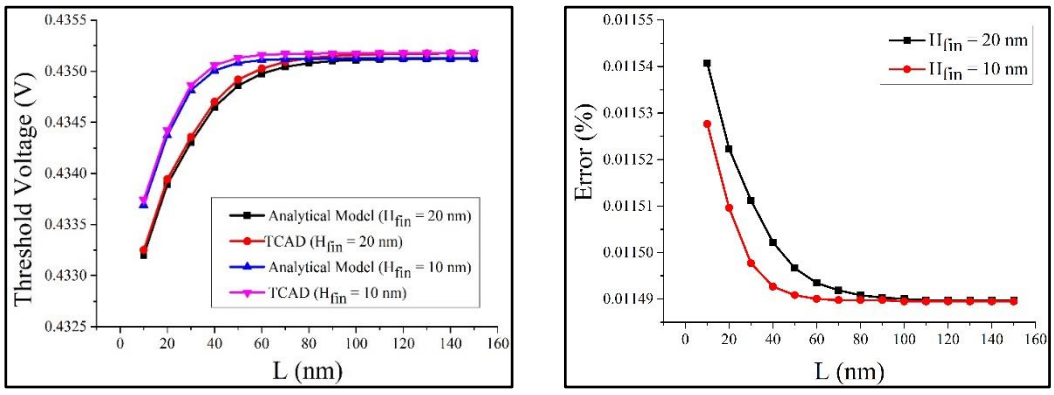
The effect of W_{fin} and H_{fin} on V_T is depicted in Fig. 4.3(a) and Fig. 4.4(a) respectively for SiO_2. To examine the change of V_T with W_{fin}, H_{fin} is taken as 20 nm and W_{fin} is kept at 5 nm to determine the variation of V_T with H_{fin} . In both cases $v_d = 0.1\,\mathrm{V}$ is kept constant. The $W_{eff} = 2H_{fin} + W_{fin}$ decreases with the decrement of W_{fin} as a result, the channel resistance increases. Therefore, V_T increases with the reduction of W_{fin}. On the other hand, enhancement of H_{fin} expands the effective gate

area, enhancing gate regulation. Under the circumstances, the V_T decreases. It is the cause of worse SCE, hence, smaller H_{fin} will provide better SCE. The percentage error between analytical result and simulation is revealed in Fig. 4.3(b) and Fig. 4.4(b). $W_{fin} = 5\,\text{nm}$, for Fig. 4.4.



(a) **(b)**

Fig.4.3: For SiO_2 at different W_{fin} (a) Change of V_T with channel length (b) Percentage error of V_T with channel length

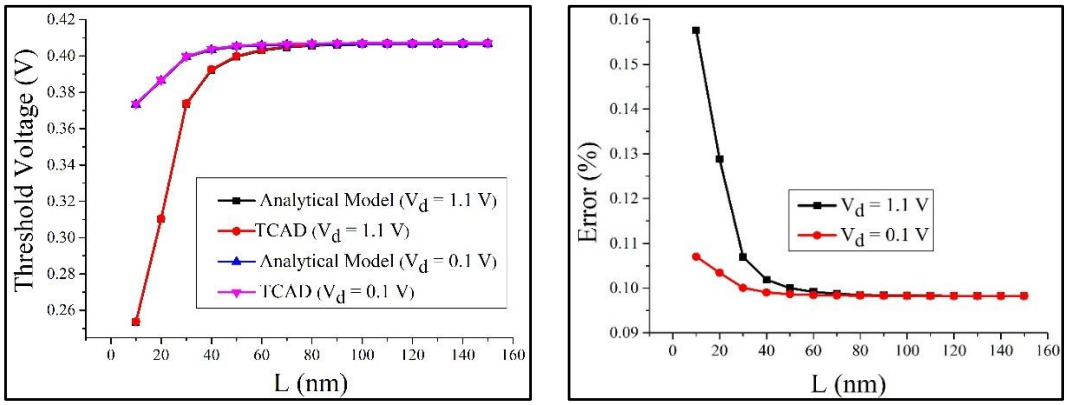


(a) **(b)**

Fig.4.4: For SiO_2 at different H_{fin} (a) Change of V_T with channel length (b) Percentage error of V_T with channel length

The effect of the v_d cannot be neglected in the short channel device. Here V_T is not only controlled by v_g but also influenced by v_d. Due to DIBL, V_T decreases rapidly at larger v_d, it is portrayed in Fig. 4.5(a). The percentage error of the

simulation and analytical results is revealed in Fig. 4.5(b). The percentage inaccuracy increases as v_d increases, yet its average value is only about 0.1 percent. For this study the physical parameters are $W_{fin} = 15\,\text{nm}$, $H_{fin} = 20\,\text{nm}$.

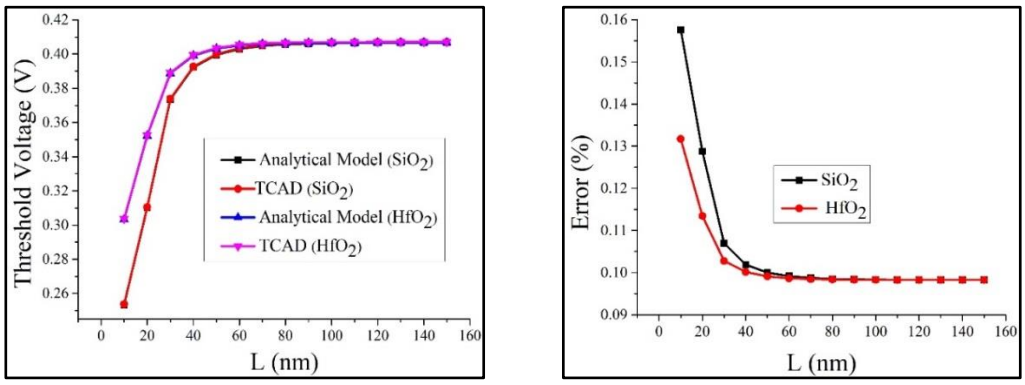


(a) **(b)**

Fig.4.5: For SiO_2 at different drain voltage (a) Change of V_T with channel length (b) Percentage error of V_T with channel length

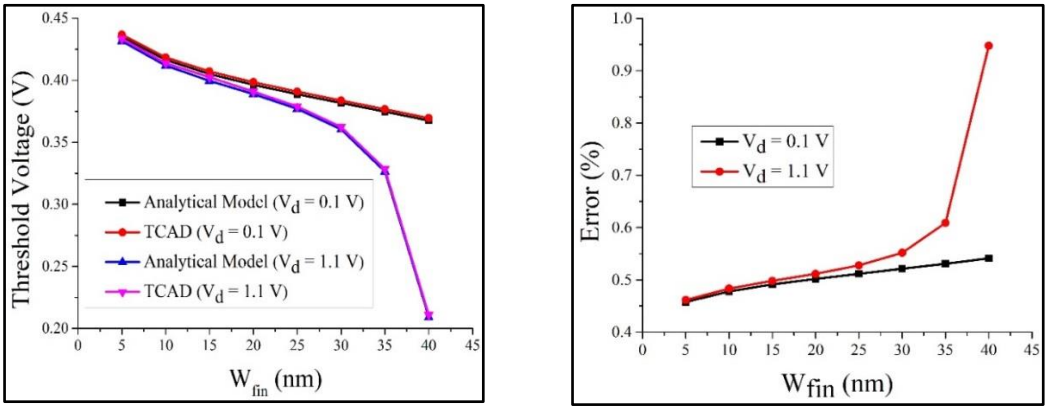
Fig.4.6 (a) compares the V_T for two dielectric materials. Up to 60 nm, it is observed that the V_T for both dielectric materials is nearly constant.; after that, it decreases rapidly for SiO_2. It is comparatively high for high-k material. The value of the 3rd term of the equation (4.28) is almost same for both dielectrics. But the 2nd term is much larger for SiO_2 material, as a result V_T is higher for high-k dielectric material. The similar type of characteristic was also reported in (Jung, 2020). The percentage error of V_T for two distinct oxide materials is practically following the same trend; however, the average value is greater for SiO_2 and it can be detected from Fig. 4.6(b). The study is done at $W_{fin} = 15\,\text{nm}$, $H_{fin} = 20\,\text{nm}$ and $v_d = 1.1\,\text{V}$.

The V_T variation with W_{fin} for two unlike drain voltages is shown in Fig.4.7 (a) for SiO_2 and in Fig.4.8(a) for HfO_2. Similar variations in V_T are noticed in both situations. Fig.4.7(b) and Fig.4.8(b) illustrate the percentage error of V_T with W_{fin} for two distinct oxide materials, and they are similar to one another with an average error of less than 1%. For both the studies the H_{fin} is 20 nm and L is 40 nm.



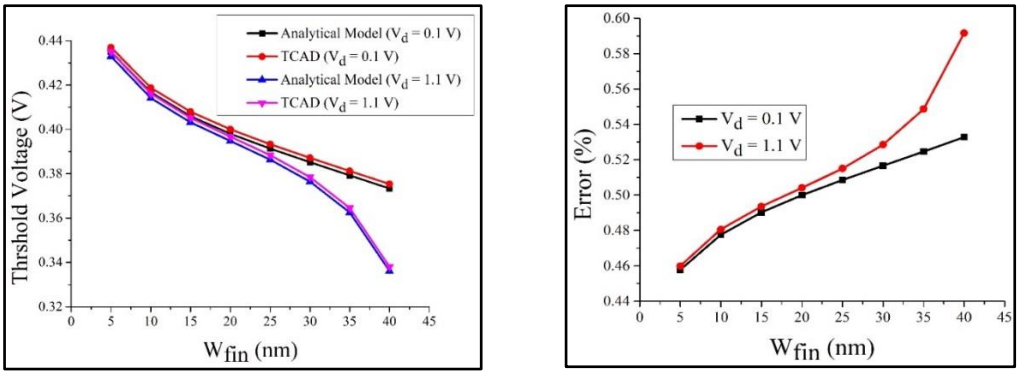
(a) **(b)**

Fig.4.6: V_T with channel length (a) Comparison between SiO_2 and HfO_2 (b) Percentage error



(a) **(b)**

Fig.4.7: For SiO_2 at different drain voltage (a) Change of V_T with W_{fin} (b) Percentage error of V_T with W_{fin}



(a) **(b)**

Fig.4.8: For HfO_2 at different drain voltage (a) Change of V_T with W_{fin} (b) Percentage error of V_T with W_{fin}

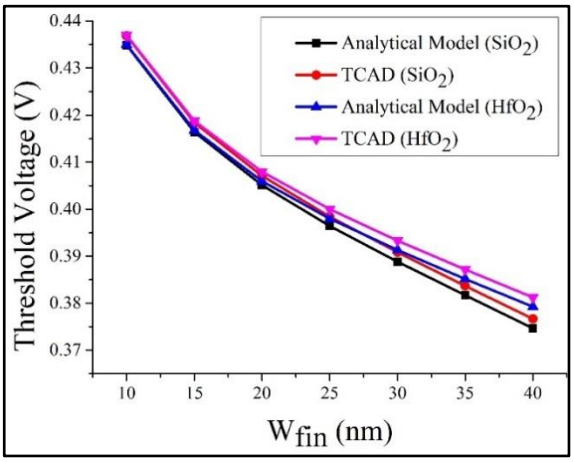
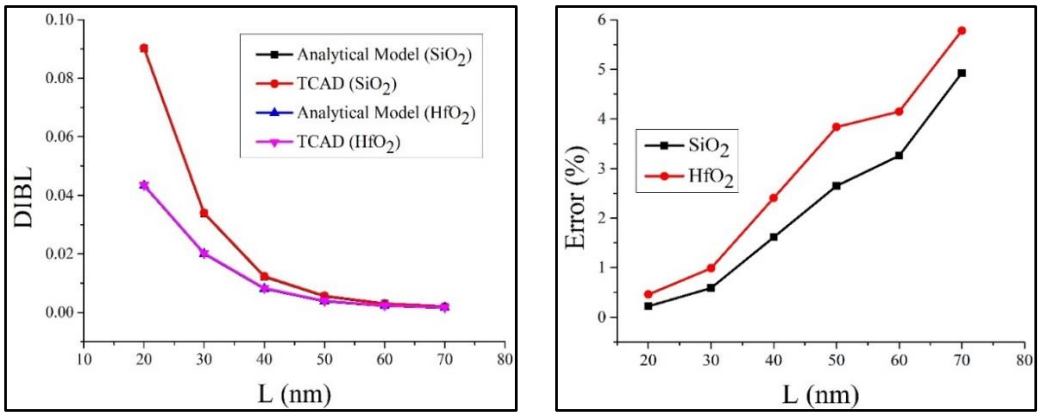


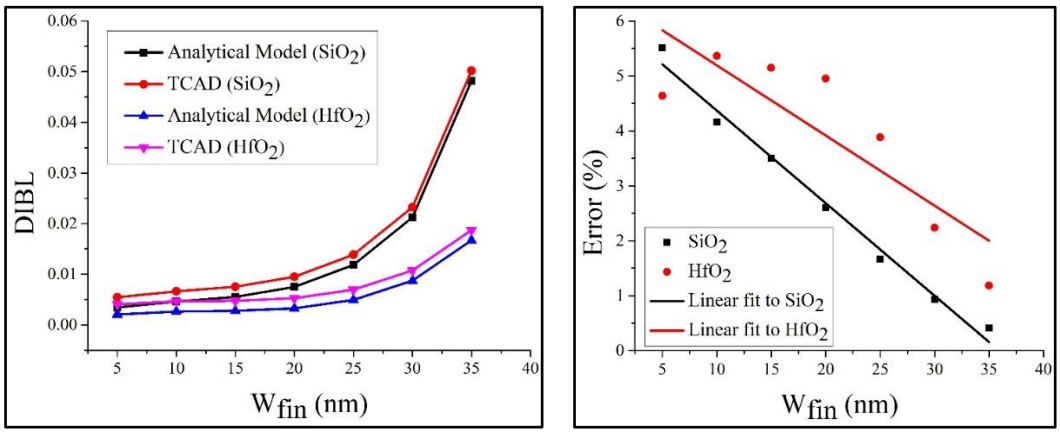
Fig.4.9: Comparison of V_T for SiO_2 and HfO_2 with device parameters $L = 40$ nm, $H_{fin} = 20$ nm and $v_d = 0.1$ V

The comparison of V_T for SiO_2 and HfO_2 for a static v_d is described in Fig. 4.9. The V_T decreases with W_{fin} increment, but a comparatively higher amount of V_T is obtained for HfO_2. The correctness of the model is also checked by calculating the DIBL coefficient. Fig.4.10(a) and Fig.4.11(a) show the variation of DIBL as a function of L and W_{fin}, respectively. To study the variation of DIBL with L, H_{fin} and W_{fin} are 20 nm and 15 nm respectively. Whereas, $L = 40$ nm and $H_{fin} = 20$ nm for viewing the change of DIBL with W_{fin}.



(a) **(b)**

Fig.4.10: DIBL with channel length (a) Comparison between SiO_2 and HfO_2 (b) Percentage error



(a) **(b)**

Fig.4.11: DIBL with W_{fin} (a) Comparison between SiO_2 and HfO_2 (b) Percentage error

All of the findings in this study are not only in close harmony with the results of the TCAD simulation, but they are also statistically connected. The well-known Pearson's product-moment correlation approach determines the correlation between simulation and analytical results. The correlation coefficient is near to 1; for instance, the correlation coefficient of simulated and analytical results of DIBL in reference to W_{fin} is 0.999986. As a result, simulation and mathematical modeling have a good relationship.

The V_T with respect to W_{fin} at a fixed $L = 60$ nm and of different fin heights is plotted in Fig.4.12. This analysis is done for SiO_2 at $v_d = 0.1\,\text{V}$ and $v_g = 0.4\,\text{V}$. It can be observed from Fig.4.7(a) that the gate terminal loses its control with the increment of W_{fin}. But the gate area will be increased with the increment of the H_{fin} and the gate regains its control. Hence, V_T improves. The analytical and simulation results support the above argument and the improvement of V_T is quite prominent.

Fig.4.13 provides a comparison of the two gate dielectric materials. It is clear that V_T for high-k material is higher while maintaining comparability with the other plots. The study is for $L = 60\,\text{nm}$, $H_{fin} = 30\,\text{nm}$ at $v_g = 0.4\,\text{V}$ and $v_d = 0.1\,\text{V}$.

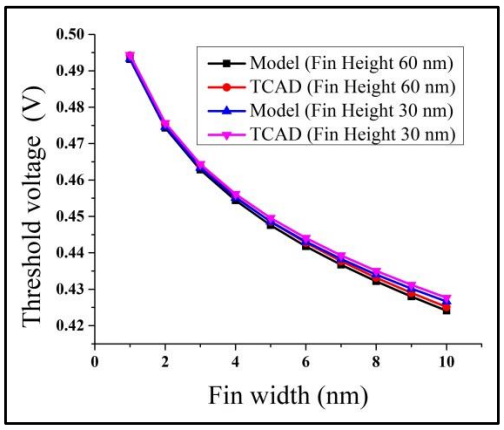


Fig.4.12: The change of V_T with W_{fin} for different fin heights for SiO_2

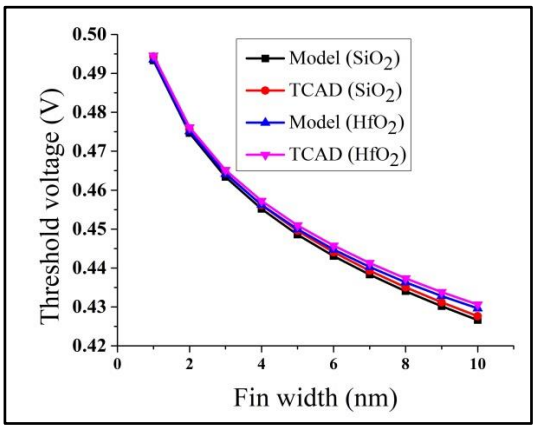


Fig.4.13: Comparison of V_T with fin width for two dielectric gate oxide

Similarly, Fig.4.14 indicates V_T variation with the W_{fin} at a fixed $H_{fin} = 60$ nm, $v_g = 0.4\,\text{V}$ and $v_d = 0.1\,\text{V}$ for different channel lengths. SCEs are dominant in the shorter L device and it will reduce V_T. This reduction of V_T can be visible for larger W_{fin}.

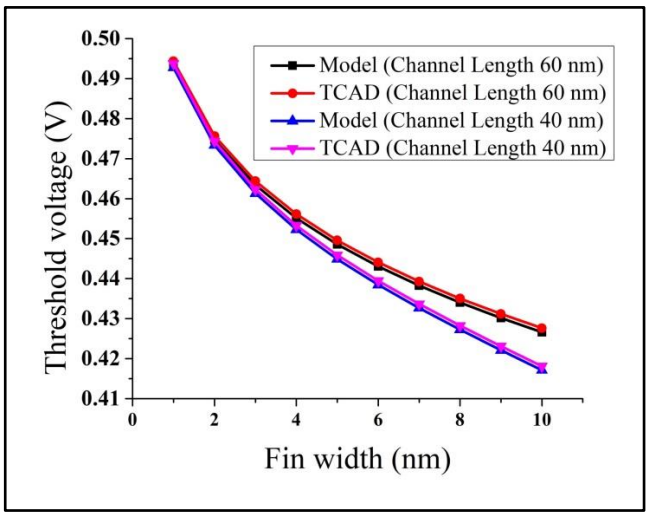


Fig.4.14: The change of V_T with fin width for different channel lengths for SiO_2

For the short channel device, such as the $L = 10\,\text{nm}$, the V_T is affected owing to the width quantization and it will be more than the V_T calculated by the classical

model. This argument is verified by Fig.4.15. The increment of V_T is 1.65% with respect to the classical theory. The study is done at $v_g = 0.4\,\text{V}$ and $v_d = 0.1\,\text{V}$.

The comparison of the V_T, including QME, between two dielectric materials is represented in Fig.4.16. The study V_T is also done at $v_g = 0.4\,\text{V}$ and $v_d = 0.1\,\text{V}$. The higher value of V_T has been obtained for high-k material and the similar trend is also followed under the influence of QM confinement.

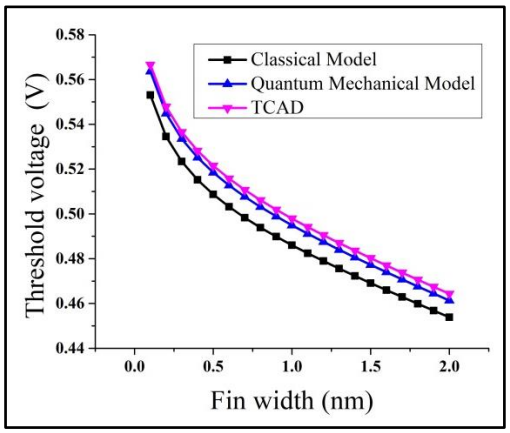


Fig.4.15: Comparison of the classical and quantum mechanical model of threshold voltage for SiO_2

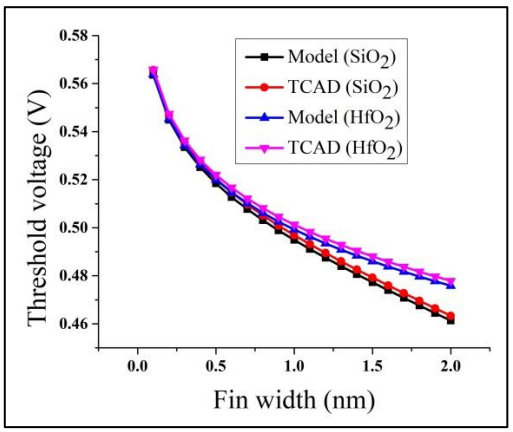


Fig.4.16: Comparison of the quantum mechanical model of V_T for two gate dielectric material

Fig. 4.17 illustrates the contrast between the classical and QM models of ΔV_T. The reflection of the increment of V_T due to the enhancement of the oxide thickness and energy quantization is echoed in ΔV_T. For $L = 10\,\text{nm}$ device v_g and v_d are kept constant at 0.4 V and 0.1 V respectively. The controllability of the gate terminal decreases with the increment of oxide thickness which results the sudden fall of the V_T for short channel device. This can be verified by Fig.4.18.

The ΔV_T for SiO_2 and HfO_2 is plotted in Fig.4.19 against W_{fin}. It is detected that the ΔV_T is less for HfO_2 material. For both two aforesaid studies v_g and v_d are kept constant at 0.4 V and 0.1 V respectively.

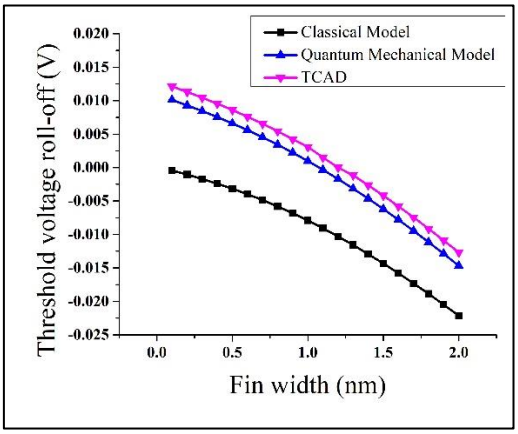


Fig.4.17: Change of ΔV_T with fin width using the quantum mechanical model for SiO_2

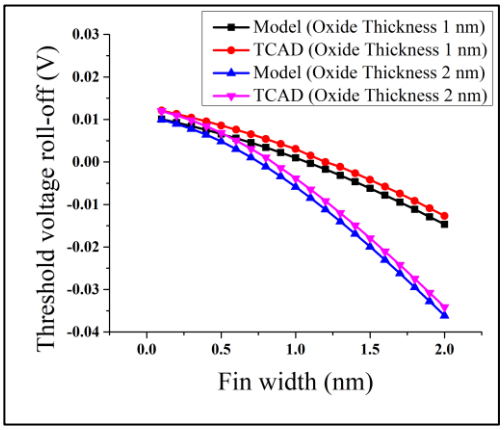


Fig.4.18: Variation of ΔV_T with fin width using the quantum mechanical model for SiO_2

The ratio L/W_{fin} is very important to determine the SCEs such as DIBL and SS. The gate loses its control, which increases the SS and DIBL for the larger W_{fin} because of the increment of fin volume and it can be observed from Fig.4.20. For $L = 10$ nm, the DIBL increases rapidly when the ratio falls below 6, i.e., W_{fin} more than 1.5 nm.

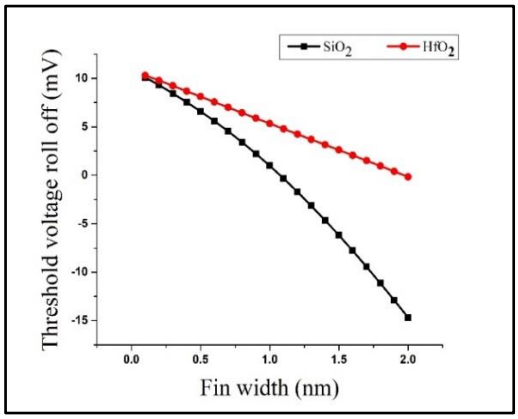


Fig.4.19: Comparison of ΔV_T with fin width using the quantum mechanical model for both dielectric materials

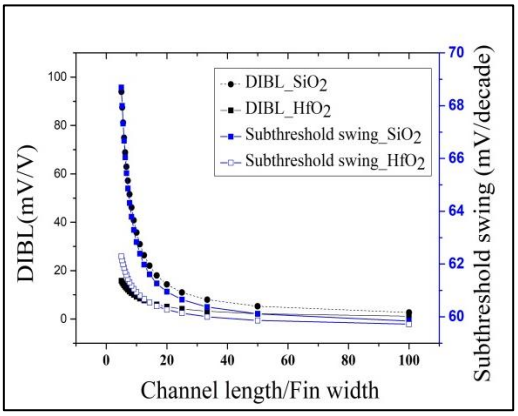


Fig.4.20: Effect of $\left(L/W_{fin}\right)$ ratio on DIBL and SS for both gate dielectric materials

The experimental result was obtained by A. Tsormpatzoglou et al. (Tsormpatzoglou et al., 2011) is quite similar to the theoretical V_T. In that study, V_T was around 0.304 V (for $L = 50$ nm, $H_{fin} = 65$ nm, and $W_{fin} = 25$ nm). The device used

HfO_2 as a gate oxide with a thickness of 1.7 nanometers. The same parameters are used to verify the current study, and $V_T = 0.35\,\text{V}$ has been obtained. The current work demonstrates that when high-k materials are used, Φ decreases and, as a result, V_T increases, even with the same t_{ox} of SiO_2 and HfO_2. However, when HfO_2 is used, the DIBL is lower than when SiO_2 is used. Therefore, the results indicate that HfO_2, which has a thicker oxide layer than SiO_2, has the same control over the channel, with superior SCE regulation, i.e., smaller DIBL. This model is also verified by the experimental result reported by Ritzenthaler et.al. (Ritzenthaler et al., 2011). For 50 nm channel the SS was approximately 81 mV/decade whereas using this model it is 86.687 mV/decade.

4.4 Summary

The V_T of TG-FinFET has been modelled by combining the of symmetric and asymmetric DG-FinFET using the perimeter-weighted sum method. The model was based on the inversion charge sheet method. The extra potentials induced in FinFET due to SCEs have been included to achieve better accuracy. A significant dependence of V_T on W_{fin} and H_{fin} have been observed due to the modulation of W_{eff} . The model has been examined for fin heights, 5 nm and 60 nm. The minimum and maximum W_{fin} were taken as 2 nm and 15 nm, respectively. The L was adjusted from 10 nm to 150 nm in order to explore how the V_T changes with regard to L . It can be observed that V_T is constant for long channel devices and it was approximately 0.4 V. The effect of the v_d on V_T was separately studied for W_{fin} and L .

The model also incorporates the QME for the device with $L = 10\,\text{nm}$. Due to the energy confinement of the charge carriers and the increment of the t_{ox} , V_T boosts up and it will not be modeled by classical analytical model. Therefore, by including the QME the difference between the two models has been explained clearly. The model has been investigated for different insulating materials, namely, SiO_2 and HfO_2. The comparison between the dielectrics has shown that the device with high-k material as a gate insulating material provides more immunity against the SCEs. The comparison

was done at $W_{fin} = 15\,\text{nm}$, $H_{fin} = 20\,\text{nm}$ and $v_d = 1.1\,\text{V}$. ΔV_T has been measured for 10 nm channel and roll-off is small for HfO_2 material. The difference between the classical and QM is also prominent in ΔV_T graph.

Due to DIBL, V_T has been reduced with the decrement of L. It was also a function of W_{fin} and L, though a less than 4% error was observed between simulation result and analytical result. The ratio $\left(L/W_{fin} \right)$ is an important metric to measure the SCEs of the short channel device. So, the DIBL and SS have been studied with respect to $\left(L/W_{fin} \right)$. It has been observed that DIBL increases rapidly when W_{fin} falls below 1.5 nm for the $L = 10\,\text{nm}$ structure. But the increment is not very rapid for HfO_2. Similar kind of trend has been found out for SS. The thorough comparison between TCAD simulation and analytical results and the validation of the model by the published experimental result proves the model's efficacy.

CHAPTER - 5

Drain Current

5.1. Introduction

The I_d is one of the well-recognized metrics for measuring device performance. To obtain I_d , v_d is applied at the drain terminal and v_g is applied at the gate terminal. When the gate to source voltage is greater than V_T , inversion layer is originated underneath the gate oxide. Due to the presence of the potential difference between drain and source, carriers are collected at the drain terminal and as a result, current flow from drain to source. In the frail inversion region, the current is due to the diffusion of the charge carriers; it depends exponentially on the gate to source voltage $\left(v_{gs}\right)$. In contrast, in the strong inversion condition I_d flows mainly due to the drift of the charge carriers.

For n-channel transistor, the drain is at a higher potential than the source. Therefore, the depletion layer is deeper in the drain side. Hence, the presence of larger number of N_A near the drain side reduces the electron concentration. Therefore, the channel thickness is not uniform. Initially I_d increases linearly with the increase of drain to source voltage. But at large v_d , all the electrons supplied by the channel are accumulated to the drain terminal, which results in a saturated I_d for a specific v_g . The v_d at which saturation occurs is known as drain saturation voltage $\left(v_{dsat}\right)$. This

voltage is required to find the V_{def}, which is a function of v_g only. Therefore, drain characteristics consist of two distinct regions, the linear region and the saturation region. The depletion region gets wider with increase of v_d and causes the shrinkage of the actual L, causing CLM. At sufficiently high v_d, the large lateral electric field saturates the carrier velocity and they become field independent. This phenomenon is less prominent for devices with longer channels as a result; the characteristic curves are almost parallel to each other for different gate-source voltages. But for short channel devices, the large v_d not only creates CLM but generates other SCEs. Therefore, the drain characteristic curves are not parallel to each other.

FinFET technology experiences difficulty in scaling W_{fin} at 7 nm node to reach the increased packing density. FinFETs have been reported in various structures due to their improved electrical characteristics. In DG-FinFETs, the SCEs and switching capacitance eventually improve as reported in (Datta et al., 2007; Tripathi, Mishra, & Mishra, 2012). Compared with the DG structure, TG-FinFET reduces SCEs to a greater extent and delivers a larger amount of driving current (J. G. Fossum, 2007; Yamamoto, Hidaka, Nakamura, Sakuraba, & Masuoka, 2006). TG-FinFET is considered to be the most power-efficient device and it also provides high gain. It is reported that 22 nm 3-D TZ-FinFET offers 37% superior performance than 32 nm 2-D planar transistor. The power consumption of the device is 50 % less than the planar structure (Bohr & Mistry, 2011). In sub-28 nm regime, an n-channel TG-FinFET is acknowledged as a potential candidate for traditional planar bulk devices and its performances are described (Pavanello et al., 2007). A FinFET structure with multiple fins and limited width is designed to drive a high current. But limited width causes width quantization in the FinFET (Nowak et al., 2004). When the width of the fin is less than 10 nm, the charge carriers can be modelled as one dimension electron gas (1DEG) in the channel and are free to roam along the channel direction only. This causes the formation of energy sub-bands and the distribution of the charge carriers in the silicon film is pointedly different from the prediction of the classical theory. In this case, the inversion layer is not localized at the silicon film's surface but extends in the "depth" of the film. This phenomenon is known as volume inversion. It was revealed by Balestra et al. in 1987 (Balestra, Cristoloveanu, Benachir, Brini, & Elewa, 1987).

By properly resolving the Schrödinger and Poisson equations, volume inversion is anticipated. Volume inversion carriers experience smaller interface scattering compared to those in a surface inversion layer, resulting in an increment of g_m and μ . The random variation in V_T (N Fasarakis et al., 2011) is also a direct outcome of volume inversion in thin-film devices. It also influences the device's high-frequency characteristics and raises the leakage current (N Fasarakis et al., 2011). Stressing and width quantization in n/p type high-k/metal TG-FinFET was reported in (W.-K. Yeh et al., 2016).

An acceptable electrostatic command on the variation of the W_{fin} was obtained by a heavily dopped stopper (Xu, Sun, Xiong, Cleavelin, & Liu, 2010). The impact of W_{fin} on device capability was stated for SOI FinFET (C. D. Young et al., 2015) and gate-first metal inserted poly-Si stack Gate FinFET (J.-W. Han, J. Lee, D. Park, & Y.-K. Choi, 2007). The effect of hot carriers on n-FinFET with wide W_{fin} have been discussed (Nathanael, Xiong, Cleavelin, & Liu, 2008). In opposition, NBTI can be found in p-FinFET with comparatively smaller W_{fin} (Lee et al., 2009; C. D. Young et al., 2015).

The effective channel length $\left(L_{eff}\right)$ of ultra-thin body underlap-FinFET was reported and it depends on the biasing situation (J. G. Fossum, 2007; Kim, Fossum, & Yang, 2006; Trivedi et al., 2004) . The underlap regions effectively increase the L and improve SCEs (J. G. Fossum, 2007). The improved g_m and low fringing capacitance of underlap-FinFETs make them attractive for the analogue/RF application (Kranti & Armstrong, 2007; Kranti, Burignat, Raskin, & Armstrong, 2010). It was reported that current gain in the order of 10^8 was achieved for DG heterojunction tunnel FinFET (Maity, Maity, & Baishya, 2019).

The SCEs such as DIBL, SS, ΔV_T are better controlled by TG-FinFET than the planar MOSFET (Abd El Hamid, Guitart, & Iñíguez, 2007; Q. Chen et al., 2003; Jiménez, Iñíguez, Suñé, & Sáenz, 2004; S.-H. Oh, Monroe, & Hergenrother, 2000). Moreover, HfO_2 as a gate insulator shows a substantial reduction of SCEs. These SCEs are noticeable if the L and space charge region of the source and drain junction are

consistent (Kahng, 1960). The lightly doped or undoped ultrathin channel is favored to reduce the adverse effect of mobility degradation (Ghani et al., 2000), random microscopic fluctuations of dopant atoms and corner effect. Because of the effects of charge-sharing between two neighboring gates, an early inversion can develop at the corners of SOI MG devices. In addition to a kink in the subthreshold properties, the occurrence of two distinct V_T, one in the corners and the other at the sidewall or top Si-SiO_2 interfaces, was reported in (Ushiki, Kotani, Funaki, Kawai, & Ohmi, 2000). Therefore, the subthreshold $I_d - v_g$ characteristics of a device is also affected by the corner effect. The W_{fin} equals two-third of the gate length and H_{fin} equals three times more than the W_{fin} providing realistic results (Riddet, Alexander, Brown, Roy, & Asenov, 2010).

This chapter proposes an analytical I_d model in the strong inversion area and validates it with TCAD simulation. The V_T, including QME, is used to model I_d. To remove the discontinuity in I_d. transition from the linear to saturation zone, a V_{def} is employed. The LambertW function is employed to demonstrate the inversion charge. CLM, saturation velocity, the effect of series resistance and μ_{eff} are also included in the mathematical modeling. The detailed formulation of g_d and the g_m has also been gleaned from the I_d equation. The effect of the high-k (HfO_2) has also been examined.

5.2. Analytical Model for Drain Current

For FinFET, the 2-D Poisson's equation including the inversion carrier charge density can be stated as (H. Lu & Taur, 2006).

$$\frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i \exp[q(\Phi - v_q)/KT] \tag{5.1}$$

$\Phi(x, y)$ indicates the potential of the channel. ε_{si} is the permittivity of Si. n_i is intrinsic carrier concentration and v_q is quasi-fermi potential. Maintaining the gradual

channel approximation v_q is maintained as constant in the x-direction or perpendicular to the channel. Following (H. Lu, Yu, & Taur, 2008), Φ can be written as,

$$\Phi = v_q - \left[2\frac{KT}{q} \ln\left\{ \frac{H_{fin}}{2\beta_y} \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} KT}} \cos\left(\frac{2\beta_y x}{H_{fin}} \right) \right\} \right] \tag{5.2}$$

β_y is a function of y. Differentiating equation (5.2) with respect to x,

$$\frac{d\Phi}{dx} = 4\frac{KT}{qH_{fin}} \beta_y \tan\left(\frac{2\beta_y x}{H_{fin}} \right) \tag{5.3}$$

Using the boundary condition of Gauss's law,

$$\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{v_g - \phi_{ms} - \Phi}{t_{ox}} = \frac{d\Phi}{dx} \tag{5.4}$$

$$\text{At } \; x = \frac{H_{fin}}{2}, \; \frac{d\Phi}{dx} = 4\frac{KT}{qH_{fin}} \beta_y \tan\beta_y \tag{5.5}$$

Equating equation (5.4) & (5.5),

$$\frac{q}{2KT}\left(v_g - \phi_{ms} - v_q \right) - \ln\left(\frac{2}{H_{fin}} \sqrt{\frac{2\varepsilon_{si} KT}{q^2 n_i}} \right) = \ln\beta_y - \ln\left(\cos\beta_y \right) + 2A\beta_y \tan\beta_y \tag{5.6}$$

Here, $A = \dfrac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} H_{fin}}$ is a constant, ϕ_{ms} is the work function difference between semiconductor and gate. ε_{ox} is the permittivity of oxide and t_{ox} is the thickness of the oxide layer. Now, $\ln\beta_y - \ln\left(\cos\beta_y \right) = \ln\beta_y + \ln\left(\sin\beta_y \right) - \ln\left(\sin\beta_y \right) - \ln\left(\cos\beta_y \right)$

$$\therefore \ln\beta_y - \ln\left(\cos\beta_y \right) = \ln\left(\beta_y \tan\beta_y \right) - \ln\left(\sin\beta_y \right) \tag{5.7}$$

Hence, equation (5.6) will be,

$$\frac{q}{2KT}\left(v_g - \phi_{ms} - v_q \right) - \ln\left(\frac{2}{H_{fin}} \sqrt{\frac{2\varepsilon_{si} KT}{q^2 n_i}} \right) = \begin{pmatrix} \ln(\beta_y \tan\beta_y) - \ln\left(\sin\beta_y \right) \\ +2A\beta_y \tan\beta_y \end{pmatrix} \tag{5.8}$$

In strong inversion condition, β_y is close to $\frac{\pi}{2}$ (H. Lu et al., 2008), applying this condition equation (5.8) reduces to

$$\frac{q}{2KT}\left(v_g - \phi_{ms} - v_q\right) - \ln\left(\frac{2}{H_{fin}}\sqrt{\frac{2\varepsilon_{si}KT}{q^2 n_i}}\right) = \ln\left(\beta_y \tan\beta_y\right) + 2A\beta_y \tan\beta_y \quad (5.9)$$

The term $\beta_y \tan\beta_y$ indicates the normalized inversion sheet charge density $\left(q_{ip}\right)$. It is represented as $\beta_y \tan\beta_y = q_{ip} = \frac{qQ_{ip}H_{fin}}{4\varepsilon_{si}KT}$, where $Q_{ip}(y)$ is the sheet charge density. Therefore, equation (5.9) is reduced as,

$$\frac{q}{2KT}\left(v_g - \phi_{ms} - v_q\right) - \ln\left(\frac{2}{H_{fin}}\sqrt{\frac{2\varepsilon_{si}KT}{q^2 n_i}}\right) = \ln\left(q_{ip}\right) + 2Aq_{ip} \quad (5.10)$$

Following (Tsormpatzoglou et al., 2010), the analytical solution of equation (5.10) in terms of LambertW function can be written as,

$$q_{ip} = \frac{1}{2A} LambertW\left(e^{\frac{v_g - V_T - v_q}{2v_{th}}} \frac{e^{\frac{v_g - V_T - v_q}{2\eta_{TG}v_{th}}}}{C + e^{\frac{v_g - V_T - v_q}{2\eta_{TG}v_{th}}}}\right) \quad (5.11)$$

where $C = 4\dfrac{\exp\left(\dfrac{V_T + v_{fb}}{n}\right)}{\exp(n_1)}$ (5.12)

Here, n_1 is constant, $n = 1\,\mathrm{V}$ is a normalizing factor, and v_q is the flat band voltage. As v_q is the quasi-fermi potential, it varies along the channel direction and changes from source ($v_q = v_s\,\mathrm{V}$) to the drain ($v_q = v_d\,\mathrm{V}$). The modified *SS* coefficient for the TG-FinFET is denoted by η_{TG} (N Fasarakis et al., 2011).

$$\eta_{TG} = \frac{\eta}{2 - \eta} \quad (5.13)$$

TG-FinFET's *SS* coefficient is indicated by η. It is denoted as $\eta = SS \big/ v_{th} \ln(10)$. So, it will be,

$$\eta = \frac{1}{1-\left[M_{1TG} + M_{2TG}\right]} \tag{5.14}$$

The expressions of M_{1TG} and M_{2TG} have been derived in chapter 4. At the source end $v_q = 0\,\text{V}$, so, at the source, normalized inversion charge density in terms of LambertW function will be,

$$LambertW\left(e^{\frac{v_g - V_T}{2v_{th}}} \frac{e^{\frac{v_g - V_T}{2\eta_{TG} v_{th}}}}{C + e^{\frac{v_g - V_T}{2\eta_{TG} v_{th}}}} \right) = q_s \tag{5.15}$$

By the same token, at the drain $v_q = v_d$,

$$LambertW\left(e^{\frac{v_g - V_T - v_d}{2v_{th}}} \frac{e^{\frac{v_g - V_T - v_d}{2\eta_{TG} v_{th}}}}{C + e^{\frac{v_g - V_T - v_d}{2\eta_{TG} v_{th}}}} \right) = q_d \tag{5.16}$$

According to (Sheu, Scharfetter, Ko, & Jeng, 1987), I_d can be written as,

$$I_d = \mu_o W_{eff} \frac{4\varepsilon_{si} KT}{q H_{fin} L} \int_0^{v_d} q_{ip} dv_q \tag{5.17}$$

Here, the W_{eff} is defined as $W_{eff} = W_{fin} + 2H_{fin}$. μ_0 is the low electric field electron mobility. Now, dv_q is obtained by differentiating equation (5. 10) and it will be,

$$dv_q = -2\frac{KT}{q}\left(2A + \frac{1}{q_{ip}}\right) dq_{ip} \tag{5.18}$$

Now, replacing dv_q by dq_{ip} and changing the limits of equation (5.17), I_d will be,

$$I_d = 2\left(\frac{KT}{q}\right)^2 \mu_o W_{eff} \frac{4\varepsilon_{si}}{H_{fin} L} \int_{q_d/2A}^{q_s/2A} q_{ip}\left(2A + \frac{1}{q_{ip}}\right) dq_{ip} \tag{5.19}$$

Now the result of integrating the aforementioned equation become,

$$I_d = 2\left(\frac{KT}{q}\right)^2 \mu_o W_{eff} \frac{4\varepsilon_{si}}{H_{fin} L}\left[A\left\{\left(\frac{q_s}{2A}\right)^2 - \left(\frac{q_d}{2A}\right)^2\right\} + \left(\frac{q_s}{2A} - \frac{q_d}{2A}\right)\right] \tag{5.20}$$

The I_d will be utilizing the value of A and simplified as,

$$I_d = \left(2v_{th}\right)^2 \frac{\mu_o W_{eff}}{L} C_{ox}\left[\frac{1}{2}\left(q_s{}^2 - q_d{}^2\right) + \left(q_s - q_d\right)\right] \tag{5.21}$$

After the pinch-off situation, the L continually decreases as the v_d rises. i.e., $v_d > \left(v_g - V_T\right)$. This leads to CLM. Hence, L_{eff} will be $L_{eff} = L - \Delta L$. The channel reduction due to CLM is indicated by ΔL, using the notion of (Y Tsividis & McAndrew, 2011), it is framed as,

$$\Delta L = \lambda_{eff} \ln\left[\frac{\left\{V_{def} - \left(v_g - V_T\right)\right\}}{\lambda_{eff} E_p} + 1\right] \tag{5.22}$$

The effective natural length $\left(\lambda_{eff}\right)$ can be narrated in respect of λ of the symmetric and asymmetric kind of DG-FinFET, i.e., λ_{sym} and λ_{asym} respectively (Mohan Vamsi Dunga, 2008), as interpreted earlier in chapter 3.

$$\lambda_{eff} = \frac{2\lambda_{sym}\lambda_{asym}}{\sqrt{4\lambda_{asym}^2 + \lambda_{sym}^2}}. \tag{5.23}$$

It determines how far the electric field lines must travel to penetrate the device's body from the drain. It indicates the control of the drain on the depletion region. In equation (5.22), E_P is the electric field in the pinch-off region close to the drain and characterized as (Y Tsividis & McAndrew, 2011) ,

$$E_p = \sqrt{\left\{\frac{V_{def} - \left(v_g - V_T\right)}{\lambda_{eff}}\right\}^2 + \left(\frac{v_{sat}}{\mu_0}\right)^2}$$

(5.24)

In light of (Tsormpatzoglou et al., 2010) , to avoid the problem of discontinuity at $v_d = \left(v_g - V_T\right)$, the V_{def} is considered as,

$$V_{def} = (v_g - V_T) + \left[\left(1 + v_d\right) - \left(v_g - V_T\right)\right]\left[1 - \frac{2\exp(-J)}{\exp(J) + \exp(-J)}\right] \quad (5.25)$$

where, $J = \left(\frac{v_d}{1 + \left(v_g - V_T\right)}\right)^2$. Hence, incorporating the consequence of V_{def} and the CLM the revised I_d equation will be,

$$I_d = \left(2v_{th}\right)^2 \mu_0 W_{eff} C_{ox}\left[\frac{1}{2L_{eff}}\left(q_s{}^2 - q_d{}^2\right) + \frac{1}{L}\left(q_s - q_d\right)\right] \quad (5.26)$$

Using (Tsormpatzoglou et al., 2012), the μ_{eff} in respect of normalized inversion charge density will be,

$$\mu_{eff} = \frac{\mu_0}{1 + \varsigma_1 q_s v_{th}} \quad (5.27)$$

Here $\varsigma_1 = \varsigma_0\left(1 + \frac{\mu_0 v_d}{v_{sat} L_{eff}}\right) + \frac{\mu_0 2W_{eff}\varepsilon_{ox} R}{L_{eff} t_{ox}}$ is the 1st order μ_0 attenuation coefficient and linear μ_0 attenuation coefficient is symbolized as ς_0. Surface scattering is not considered in this study, hence, ς_0 is taken as zero. Here, the series resistance is indicated by R. Therefore, including μ_{eff} equation (5.26) will be modified to,

$$I_d = \left(2v_{th}\right)^2 \mu_{eff} W_{eff} C_{ox}\left[\frac{1}{2L_{eff}}\left(q_s{}^2 - q_d{}^2\right) + \frac{1}{L}\left(q_s - q_d\right)\right] \quad (5.28)$$

So, equation (5.28) indicates the I_d for the TG-FinFET. But the structure of the device indicates the formation of a quantum well inside the channel. Hence, QM confinement must be an integrated part of this $L = 10$ nm device. The impact of QME has been already incorporated into the threshold model and discussed in chapter 4. Therefore, including the V_{T_QM} a more accurate I_d is achieved. But, as the equation (5.28) does not contain V_T directly, it is not modified. Following the approximation used by (Tsormpatzoglou et al., 2012), at widespread of v_g and low v_d $(v_d \to 0)$, q_d can be written as,

$$q_d \approx q_s - \frac{v_d}{2v_{th}} \tag{5.29}$$

Using the above approximation, equation (5.28) will be,

$$I_d = (2v_{th})\frac{\mu_{eff} W_{eff}}{L} C_{ox} v_d + \frac{2v_{th}\mu_{eff} W_{eff}}{L} C_{ox} v_d q_s - \frac{\mu_{eff} W_{eff}}{2L} C_{ox} v_d^2 \tag{5.30}$$

Therefore, differentiating equation (5.30) with respect to v_d, g_d has been calculated as,

$$g_d = 2v_{th}\frac{\mu_{eff} W_{eff}}{L} C_{ox}\left(1 + q_s - \frac{v_d}{2v_{th}}\right) \tag{5.31}$$

Similarly, g_m has also been obtained by differentiating equation (5.30) in respect of v_g. It is important to notify that q_s determined by LambertW function is the single term that contains v_g. Thus, using the differentiation property of the LambertW function g_m is formulated as,

$$g_m = \frac{Dq_s}{(1+\varsigma_1 q_s v_{th})^2 (1+q_s)}\left[1 - \varsigma_1 v_{th} + \frac{v_d \varsigma_1}{4}\right] \tag{5.32}$$

where, $D = \dfrac{2v_{th}\mu_0 W_{eff} C_{ox} v_d}{L}$ is a constant. Hence, I_d model is established and is verified in the result section.

5.3. Results and Discussions

The channel's doping concentration is kept low to circumvent random dopant variation. To avoid the bottom gate interaction with the side gates, t_{oxb} is taken bigger than the channel thickness.

To keep the similarity with the Φ and V_T model, interface charge density and work function difference between semiconductor and metal have been kept at zero. The relation $W_{fin} < 0.7L$ and $W_{fin} < {H_{fin}}/{2}$ are maintained throughout the study to obtain realistic results (N Fasarakis et al., 2011) .

The plot of I_d with variation of v_d for multiple values of v_g, has been rendered in Fig.5.1. The drain characteristic has been obtained for two different gate voltages. It follows the conventional MOSFET theory, i.e., the accumulation of electrons in the inversion layer increases with the increment of v_g, leading the current to saturate at a higher value.

Table 5.1: Design Parameter Values for Drain Current

SI.	Design Parameters	Value
1.	N_A - Uniform body doping concentration	1.45×10^{16} m^{-3}
2.	N_D - Source/ Drain doping concentration	10^{26} m^{-3}
3.	t_{ox} - Gate oxide thickness	1 nm
4.	t_{oxb} - Bottom oxide thickness	100 nm
5.	v_{sat} - saturation velocity	10^5 m/sec
6.	μ_0 - Low electric field electron Mobility	200×10^{-4} m^2/V.Sec
7.	m_0 - Free electron mass	9.01×10^{-31} Kg
8.	m^* - Isotropic effective mass	6.37×10^{-31} Kg

Initially, I_d increases in a linear fashion with the v_d and this part of the characteristic curve is known as the linear region. But when the v_d is equal to the difference between the v_g and V_T, gate to channel voltage is identical to V_T. Hence, the inversion charge begins to disappear at the drain end and the I_d starts to saturate. The channel achieves pinched off state at this point of time, and the I_d becomes constant. This region of the characteristics curve is called the saturation region.

From I_d equation, it can be stated that the I_d is linear function of the C_{ox}. Therefore, I_d should saturate at a higher value when the high-k material replaces SiO_2. As t_{ox} remains the same for both the dielectrics, better capacitive coupling is achieved for HfO_2. So, I_d saturates at higher value for high-k dielectric material, which can be validated in Fig.5.2. $I_d = 53.5\,\mu A$ for HfO_2 and 38 µA for SiO_2 has been obtained for a $L = 10\,nm$ with $W_{fin} = 2\,nm$ and $H_{fin} = 10\,nm$. These values have been taken at $v_g = 1.02\,V$ and $v_d = 1\,V$.

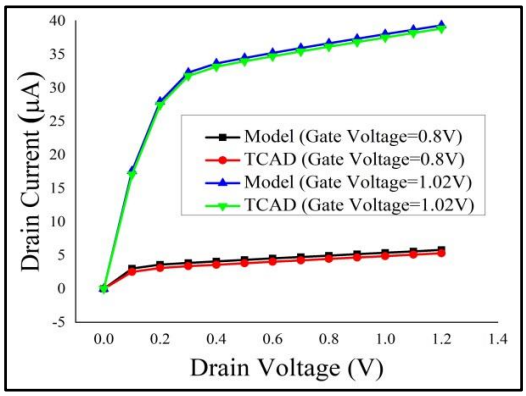


Fig.5.1: Drain characteristics at different gate voltage for SiO_2

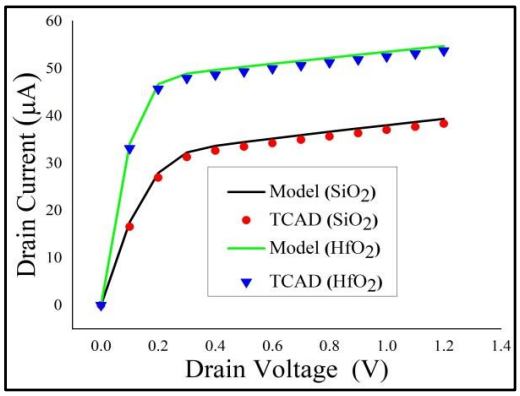


Fig.5.2: Comparison of drain current for two gate oxides

The effect of W_{fin} and H_{fin} are also studied for this short channel device. Fig.5.3 depicts the variation of drain characteristics with the two different fin widths. As the higher amount of v_g is required to create the inversion layer in the smaller W_{fin} device, hence with the same amount of v_g, more electrons are accumulated in the inversion channel, which in turn indicates that I_d will saturate at a large value for

broader W_{fin} device. The length of the channel and height of the fin are kept constant at 10 nm. The study was done at $v_g = 0.8\,\text{V}$.

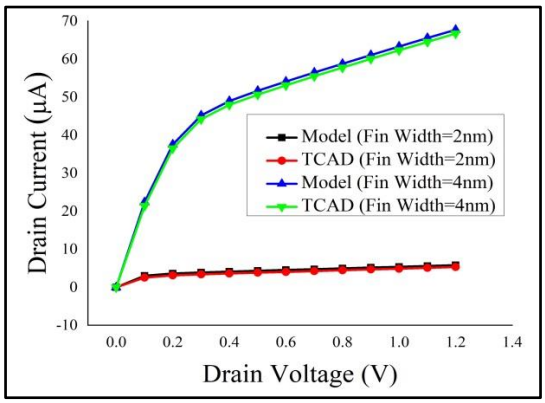


Fig.5.3: Drain characteristics at two different fin widths at for SiO_2

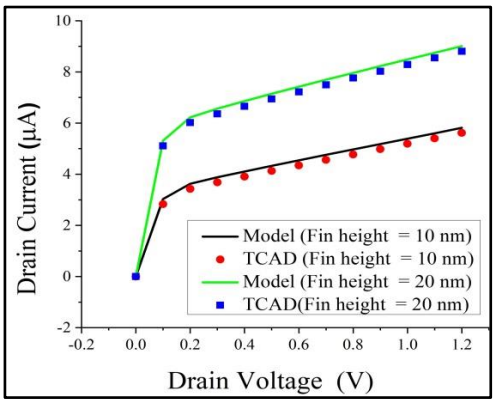


Fig.5.4: Drain characteristics at two different fin heights for SiO_2

The higher the H_{fin}, the more fringing field is produced, which raises Φ and thus the inversion charge density. As a result, I_d increases with H_{fin}, as shown in Fig.5.4. Here, also the L was 10 nm. The v_g and W_{fin} are taken as 0.8 V and 2 nm, respectively.

The transfer characteristic at two different channel lengths is shown in Fig.5.5. The height and width of the device fin are taken as 10 nm and 2 nm, respectively. The v_d is kept constant at 0.1 V. It has been observed that I_{OFF} and I_{ON} both increase for short channel device. The effect of W_{fin} can be observed in Fig.5.6. The gate control diminishes with an increment of W_{fin} because the gate loses its control over the mid-point of the channel. Therefore, the I_{OFF} is higher for $W_{fin} = 4\,\text{nm}$ device and it is in the order of 10^{-12}A. On the other hand, I_{OFF} is approximately 10^{-17}A for $W_{fin} = 2\,\text{nm}$ device. For this study L and H_{fin} are fixed at 10 nm. Here, also $v_d = 0.1\,\text{V}$.

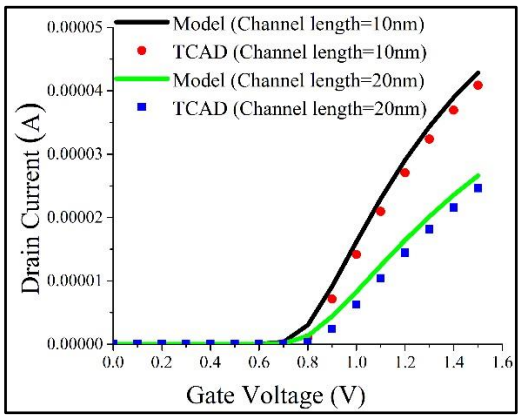


Fig.5.5: Transfer characteristics at two distinct channel lengths, for SiO_2

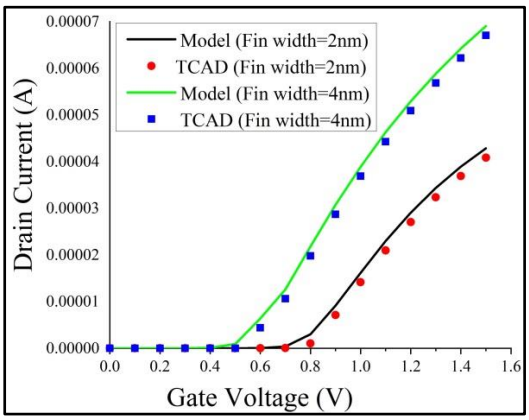


Fig.5.6: Transfer characteristics for various fin widths for SiO_2

The transfer characteristic at two distinct drain voltages is shown in Fig.5.7. Due to the charge-sharing effect in the broader space charge region, the I_{OFF} rises with v_d. The experiment is conducted on the device with $L = 10$ nm, $H_{fin} = 10$ nm and $W_{fin} = 2$ nm.

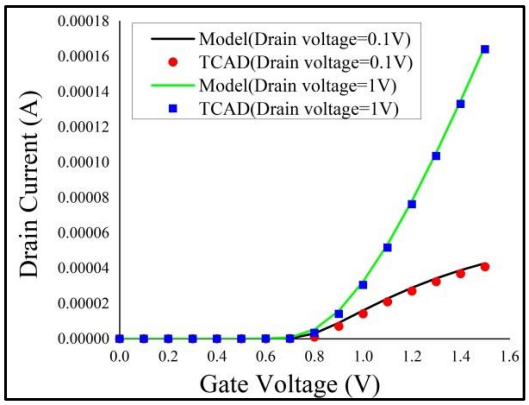


Fig.5.7: Transfer characteristics with drain voltages as parameter for SiO_2

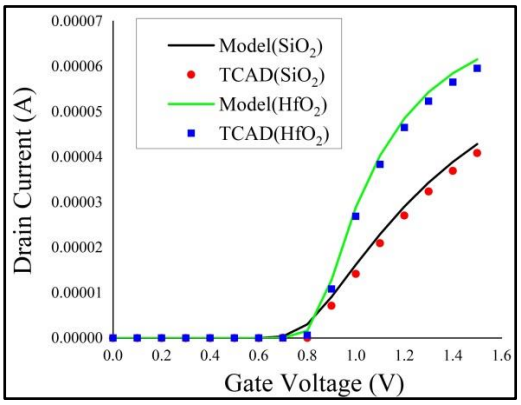


Fig.5.8: Comparison of transfer characteristics for two gate dielectrics

The comparison of the transfer characteristics depending on the two gate dielectric materials has been shown in Fig.5.8. At $W_{fin} = 2$ nm, $I_{OFF} = 10^{-17}$ A and $I_{ON} = 10^{-5}$ A for SiO_2. Thus, the gain I_{ON}/I_{OFF} will be 10^{12}. On the other hand, the I_{ON}/I_{OFF} ratio is 10^{14} for HfO_2. It can also be observed that the off current value is

much less for high-k dielectric material. To measure the transfer characteristics, the H_{fin} and v_d are kept constant at 10 nm and 0.1 V.

The g_m versus v_g with v_d as a parameter is plotted in Fig.5.9. The g_m measures the amplification of the device. It can be observed that at $v_d = 1\,\text{V}$ the g_m initially increases with the v_g and attains a maximum value at 0.9 V, after which it decreases. At higher v_g, enhanced surface scattering degrades μ of the charge carriers in the channel, reducing the g_m with the further increment of v_g. The equation (5.32) shows that the 1st term of g_m is proportional to v_d and the 3rd term is proportional to the square of the v_d, as a result the g_m curve shifts upward for larger v_d. The device comprises $L = 10\,\text{nm}$, $W_{fin} = 2\,\text{nm}$ and $H_{fin} = 10\,\text{nm}$.

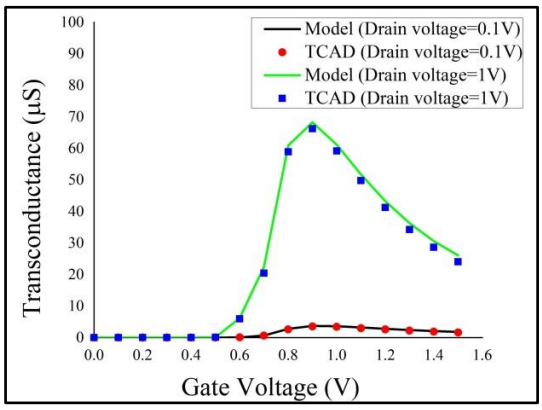


Fig.5.9: Ttransconductance with v_d for SiO_2

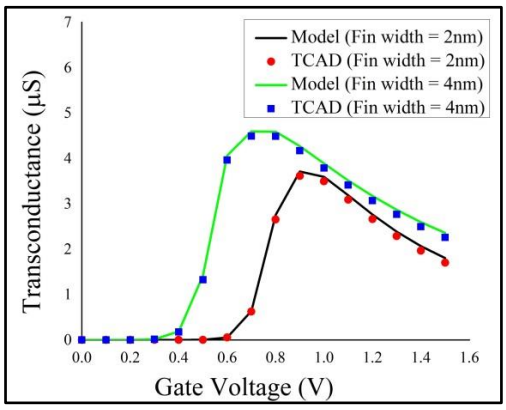


Fig.5.10: Ttransconductance with two fin widths for SiO_2

As W_{fin} shrinks, fin volume shrinks, increasing source and drain resistance and decreasing inversion charge density (Dixit et al., 2005). As shown in Fig. 5.10, the g_m with v_g plot can also be used to visualize this phenomenon. The value of maximum transconductance $\left(g_{m\_\max}\right)$ is 4.59 μS for $W_{fin} = 4\,\text{nm}$. On the other hand, it is 3.71 μS for 2 nm and it can also be observed that $g_{m\_\max}$ is achieved at a higher v_g for a lower W_{fin} device. The L and H_{fin} are kept constant at 10 nm and the v_d was kept 0.1 V.

The comparison of g_m for SiO_2 and HfO_2 is shown in Fig.5.11. Equation (5.32) indicates that it is proportional to the gate oxide. Hence, as the t_{ox} is the same for both the dielectric, the capacitance value will be higher for HfO_2, leading to the g_m increment. The improved g_m peak indicates the better charge controllability of the high-k gate insulating material. The study is conducted on a device consisting of length of channel as 10 nm, $H_{fin} = 10$ nm, $W_{fin} = 2$ nm. v_d is fixed at 1 V.

The I_d indicates the device's power dissipation, whereas g_m indicates the amplification factor of the device. The ratio g_m / I_d is a quality factor of the device and a higher value will be more useful for analogue applications. It is also known as the TGF. From Fig.5.12, it can be observed that the curve is almost flat up to the device's V_T and after that decreases with the increment of the v_g. For a device with $W_{fin} = 4$ nm, V_T is approximately 0.5 V; hence the curve is almost constant up to 0.5V; a similar argument is valid for the device with $W_{fin} = 2$ nm. In this case also L and H_{fin} both are kept constant at 10 nm and v_d is fixed at 0.1 V.

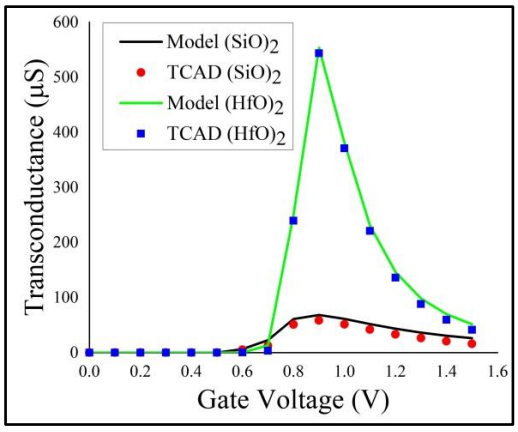


Fig.5.11: Comparison of transconductance for two gate oxide materials

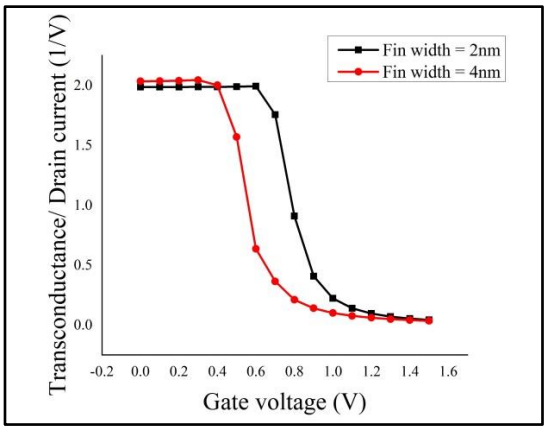


Fig.5.12: Transconductance/ Drain current with gate voltage for SiO_2

To check the model's accuracy, g_d has also been studied. CLM and DIBL are the two major SCEs that affect g_d. Equation (5.31) indicates that g_d is inversely proportional to L. Hence, it should be decreased with the increment of L. The study was conducted on $H_{fin} = 10$ nm, $W_{fin} = 2$ nm, $v_g = 1$ V. This is verified in Fig.5.13.

A larger I_d for larger W_{fin} indicates the enhancement of g_d for higher W_{fin}. This can be verified by Fig.5.14.

The comparison is done at $v_g = 1\,\text{V}$. The L and H_{fin} of the device are kept at 10 nm and the W_{fin} is kept at 4 nm. The g_d between two insulating gate materials is shown in Fig. 5.15. When the SiO_2 is replaced with HfO_2 material, the device with structural parameter $L = 10\,\text{nm}$, $H_{fin} = 10\,\text{nm}$ and $W_{fin} = 4\,\text{nm}$ provides a large enhancement of g_d with respect to SiO_2. The experiment is conducted on $v_g = 1\,\text{V}$.

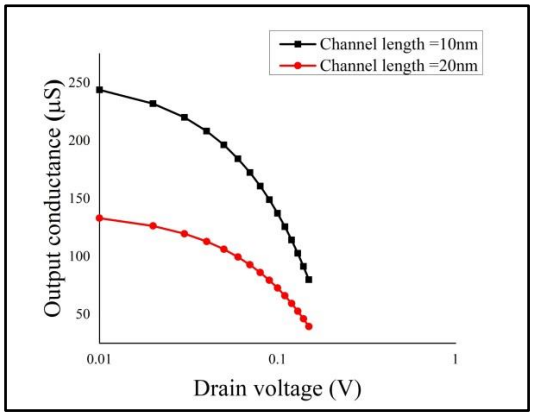


Fig.5.13: Output conductance with channel length for SiO_2

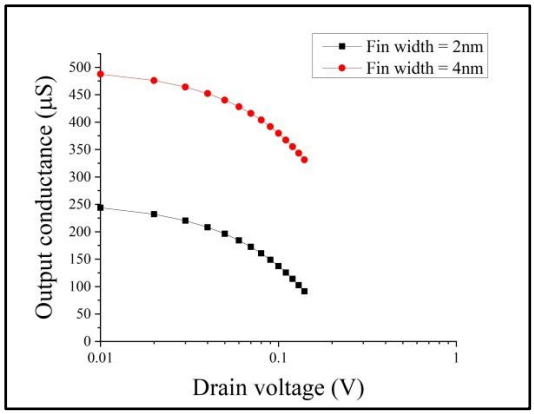


Fig.5.14: Output conductance with fin width for SiO_2

According to the physics of MOS, the SS decreases with the increment of the g_m/I_d (Kilchytska et al., 2003). This can be verified from Fig.5.16. It can be explained alternatively, as the gate control improves in smaller W_{fin}; therefore, the SCE, i.e., SS will also be improved for the same structure.

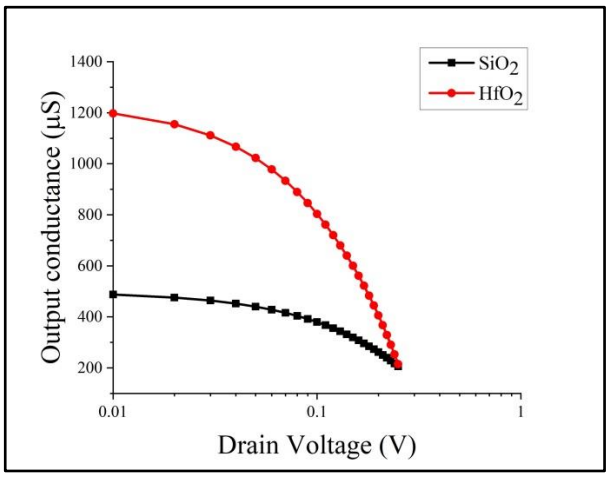


Fig.5.15: The comparison of output conductance for two dielectric materials.

The comparison of the *SS* for two dielectric gate materials is shown in Fig.5.17. When comparing the results, it can be seen that HfO_2 (67.1 mV/decade) has a lower value of *SS* than SiO_2 (84.6 mV/decade). Therefore, improvement of *SS* is obtained for the high-k dielectric.

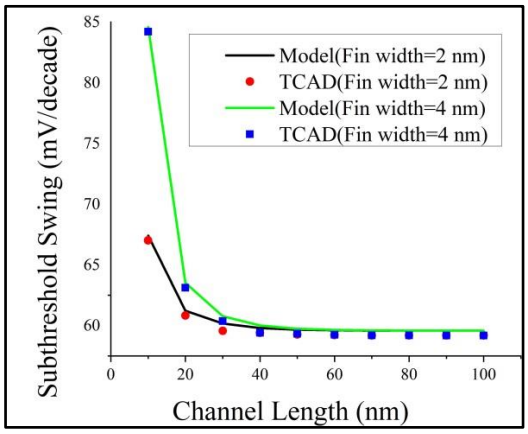


Fig.5.16: Subthreshold swing with channel length at different fin widths

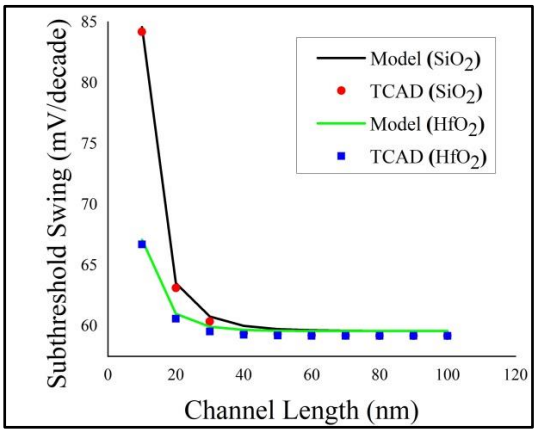


Fig.5.17: Comparison of subthreshold swing for two dielectric materials

A striking resemblance between the analytically derived model and the TCAD simulation has been found. Simulated results support this analytical model, and they are also fairly close to the reported fabricated result (Collaert, Demand, et al., 2005). The transfer characteristic is evaluated on an n-channel TG FinFET produced at IMEC on an SOI wafer (Leuven).The entire fabrication steps were explained in detail (Collaert, Demand, et al., 2005). Boron was doped in the Si channel at a concentration

of 10^{15} cm^{-3}. The doping concentrations in the source and drain were both $2x10^{20}$ cm^{-3}.

At (Tsormpatzoglou, Tassis, et al., 2009), an n-channel device with a TiN/HfO_2 gate insulator stack with $H_{fin} = 65$ nm, $W_{fin} = 875$ nm and L of 910 nm produced I_d in the order of 10^{-7}A. This was done at $v_d = 1.02$ V, $v_g = 0.5$ V. The comparable t_{ox} was determined to be 1.7 nm. These parameters have been used in the proposed model and got a I_d of about 200 nA. The mathematical model ignores the length of the extensions under the spacers between the gate, source, and drain pads and the presence of charges at the interface. So, these are the most likely causes of the analytical result differing from the experimental data.

5.4 Summary

The suggested short channel TG-FinFET has a low leakage current. By substituting HfO_2 for SiO_2, the current is significantly lowered. The fin volume changes with the H_{fin} and W_{fin}. Therefore, the direct effect of the fin's physical structure on the electron's accumulation cannot be neglected. So, the impact of H_{fin} and W_{fin} on I_d has been observed and clarified in detail. It can be concluded that the current saturates at a low value for smaller W_{fin} devices. But it attains a high I_d value for a larger H_{fin} device. The g_m characteristics support the trends of drain characteristics by varying fin physical parameters and electrical parameters. The V_T, including QME has been employed in the current model and the I_d is used to create the formulations of the small-signal parameters, namely g_m and g_d. Hence, the behaviour of all parameters is more accurately examined. At constant v_d, g_m attains a higher value for larger W_{fin} device which indicates more amplification for the wider W_{fin} device. The g_d also enhances for wider W_{fin} device. The consequence of short channels, such as, SS is also investigated. The subthreshold characteristics regarding L indicate that the smaller W_{fin} device can withstand SCE better than the larger W_{fin} device as the gate control improves in the smaller W_{fin} device. It has been clearly

shown that the electrical parameters are in accordance with the TCAD simulation. The model and the published fabricated device characteristics agree very well. Therefore, this model provides a compact performance of $L = 10$ nm TG-FinFET.

CHAPTER - 6

Trans-Capacitance

6.1 Introduction

Accurate device modeling is very important for circuit designers for circuit development. It has been playing the most vital role as semiconductor technology progresses every day and transistor channel capacitance modeling has been a continuous effort. The MOSFET forms a capacitive structure by embedding the thin oxide layer in between a metal or polysilicon gate and the semiconductor substrate. Though several other capacitances are associated with MOSFET, the C_{ox} per unit area is taking a significant role in the device performance. The unintentional capacitances which are generated due to the structure of the device are called parasitic capacitances. There are two types of parasitic capacitances, oxide-related capacitance and junction-related capacitance. The oxide-related capacitances arise owing to gate oxide structure. It forms between the gate and the other three terminals: the source, drain and body/substrate. The junction capacitance, commonly known as diffusion capacitance, forms between the substrate and source/drain.

Applying negative voltage at the gate terminal, n-channel MOSFET enters into the accumulation region and govern by the C_{ox}. Now, if a small positive voltage is applied to the gate terminal, holes are repealed and the depletion region starts to create under the oxide layer and the device is entering into the depletion mode. Hence, the

distance of the induced charge from the gate terminal increases. As a result, the capacitance starts to decrease. With the increment of the positive voltage depletion region width increases up to a finite value. Following the mass action law, hole density reduces, and electron density increases. The inversion layer is formed at V_T. When the v_g is above the V_T, it induces a greater number of electron and the capacitance value start to increase. In strong inversion, it will again equal C_{ox}.

But from the above discussion, it is clear that the modeling of capacitance is not so simple because of the presence of the parasitic, fringing capacitances which are formed because of the complex device architecture. However, if the contributing component for each geometrical parameter, process parameter, and the biassing condition is quantified, then these unwanted capacitances can be optimized exactly. As a result of this quantitative study, the performance can be fine-tuned to meet the needs. This study is critical and must be considered when modeling nano-scaled devices.

Meyer first gave an idea of the reciprocal gate-capacitive model (Meyer, 1971). The charge-based, non-reciprocal capacitance model was given by Ward (Donald Edward Ward, 1981). Several comparative studies of these two models have been reported. The Meyer model is causing some contradiction among experts. Some researchers (Chung, 1989; Sakallah, Yen, & Greenberg, 1990; Sheu, Hsu, & Ko, 1988; Snider, 1995) claim that it does not work properly owing to charge non-conservation. On the other hand, others state (Cirit, 1989; Sakallah, Yen, & Greenberg, 1987; P. Yang, Epler, & Chatterjee, 1983) that the charge non-conservation arises because of the inaccurate mathematical model of the simulation package. The non-conservation of charge or charge pumping means the stored charge in a node is not equal to the integrated net current flowing into the node. However, this kind of discontinuities in the capacitance functions creates instabilities in the Newton-Raphson iteration technique (Donald E Ward & Dutton, 1978).

Ward's model divides the channel charge artificially into the source and drain components. The discrepancies in Ward's model have been reported by Roy, A.S.,

Enz, C.C., & Sallese, J. M. (Roy, Enz, & Sallese, 2007) and Aarts, A. C et.al (Aarts et al., 2006).

The most widespread, Berkeley Short-Channel IGFET (BSIM) Capacitive Model, (Sheu et al., 1987) consists of above mentioned and other modeling techniques to evaluate the performance of Insulated Gate Field Effect Transistors (IGFET). However, due to charge redistribution in the channel, the BSIM capacitive model cannot incorporate first-order trans-capacitive currents. Hence, a discrepancy was generated between the device's actual outcome and simulation results (W. Liu & Chang, 1998). The first-order terms in the BSIM capacitive model are assumed to be energy storage terms (like capacitors and inductors) that do not dissipate energy, which is not happening in practical conditions. With all these limitations, the BSIM model is used because of its analogue-friendly and continuous quasi-static models and it also provides truthful I-V characteristics.

Hence, the models mentioned above have successfully modelled the MOS planar structure, which has served the industry for over 40 years. However, scaling difficulties such as amplified SCEs, DIBL and gate tunnelling current have resulted in a vertical fin-like 3-D structure. Due to its superior gate control for lowering SCE, the TG-FinFET has emerged as the most promising 3-D structure (Zhang et al., 2005). It is well known that the intrinsic gate capacitance to parasitic capacitance ratio determines gate latency. Therefore, to lessen gate delay, the ratio should be high. As a result, circuit simulation relies heavily on the modeling of trans-capacitance. However, the capacitance analytical model is limited to the ultra-scaled DG-FinFETs (Sharma et al., 2017). An analytical study of overlap and parasitic fringing capacitances for multi-fin DG-FinFET was reported by Wu, W., & Chan, M (W. Wu & Chan, 2007).

According to Ward–Dutton partitioning approach (S.-Y. Oh, Ward, & Dutton, 1980) trans-capacitances are evaluated by means of equivalent charge densities at source, drain, and gate nodes. Hence, the distribution of the mobile charges should be calculated from the current continuity equation. The charge is a complicated function of time. Customarily, the charge at any given time is governed by the terminal voltages at that particular time. Hence, steady-state circumstances can be used to calculate the

charge. Therefore, a simple mathematical model that accurately predicts the trans-capacitances of the undoped or weakly doped nanoscale TG-FinFET is required for exact circuit simulation.

This research constructed a charge-based compact capacitance model for undoped or weakly doped nanoscale TG-FinFETs with $L = 10\,\text{nm}$ and $t_{ox} = 1\,\text{nm}$. The structure provides a high drive current and faster response, as discussed in the previous chapters. Keeping the similarity with the previous chapters, a comparative study has also been done between SiO_2 and HfO_2. The Ward–Dutton linear-charge-partition method and the I_d continuity method are used to calculate the terminal charges analytically. The tans-capacitance is calculated using MATLAB simulation. TCAD simulation is used to confirm the results.

6.2 Analytical Model for Trans-Capacitance

The channel charge or gate charge $\left(Q_g\right)$ in the strong inversion region can be found out by integrating the inversion charge density $\left(Q_{inv}\right)$ over the L . Hence, Q_g will be,

$$Q_g = -W_{eff}\int_0^L Q_{inv}\left(y\right)dy \tag{6.1}$$

$W_{eff} = 2H_{fin} + W_{fin}$ is discussed in previous chapters. Now, from the current continuity equation,

$$dy = -\mu_0 W_{eff}\frac{4\varepsilon_{si}v_{th}}{H_{fin}}q_{ip}(y)\frac{dv_q}{I_d(y)} \tag{6.2}$$

According to (Tsormpatzoglou et al., 2010), q_{ip} is the normalized sheet charge density, which has been discussed in Chapter 5 in equation (5.11) can be written as

$$q_{ip} = \frac{1}{2A}LambertW\left(e^{\frac{v_g - V_T - v_q}{2v_{th}}}\frac{e^{\frac{v_g - V_T - v_q}{2\eta_{TG}v_{th}}}}{C + e^{\frac{v_g - V_T - v_q}{2\eta_{TG}v_{th}}}}\right) \tag{6.3}$$

where, $C = 4\dfrac{\exp\left(\dfrac{V_T + v_{fb}}{n}\right)}{\exp(n_1)}$, $n = 1\,\text{V}$ is a normalizing factor, n_1 is a constant, $A = \dfrac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} H_{fin}}$. The modified SS coefficient for the TG-FinFET is denoted by η_{TG} (N Fasarakis et al., 2011). Therefore, replacing equation (6.1) will be,

$$Q_g = \frac{\mu_0 W_{eff}{}^2 4\varepsilon_{si} v_{th}}{H_{fin} I_d} \int_{v_s}^{v_d} Q_{inv} q_{ip}(y) dv_q \tag{6.4}$$

As discussed in Chapter 5, v_q is the quasi-fermi potential which varies along the y direction and changes from v_s ($v_q = v_s = 0\,\text{V}$) to the v_d ($v_q = v_d$ V). From equation (5.18) $dv_q = -2\dfrac{KT}{q}\left(2A + \dfrac{1}{q_{ip}}\right) dq_{ip}$. Hence, equation (6.4) is again modified to,

$$Q_g = -2v_{th} \frac{\mu_0 W_{eff}^2}{I_d} \frac{4\varepsilon_{si} v_{th}}{H_{fin}} \int_{\frac{q_s}{2A}}^{\frac{q_d}{2A}} Q_{inv} q_{ip}(y) \left(2\,\text{A} + \frac{1}{q_{ip}}\right) dq_{ip} \tag{6.5}$$

Here, v_{th} is thermal voltage. Now, following (Tsormpatzoglou et al., 2010) the inversion charge density Q_{inv} is written as,

$$Q_{inv}(y) = \frac{4\varepsilon_{si} v_{th}}{H_{fin}} q_{ip}(y) \tag{6.6}$$

Therefore, replacing $Q_{inv}(y)$, equation (6.5) will be changed to,

$$Q_g = -2v_{th} \frac{\mu_0 W_{eff}^2}{I_d} \left(\frac{4\varepsilon_{si} v_{th}}{H_{fin}}\right)^2 \int_{\frac{q_s}{2A}}^{\frac{q_d}{2A}} q_{ip}{}^2(y) \left(2\,\text{A} + \frac{1}{q_{ip}}\right) dq_{ip} \tag{6.7}$$

Omit the negative sign by changing the limit the equation (6.7) becomes,

$$Q_g = 2v_{th} \frac{\mu_0 W_{eff}^2}{I_d} \left(\frac{4\varepsilon_{si} v_{th}}{H_{fin}}\right)^2 \int_{\frac{q_d}{2A}}^{\frac{q_s}{2A}} q_{ip}{}^2(y) \left(2\,\text{A} + \frac{1}{q_{ip}}\right) dq_{ip} \tag{6.8}$$

Now, integrating the above equation and putting the value of I_d from equation (5.21), the gate charge will be,

$$Q_g = \frac{v_{th}}{3} C_{ox} W_{eff} L \frac{3\left(q_s^2 - q_d^2\right) + 2\left(q_s^3 - q_d^3\right)}{\left(q_s - q_d\right) + 0.5\left(q_s^2 - q_d^2\right)} \tag{6.9}$$

Here, q_s the normalized sheet charge density in terms of LambertW function at the source end and similarly, q_d is the normalized sheet charge density in terms of LambertW function at drain end and these two terms have already been discussed in chapter 5 equation (5.15) and (5.16) respectively. By following the Ward-Dutton linear – charge partition method (Donald E Ward & Dutton, 1978), the drain charge i.e., the charge near the drain region, can be written as,

$$Q_d = W_{eff} \int_0^L \left(\frac{y}{L}\right) Q_{inv}(y)\, dy \tag{6.10}$$

To maintain the current continuity equation, we have considered that the current must be constant at any channel position. Considering the uniform μ and proportional petitioning scheme $\frac{y}{L}$ can be represented as,

$$\frac{y}{L} = \frac{\left(q_s - q_y\right) + 0.5\left(q_s^2 - q_y^2\right)}{\left(q_s - q_d\right) + 0.5\left(q_s^2 - q_d^2\right)} \tag{6.11}$$

Due to the presence of the local electric field, μ degrades near the drain. To maintain a constant μ along the channel, a new parameter ℓ is introduced and it also reflects the channel modulation. Hence, (6.11) will be modified to,

$$\frac{y}{L} = \ell \frac{\left(q_s - q_y\right) + 0.5\left(q_s^2 - q_y^2\right)}{\left(q_s - q_d\right) + 0.5\left(q_s^2 - q_d^2\right)} \tag{6.12}$$

For, the long channel ℓ is 1, but for short channel TG-FinFET, the empirical relation (Nikolaos Fasarakis et al., 2012) is given below:

$$\ell = 1 + \frac{3.5\lambda_{eff}}{L}\tanh\left(v_d / V_r\right) \tag{6.13}$$

Here, V_r regulates the transition from linear to saturation region. Now, using equation (6.2) and (6.12) in equation (6.10), the drain charge from (Nikolaos Fasarakis et al., 2012) will be,

$$Q_d = -\frac{v_{th}}{3} C_{ox} W_{eff} L\ell \frac{a_1 + a_2 + a_3}{\left(q_s - q_d\right) + 0.5\left(q_s^2 - q_d^2\right)} \tag{6.14}$$

where, $a_1 = \frac{2}{5}\left[\frac{\left(q_s - q_d\right)\left(2q_s^3 + 4q_s^2 q_d + 6q_d^2 q_s + 3q_d^3\right)}{2 + q_s + q_d}\right]$ (6.15a)

$$a_2 = \frac{1}{2}\left[\frac{\left(q_s - q_d\right)\left(5q_s^2 + 10q_s q_d + 9q_d^2\right)}{2 + q_s + q_d}\right] \tag{6.15b}$$

and $a_3 = \frac{2}{4}\left[\frac{\left(q_s - q_d\right)\left(q_s + 2q_d\right)}{2 + q_s + q_d}\right]$ (6.15c)

Similarly, the source charge can be calculated as,

$$Q_s = W_{eff}\int_0^L \left(1 - \frac{y}{L}\right) Q_{inv}\left(y\right) dy = -Q_g - Q_d \tag{6.16}$$

CLM plays a significant role in characterizing the SCEs of such a short-channel device. Therefore, at $v_d > \left(v_g - V_T\right)$ the L_{eff} can be represented as,

$$L_{eff} = L - \Delta L \tag{6.17}$$

ΔL is the channel reduction due to CLM, it has been given in equation (5.22). The λ_{eff} in terms of λ_{sym} and λ_{asym} has been given in equation (5.23). To eliminate the discontinuity at transition, i.e., from linear to saturation (Tsormpatzoglou et al., 2010), and V_{def} is considered and given in equation (5.25). Hence, by incorporating the concept of CLM, the improved gate charge and drain charge equations will be,

$$Q_g = \frac{v_{th}}{3} C_{ox} W_{eff} L_{eff} \frac{3\left(q_s^2 - q_d^2\right) + 2\left(q_s^3 - q_d^3\right)}{\left(q_s - q_d\right) + 0.5\left(q_s^2 - q_d^2\right)} \tag{6.18}$$

$$Q_d = -\frac{v_{th}}{3} C_{ox} W_{eff} L_{eff} \ell \frac{a_1 + a_2 + a_3}{\left(q_s - q_d\right) + 0.5\left(q_s^2 - q_d^2\right)} \tag{6.19}$$

The trans-capacitance can be derived by differentiating the charges with respect to the node voltages. Therefore, the trans-capacitances are defined as,

$$C_{jk} = \frac{\delta Q_j}{\delta v_k}|_{j=k} \text{ and } C_{jk} = -\frac{\delta Q_j}{\delta v_k}|_{j \neq k} \tag{6.20}$$

Here, j and k stand for source, gate and drain. MATLAB simulation is used to determine the trans-capacitance. The constant terms used in trans-capacitance are given below:

$$b_s = \exp\left(\frac{v_g - V_T}{2\eta_{TG} v_{th}}\right) \tag{6.21}$$

$$b_d = \exp\left(\frac{v_g - V_T - v_d}{2\eta_{TG} v_{th}}\right) \tag{6.22}$$

$$a_4 = \frac{\exp\left(\frac{-\left(v_d - v_g + V_T\right)}{2v_{th}}\right)\exp\left(b_d\right)}{C + b_d} \tag{6.23}$$

$$a_5 = \frac{\exp\left(\frac{-\left(v_s - v_g + V_T\right)}{2v_{th}}\right)\exp\left(b_s\right)}{C + b_s} \tag{6.24}$$

$$Lambertw\left(0, a_4\right) = LW\left(0, a_4\right) \tag{6.25}$$

$$Lambertw\left(0, a_5\right) = LW\left(0, a_5\right) \tag{6.26}$$

$$v_{th}\left(LW\left(0, a_4\right) + 1\right) = VLW\left(0, a_4\right) \tag{6.27}$$

$$v_{th}\left(LW\left(0, a_5\right) + 1\right) = VLW\left(0, a_5\right) \tag{6.28}$$

$$LW\left(0,a_4\right)LW\left(0,a_5\right)=L_1 \tag{6.29}$$

$$LW\left(0,a_4\right)-LW\left(0,a_5\right)=L_2 \tag{6.30}$$

$$\frac{LW\left(0,a_4\right)}{2VLW\left(0,a_4\right)}=L_3 \tag{6.31}$$

$$\frac{LW\left(0,a_5\right)}{2VLW\left(0,a_5\right)}=L_4 \tag{6.32}$$

$$LW\left(0,a_4\right)^3=L_5 \tag{6.33}$$

$$LW\left(0,a_5\right)^3=L_6 \tag{6.34}$$

$$LW\left(0,a_5\right)^2=L_7 \tag{6.35}$$

$$LW\left(0,a_4\right)^2=L_8 \tag{6.36}$$

$$LW\left(0,a_4\right)+LW\left(0,a_5\right)+2=LW\left(0,a_4,a_5\right) \tag{6.37}$$

Using the above constants, the trans-capacitances are expressed below:

$$C_{gs}=\frac{\left(C_{ox}L_{eff}v_{th}W_{eff}\left(\frac{3LW\left(0,a_5\right)^2}{2VLW\left(0,a_5\right)}+\frac{3LW\left(0,a_5\right)}{2VLW\left(0,a_5\right)}\right)\left(\begin{matrix}3LW(0,a_4)^2+2LW\left(0,a_4\right)^3\\-3LW(0,a_5)^2-2LW(0,a_5)^3\end{matrix}\right)\right)}{\left(\begin{matrix}\frac{3LW\left(0,a_4\right)^2}{2}+3LW\left(0,a_4\right)\\-\frac{3LW\left(0,a_4\right)^2}{2}-3LW\left(0,a_5\right)\end{matrix}\right)^2} \tag{6.38}$$

$$-\frac{\left(C_{ox}L_{eff}v_{th}W_{eff}\left(\frac{3LW\left(0,a_5\right)^2}{VLW\left(0,a_5\right)}+\frac{3LW\left(0,a_5\right)^3}{VLW\left(0,a_5\right)}\right)\right)}{\left(3LW\left(0,a_4\right)-3LW\left(0,a_4\right)+\frac{3LW\left(0,a_4\right)^2}{2}-\frac{3LW\left(0,a_4\right)^2}{2}\right)}$$

$$C_{gg} = \frac{\left(C_{ox} L_{eff} v_{th} W_{eff} \left(\frac{3LW(0,a_4)^2}{VLW(0,a_4)} + \frac{3LW(0,a_4)^3}{VLW(0,a_4)} - \frac{3LW(0,a_5)^2}{VLW(0,a_5)} - \frac{3LW(0,a_5)^3}{VLW(0,a_5)} \right) \right)}{\left(3LW(0,a_4) - 3LW(0,a_5) + \frac{3LW(0,a_4)^2}{2} - \frac{3LW(0,a_5)^2}{2} \right)}$$

$$- \frac{\left(C_{ox} L_{eff} v_{th} W_{eff} \left(\frac{3LW(0,a_4)^2}{2VLW(0,a_4)} - \frac{3LW(0,a_5)^2}{2VLW(0,a_5)} + \frac{3LW(0,a_4)}{2VLW(0,a_4)} - \frac{3LW(0,a_5)}{2VLW(0,a_5)} \right) \right)}{\left(3LW(0,a_4)^2 + 2LW(0,a_4)^3 - 3LW(0,a_5)^2 - 2LW(0,a_5)^3 \right)} \qquad (6.39)$$

$$\left(\frac{3LW(0,a_4)^2}{2} + 3LW(0,a_4) - \frac{3LW(0,a_5)^2}{2} + 3LW(0,a_5) \right)^2$$

$$C_{dg}=\frac{1}{\left(3\left(L_2+\frac{L_8}{2}-\frac{L_7}{2}\right)\right)}\left(\begin{array}{l}C_{ox}L_{eff}v_{th}W_{eff}\left(\frac{(L_3-L_4)(10L_1+9L_5+5L_7)}{2LW(0,a_4,a_5)}\right)\\+\frac{\left(L_1\left(\frac{27L_5}{2VLW(0,a_4)}+\frac{5L_7}{VLW(0,a_5)}+\frac{5L_1}{VLW(0,a_4)}+\frac{5L_1}{VLW(0,a_5)}\right)\right)}{2LW(0,a_4,a_5)}\\+\frac{\left(2(L_3-L_4)\left(4L_1^2+6L_8LW(0,a_5)+3L_5+2L_6\right)\right)}{5LW(0,a_4,a_5)}\\+\frac{\left(\frac{LW(0,a_4)}{VLW(0,a_4)}+L_4\right)L_2}{2LW(0,a_4,a_5)}+\frac{\left((L_3-L_4)(2LW(0,a_4)+LW(0,a_5))\right)}{2LW(0,a_4,a_5)}\\+\left(\frac{2L_2\left(\begin{array}{l}\frac{9L_5}{2VLW(0,a_4)}+\frac{3L_6}{VLW(0,a_5)}+\frac{2L_1^2}{VLW(0,a_4)}\\+\frac{6L_8LW(0,a_5)}{VLW(0,a_4)}+\frac{4L_1^2}{VLW(0,a_5)}+\frac{3L_8LW(0,a_5)}{VLW(0,a_5)}\end{array}\right)}{5LW(0,a_4,a_5)}\right)\\-\frac{(L_3+L_4)L_210L_1+9L_5+5L_7}{2LW(0,a_4,a_5)^2}\\-\frac{\left(2(L_3+L_4)L_2\left(\begin{array}{l}4L_1^2+6LW(0,a_4)^2LW(0,a_5)\\+3L_5+2L_6\end{array}\right)\right)}{5LW(0,a_4,a_5)^2}\\-\frac{\left((L_3+L_4)L_2(2LW(0,a_4)+LW(0,a_5))\right)}{2LW(0,a_4,a_5)^2}\end{array}\right)$$

$$-\frac{1}{3\left(\frac{L_8}{2}+\frac{L_2^2}{2}-L_7\right)}\left(\begin{array}{l}C_{ox}L_{eff}v_{th}W_{eff}\left(\begin{array}{l}\left(\frac{L_2(2LW(0,a_4)+LW(0,a_5))}{2LW(0,a_4,a_5)}\right)+\frac{L_2(10L_1+9L_5+5L_7)}{2LW(0,a_4,a_5)}\\+\frac{2L_2\left(4L_1^2+6L_8LW(0,a_5)+3L_5+2L_6\right)}{5LW(0,a_4,a_5)}\end{array}\right)\\\left(\frac{L_8}{2VLW(0,a_4)}-\frac{L_7}{2VLW(0,a_5)}+(L_3-L_4)\right)\end{array}\right)$$

(6.40)

$$C_{ds}=\frac{1}{\left(3\left(L_2+\frac{L_8}{2}-\frac{L_7}{2}\right)\right)}\left(C_{ox}L_{eff}v_{th}W_{eff}\left(\begin{array}{l}\left(\frac{LW(0,a_5)(10L_1+9L_5+5L_7)}{4LW(0,a_5)LW(0,a_4,a_5)}\right)\\ -\frac{\left(2L_2\left(\frac{3L_6}{VLW(0,a_5)}+\frac{4LW(0,a_4)L_7}{VLW(0,a_5)}+\frac{3L_8LW(0,a_5)}{VLW(0,a_5)}\right)\right)}{5LW(0,a_4,a_5)}\\ -\frac{L_2\left(\frac{5L_7}{VLW(0,a_5)}+\frac{5L_1}{VLW(0,a_5)}\right)}{2LW(0,a_4,a_5)}\\ +\frac{\left(LW(0,a_5)\left(4LW(0,a_4)L_7+6L_8LW(0,a_5)+3L_5+2L_6\right)\right)}{5VLW(0,a_5)LW(0,a_4,a_5)}\\ -\frac{LW(0,a_5)L_2}{4VLW(0,a_5)LW(0,a_4,a_5)}+\frac{LW(0,a_5)\left(2LW(0,a_4)+LW(0,a_5)\right)}{4VLW(0,a_5)LW(0,a_4,a_5)}\\ +\frac{LW(0,a_4)L_2(10L_1+9L_5+5L_7)}{4VLW(0,a_4)LW(0,a_4,a_5)^2}\\ +\frac{LW(0,a_4)L_2\left(4LW(0,a_4)L_7+6L_8LW(0,a_5)+3L_5+2L_6\right)}{5VLW(0,a_5)LW(0,a_4,a_5)^2}\\ +\frac{LW(0,a_5)L_2\left(2LW(0,a_4)+LW(0,a_5)\right)}{4VLW(0,a_4)LW(0,a_4,a_5)^2}\end{array}\right)\right)$$

$$-\frac{\left(C_{ox}L_{eff}v_{th}W_{eff}\left(\left(\frac{L_7}{2VLW(0,a_4)}+\frac{LW(0,a_4)}{2VLW(0,a_4)}\right)\left(\begin{array}{l}\frac{L_2\left(2LW(0,a_4)+LW(0,a_5)\right)}{2LW(0,a_4,a_5)}\\ +\frac{L_2(10L_1+9L_5+5L_7)}{2LW(0,a_4,a_5)}\\ +\frac{2L_2\left(4LW(0,a_4)L_7+6L_8LW(0,a_5)+3L_5+2L_6\right)}{5LW(0,a_4,a_5)}\end{array}\right)\right)\right)}{3\left(\frac{L_8}{2}+LW(0,a_4)-\frac{L_7}{2}-LW(0,a_5)\right)^2} \tag{6.41}$$

Now, according to charge conservation law the other capacitances are formulated below:

$$C_{ss}=C_{dg}+C_{gs} \tag{6.42}$$

$$C_{dd}=C_{ds}+C_{dg} \tag{6.43}$$

$$C_{gd}=C_{gg}-C_{gs} \tag{6.44}$$

$$C_{sg}=C_{gg}-C_{dg} \tag{6.45}$$

$$C_{sd} = C_{dd} + C_{gd} \tag{6.46}$$

With the miniaturization of the L , the interelectrode coupling between side and top gate electrodes are very sensitive (Børli, Vinkenes, & Fjeldly, 2008). According to Gauss' law total charge accumulated to an electrode can be calculated by integrating the vertical electric field terminating on that electrode. The interelectrode coupling charge can be calculated based on the above principle. The mobile charge's contribution is almost zero in the sub-threshold region; hence, this region is chosen for calculating the interelectrode coupling. Now, from the concept of planar MOS, the distribution of the v_g can be written as,

$$v_g = v_{fb} + \Phi_s + \Phi_{ox} \tag{6.47}$$

Keeping the similarity with the symmetric FinFET, the Φ along the channel in the presence of the electric field at the interface of the side gates $\left(\Phi_{side}\right)$ can be written as,

$$\Phi_{side} = \frac{1}{e^{2L/\lambda_{side}} - 1}\left\{\begin{array}{l}\left(v_{\mathrm{bi}} + v_d - v_g - v_{fb}\right)\left(e^{(L+y)/\lambda_{side}} - e^{(L-y)/\lambda_{side}}\right) \\ +\left(v_{bi} - v_g - v_{fb}\right)\left(e^{(2L-y)/\lambda_{side}} - e^{y/\lambda_{side}}\right) \\ +\left(v_g - v_{fb}\right)\left(e^{2L/\lambda_{side}} - 1\right)\end{array}\right\} \tag{6.48}$$

Therefore, using the Gauss' theorem, the charge related to side electrodes can be determined from equation (6.47) and it will be,

$$Q_{in\_side} = C_{ox} H_{fin} \int_0^L \left(v_g - v_{fb} - \Phi_{side}\right) dy \tag{6.49}$$

Replacing the Φ_{side} and integrating the equation (6.49), Q_{in_side} will be,

$$Q_{in\_side} = -C_{ox} H_{fin} \lambda_{side}\left[2v_{bi} + v_d - 2\left(v_g + v_{\mathrm{fb}}\right)\right] \frac{\exp\left(\frac{L}{\lambda_{side}}\right) - 1}{\exp\left(\frac{L}{\lambda_{side}}\right) + 1} \tag{6.50}$$

where, $\lambda_{side} = \sqrt{\frac{\varepsilon_{si} W_{fin}}{2C_{ox}}}$. The derivative of equation (6.50) with respect to v_g will produce the interelectrode capacitance for the side gates.

$$C_{g\_in\_side} = 2C_{ox} H_{fin} \lambda_{side} \left[\frac{\left(\exp\left(\frac{L}{\lambda_{side}} \right) - 1 \right)}{\left(\exp\left(\frac{L}{\lambda_{side}} \right) + 1 \right)} \right] \tag{6.51}$$

Using a similar technique, the interelectrode capacitance for the top gate will become,

$$C_{g\_in\_\mathrm{top}} = 2C_{ox} W_{fin} \lambda_{top} \left[\frac{\left(\exp\left(\frac{L}{\lambda_{top}} \right) - 1 \right)}{\left(\exp\left(\frac{L}{\lambda_{top}} \right) + 1 \right)} \right] \tag{6.52}$$

where, $\lambda_{top} = \sqrt{\frac{\varepsilon_{si} H_{fin}}{2C_{ox}}}$. Hence, the total interelectrode capacitance will be,

$$C_{g\_in} = C_{g\_in\_side} + C_{g\_in\_top} \tag{6.53}$$

Therefore, the total gate capacitance C_g will be the sum of C_{g_in} and C_{gg}.

$$C_g = C_{g\_in} + C_{gg} \tag{6.54}$$

Both the components of the interelectrode capacitance depend on the device structure, whereas C_{gg} also depend on the node voltage.

6.3 Results and Discussions

An undoped or lightly doped TG-FinFET is considered herein to investigate the trans-capacitance of the device. The list of the parameters used for this study is given below:

Table 6.1: ***Design Parameter Values for Trans-Capacitance***

SI.	Design Parameters	Value
01.	$N_A \rightarrow$ Uniform body doping concentration	10^{21} m^{-3}
02.	$N_D \rightarrow$ Source/ Drain doping concentration	10^{26} m^{-3}
03.	$t_{ox} \rightarrow$ Gate oxide thickness	1 nm
04.	$t_{oxb} \rightarrow$ Bottom oxide thickness	100 nm
05.	$W_{fin} \rightarrow$ Fin width	2-4 nm
06.	$H_{fin} \rightarrow$ Fin Height	10-20 nm
07	$L \rightarrow$ Channel length	10 nm
08.	$\varepsilon_{si} \rightarrow$ Permittivity of Silicon	11.7
09.	$\varepsilon_{ox} \rightarrow$ Permittivity of Oxide	3.9/22
10.	$x \rightarrow$ Coordinate of x-axis	0 nm
11.	$z \rightarrow$ Coordinate of z-axis	0 nm
12.	$\mu_0 \rightarrow$ Low electric field electron Mobility	200x10^{-4} m^2/V. s

The flat band voltage and the interface charges are accounted for as zero to disentangle the mathematical model. Before discussing the trans-capacitance, the source, drain and the gate charge as a function of v_g for SiO_2 are shown in Fig.6.1. In this study, the v_d is kept constant at $v_d = 0.1$ V. As the study is conducted on the n-channel device, it can be observed that source and drain both terminals are contributing negative charge. The analytical model is validated with TCAD simulation.

The effect of the high-k material as a replacement of SiO_2 with the same t_{ox} can be detected in Fig.6.2, indicating that all three charges are increased for high-k dielectric material.

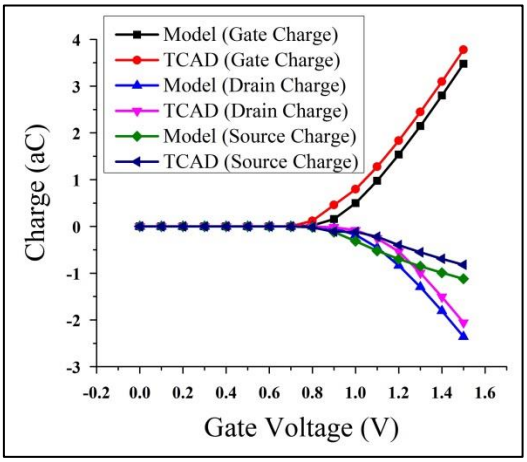


Fig.6.1: The gate, drain and source terminal charge with gate voltage for SiO_2

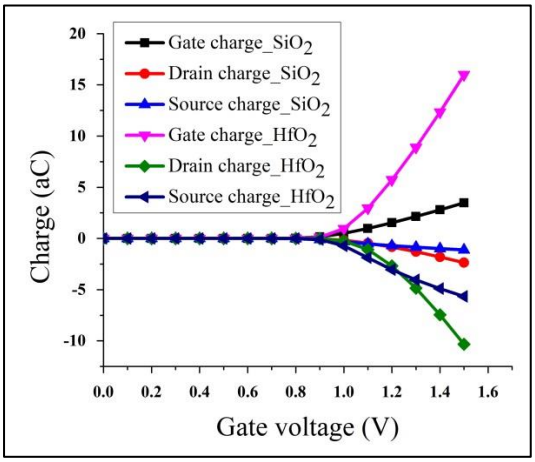


Fig.6.2: Comparison of the charges for SiO_2 and HfO_2

The variation of the three charges with the v_d for both the dielectric is depicted in Fig.6.3. It can be observed that the charges are almost constant with the increment of the v_d. The experiment is done for $v_g = 1$ V. The H_{fin}, W_{fin} and L are kept constant at 10 nm, 2 nm and 10 nm respectively, during the study of the charge variation with respect to v_g and v_d.

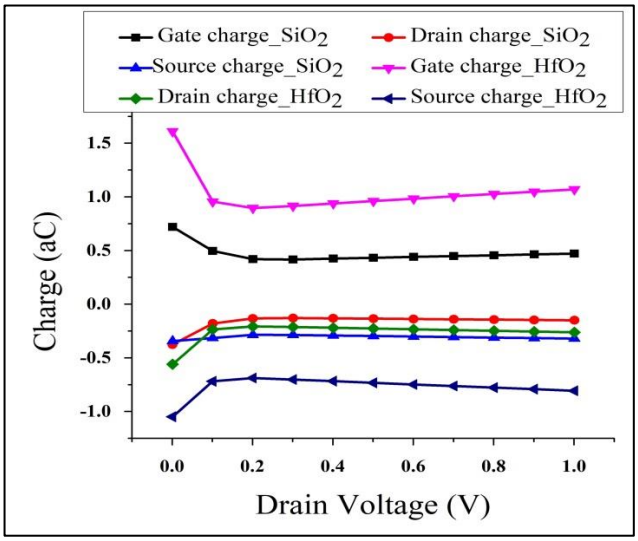


Fig.6.3: Variation of charges with v_d for both dielectrics

The trans-capacitance can be obtained by differentiating the charges with respect to node voltage. Fig.6.4, Fig.6.5 and Fig.6.6 show the source, gate and drain related trans-capacitance, respectively for SiO_2 and HfO_2. These figures illustrate the

trans-capacitances versus v_g at $v_d = 0.1\,\text{V}$. It can be examined that the trend of the trans-capacitance is similar for SiO_2 and HfO_2.

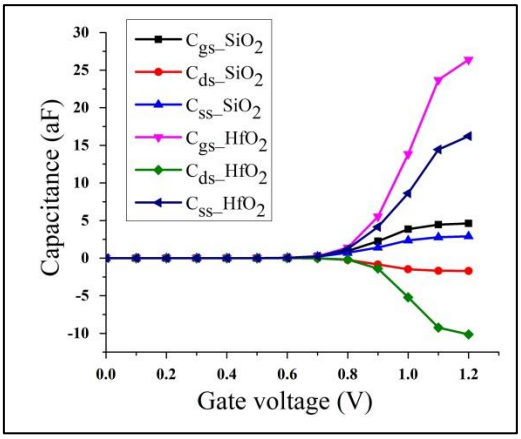


Fig.6.4: Source related trans-capacitance at for SiO_2 and HfO_2

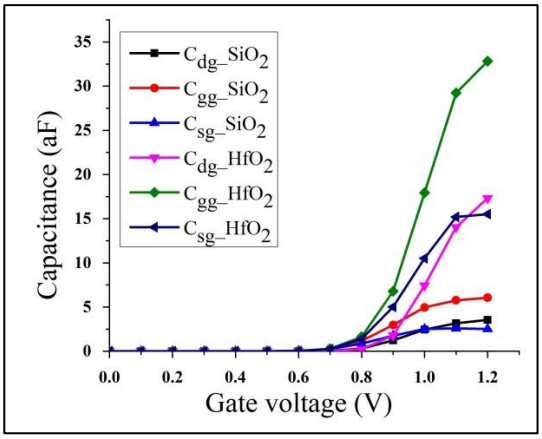


Fig.6.5: Gate related trans-capacitance at for SiO_2 and HfO_2

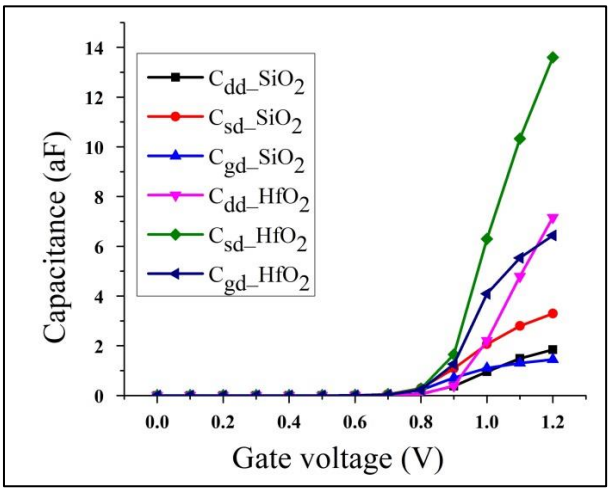


Fig.6.6: Drain related trans-capacitance with gate voltage for SiO_2 and HfO_2

The structure of the device is kept constant to find the different charges at the three nodes. The effect of higher v_d i.e., $v_d = 1\,\text{V}$ on the trans-capacitances is detected in Fig.6.7. The value of C_{gd} and C_{sd} are very close to each other, therefore, they cannot be distinguished in the plot.

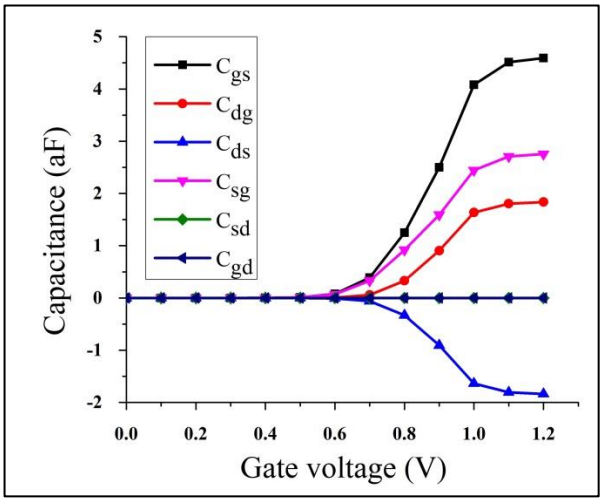


Fig.6.7: Trans-capacitance with gate voltage for SiO_2

The charge storing capacity at the drain terminal must be reduced with the increment of the v_d and, as a result, C_{dg} decreases. This phenomenon is supported by the pinch-off condition and is depicted in Fig.6.8.

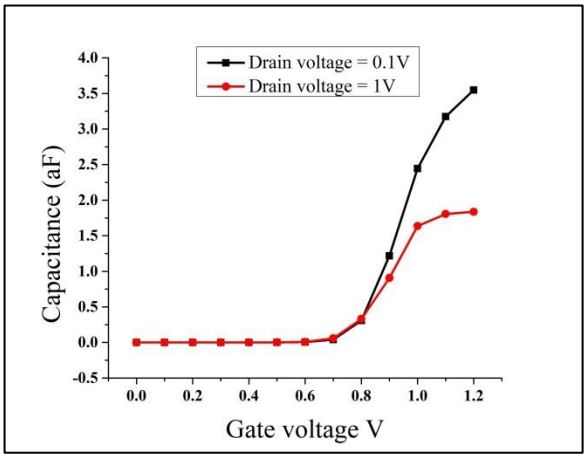


Fig.6.8: C_{dg} variation with gate voltage with v_d as a parameter for SiO_2

The Meyer model assumed that $C_{gd} = C_{dg}$, but practically $C_{gd} \neq C_{dg}$. C_{gd} indicates the impact of v_d at gate charge and opposite is valid for C_{dg}. Now at higher v_d ($v_d = 1\,\text{V}$), the drain is cut-off from the channel because of the pinch-off condition; therefore, the gate charge is unaffected by the v_d. So, the change of C_{gd} is negligible.

But a noticeable variation is observed for small v_d ($v_d = 0.1\text{V}$). However, the change of v_g will alter the channel charge and as a result, the effect of v_g on drain charge i.e., C_{dg} is visible for both drain voltages. This discussion can be verified in Fig.6.9.

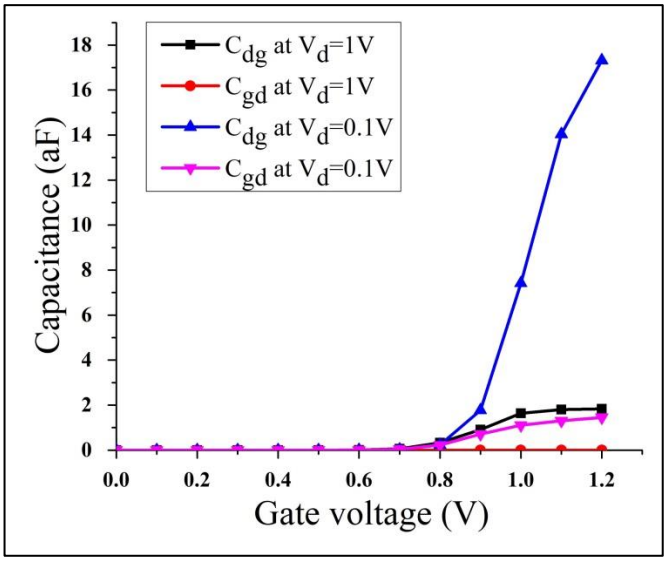


Fig.6.9: Change of C_{gd} & C_{dg} with gate voltage at different drain voltages for SiO_2

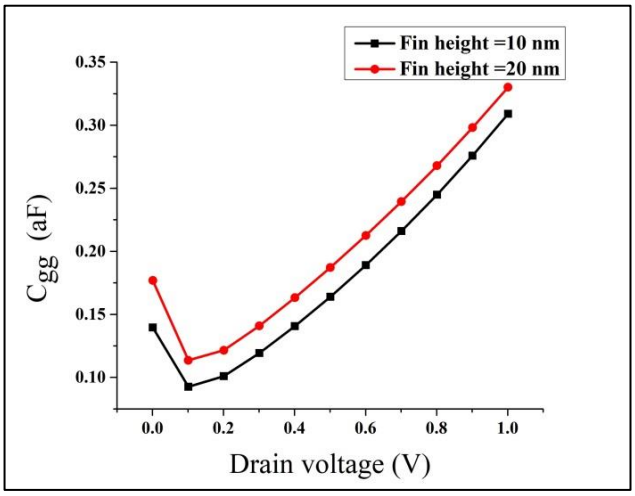
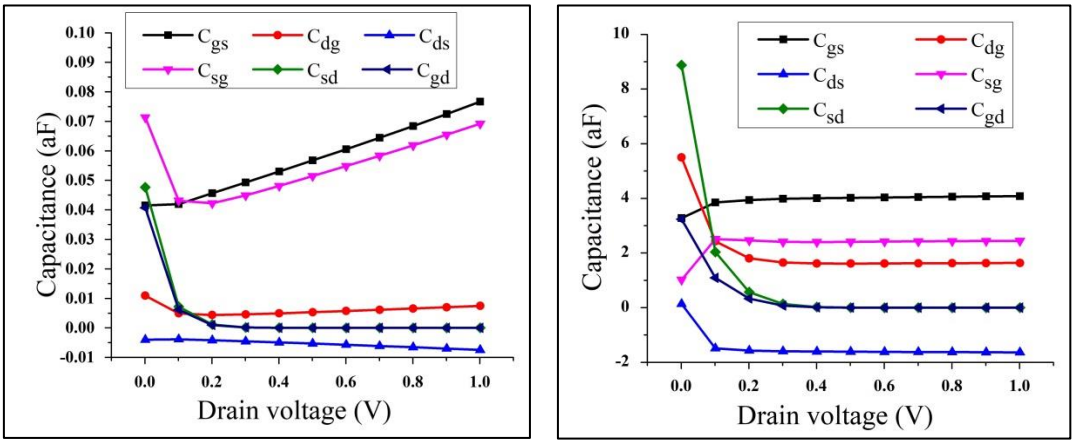


Fig.6.10: Trans-capacitance variation with v_d for SiO_2

Fig.6.10 shows the trans-capacitance versus v_d at $v_g = 0.6\,\text{V}$ with H_{fin} as parameter. The W_{fin} and L are kept constant at 4 nm and 10 nm, respectively. For better

understanding C_{gg} is only plotted against the v_d. It can be observed that the trans-capacitance increases with the increment of the H_{fin}.

The trans-capacitance with v_d for $v_g = 0.6$ V and $v_g = 0.1$ V is shown in Fig.6.11(a) and Fig.6.11(b) respectively. In this case the structural parameters are $H_{fin} = 10$ nm and $W_{fin} = 2$ nm.



(a) **(b)**

Fig.6.11: Trans-capacitance variation with v_d for SiO_2 when (a) $v_g = 0.6V$ (b) $v_g = 1.0V$

6.4 Summary

Analytical modeling is employed to study the trans-capacitance of the undoped or lightly doped TG-FinFET. The variation of charge at three different terminals with respect to v_g and v_d has been discussed. The increment of charges for high-k dielectric material is confirmed by comparing the HfO_2 and SiO_2. The trans-capacitance is calculated by differentiating the node charge with respect to other nodes. It can be verified that the Meyer model is not valid for the practical short channel device. The comparative study of trans-capacitance has also been demonstrated to indicate that the value of trans-capacitance increases with the increment of relative permittivity of the dielectric. The indirect application of the QME also enriched the mathematical model. An excellent agreement with TCAD simulation has proved that it can be useful for circuit designers. Quantum capacitance due to the spatial distribution of the electrons must be included in the mathematical model to get the

accurate gate capacitance for such a small device. This will be the future scope of this study.

CHAPTER - 7

Fin Shape Effect

7.1. Introduction

FinFET is a potential architecture which can be superior to the MOS transistors with gate lengths of 50 nm or less. It provides improved current drive and the more immune to SCEs than the conventional MOSFET (J-P Colinge, 2004; Cristoloveanu & Li, 1995). In addition to having improved performance, its manufacturing procedure is not considerably different from the standard SOI-CMOS technology (J-P Colinge, 2004). The design and analysis of rectangular (RE) FinFETs are generally reported by researchers, but they are hardly constructed in the industry. The limitation of the etching process results in non-vertical sidewall FinFET with angled lateral gates. Width variation can be mostly found along the vertical direction. If the vertical W_{fin} changes are not managed, they may result in subpar device performance or complete failure because of uninhibited SCE in particular fin locations. It also generates non-uniform current flow in the vertical direction. This phenomenon is originated from non-uniform series resistance along the height of the fin and the vertical electric field component that results from non-vertical gates. The most common fabricated cross sections are trapezoidal (TZ), concave and convex (Kedzierski et al., 2002; X. Wu et al., 2004). Even though some research has been done on purposefully non-rectangular shapes with fixed angles (Y. Liu et al., 2004), the top of the W_{fin} can be decreased up to a certain minimum value to achieve the triangular-shaped fin. Therefore, without changing technologies and other parameters, the RE-FinFET and TZ-FinFET can be

transformed into triangular (TI) FinFET. It is reported that 22 nm TI-FinFET can reduce approximately 70 % of leakage current compared to RE-FinFET (K. Wu et al., 2013). Xiu, K., & Oldiges, P. suggested that electron μ increases to some extent in inclined side walls, whereas the hole μ degrades (Xiu & Oldiges, 2012). Very few analytical models were developed for Non-rectangular FinFETs; the majority of literature presents the experimental or simulation results. The BSIM-CMG compact model for FinFETs is the first and only industry standard compact model, according to the Compact Model Council (CMC) (Paydavosi et al., 2013). The rectangular shape DG-FinFET solution serves as the foundation for the central model employed by BSIM-CMG. Yu, B et al. (Bo Yu et al., 2008) proposed a compact model for a non-rectangular shaped FinFET by combining the models implemented for DG-FinFET (Yuan Taur, 2000) and Cy-GAA FinFET (Y. Chen & Luo, 2001).

By finding an equivalent channel thickness for different fin-shaped structures, a compact model for undoped or weakly doped FinFETs was expanded by Chevillon, N et al. Additionally, a compact model based on a universal model framework was proposed for doped FinFET devices with various cross-sectional forms (Duarte et al., 2012; Duarte, Choi, et al., 2013). The symmetric non-vertical sidewalls with identical lateral side slopes are considered for compact modeling of TZ-FinFET (Nikolaos Fasarakis et al., 2013). This assumption is true for actual Intel-made products. But the asymmetric sidewalls ought to be a fascinating second-order effect.

A unified model was reported for TI-FinFET and TZ-FinFET. This model was based on the area of the channel, doping in the channel and insulator capacitance per unit length. Giacomini et al. examined the effect of fin shape on V_T while gate width and doping concentration varied widely (Giacomini & Martino, 2008). Buhler et al. inspected the dependence of the FinFET analogue characteristics on the trapezoidal Fin cross-section at various process node sizes (Bühler et al., 2009). Buhler et al. investigated the impact of irregular rectangle fins on the analogue performance of nanoscale devices (Bühler et al., 2009). Stanojevic et al. only gave a small number of intrinsic physical factors such as sub-band energy and μwhen they depicted the transition from a trapezoidal fin to a rectangular one (Stanojević et al., 2013) The effect

of fin shape on the gate leakage current was also studied by Gaynor et al (Gaynor & Hassoun, 2014).

The multiple gates of the FinFET provide better channel control and improve SCEs, but because of its 3-D architecture, it produces new coupling effects such as the corner effect. The top gate's involvement with the side gates was the primary cause of the corner effect. The V_T and current distribution in the cross-section of the fin is impacted by the inversion charge density that forms close to the device's corners. The corner effect is a function of the radius of the corners and dopant density (Bechelli & Giacomini, 2006). It was reported that the I-V characteristics of the device could be severely affected by the corner effect (Doyle et al., 2003; Jahanb & Cristoloveanu, 2006; Stadele et al., 2004). Comparatively, a lower V_T was created at the corner of the fin than the side wall gates. This low V_T lead to an increase in the I_{OFF}. Hence, the corner effect degrades device performance (J. Colinge, Park, & Xiong, 2003; Jahanb & Cristoloveanu, 2006). The inclination angle increases as we move from RE-TG FinFET to TI-TG FinFET. TI-TG FinFET has a lower corner effect than TZ-TG FinFET and RE-TG FinFET as the electric field and the inversion charge density reduce with the inclination angle increment.

This chapter deals with the three shapes of TG-FinFET. The V_T and I_d model are based on the previously explained model. Required changes are incorporated in the developed analytical models to include the shape effect. RE-TG FinFET, TZ-TG FinFET and TI-TG FinFET are compared with respect to different electrical parameters such as V_T, I_d, g_d and g_m. The short channel parameters, namely, DIBL, SS, ΔV_T and the I_{ON}/I_{OFF} ratio, have also been studied. The impact of the inclination angle and the corner effect on the I-V characteristics are examined. Keeping the similarities with previous chapters, the impact of the HfO_2 has also been inspected.

7.2. Analytical Model

The impact of the fin shape on the electrical and shot channel parameters is based on the previously described V_T model and I_d model. Those models are developed on RE-TG FinFET, where the top and bottom fin widths have the same

length and are indicated by $W_{rectangular\_fin} = W_{fin}$. But as the non-rectangular fin is considered for this study, the W_{eff} needs to be modified. For a non-rectangular fin, the top and bottom widths are not same. Thus, W_{fin_t} indicates the top width of the fin, while W_{fin_b} defining the bottom width of the fin. Therefore, the W_{fin} will be,

$$W_{fin} = W_{non\_rectangular} = W_{fin\_t} + \left(\frac{\xi}{1+\xi}\right)\left(W_{fin\_b} - W_{fin\_t}\right) \tag{7.1}$$

Here ξ is,

$$\xi = \frac{2W_{fin\_b} + W_{fin\_t}}{2W_{fin\_t} + W_{fin\_b}} \tag{7.2}$$

It is significant to note that for TI-TG FinFET, W_{fin_t} is zero. Whereas in rectangular fin both top and bottom fin widths are same and in that condition, $\xi = 1$. So, the generalized fin width is indicated by W_{eff}. Therefore, the W_{eff} can be represented as,

$$W_{eff} = W_{fin} + 2H_{fin} \tag{7.3}$$

The anatomy of the three different FinFET is depicted in Fig.7.1.

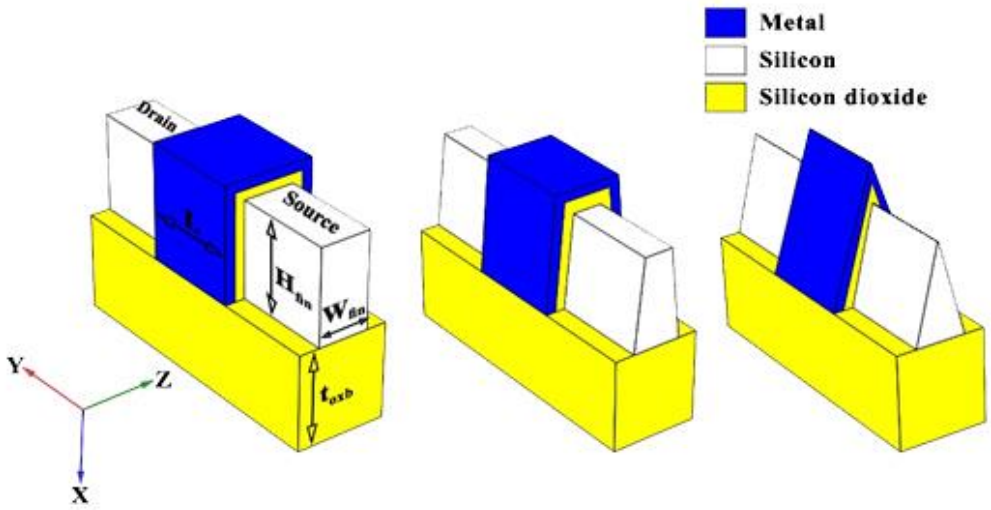


Fig.7.1: Anatomy of three TG-FinFET

The V_T equation (4.29) developed in Chapter 4 has been used to calculate the V_T for the TG-FinFET. In the case of a non-rectangular fin, the W_{fin} is replaced by $W_{non\_rectangular}$. Simple geometry is shown in Fig.7.2 can be used to establish the bottom width of the fin as a function of inclination angle (θ_i) and represent it as,

$$W_{fin\_b} = W_{fin\_t} + 2H_{fin} \tan\theta_i \tag{7.4}$$

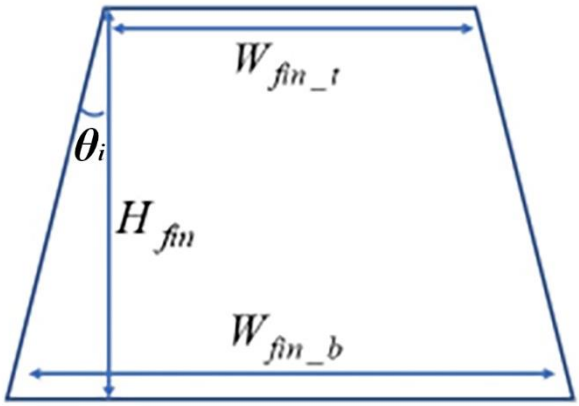


Fig.7.2: Cross-sectional view of trapezoidal FinFET

As a result, using the formula above, the bottom fin's width grows as θ_i increases. Incrementing the distance between the top and side gates with the increment of θ_i lessens the effectiveness of the corner effect. Fasarakis, N. et al. stated that the corner effect parameter f_{ce} does not dependent on the L and fin dimension (Nikolaos Fasarakis et al., 2013). It can be stated as,

$$f_{ce} = 1 - 0.0084 \cdot \theta_i \cdot \left(\frac{H_{fin}}{W_{fin\_b}} \right) \tag{7.5}$$

Using f_{ce} the precise I_d for rectangular as well as non-rectangular TG-FinFET will become,

$$I_{d\_\mathrm{mod}} = I_d f_{ce} \tag{7.6}$$

Here, the I_d is described in equation (5.30) in chapter 5. With a known value of H_{fin}, W_{fin_b}, W_{fin_t} equation (7.4) may be used to compute the value of θ_i for TG-

FinFET. 0°, 2.864° and 7.125° are the computed values of θ_i for RE-TG FinFET, TZ-TG FinFET and TI-TG FinFET respectively. H_{fin} is 20 nm for all TG-FinFET. The top and bottom fin widths are same for RE-TG FinFET and it is considered as 5 nm. For the TZ-TG FinFET W_{fin_b} is 5 nm and W_{fin_t} is 3 nm. As discussed above the W_{fin_t} is 0 nm for TI-TG FinFET and W_{fin_b} is 5 nm. Now using equation (7.5) f_{ce} will be 1, 0.9038, and 0.7606 for RE-TG FinFET, TZ-TG FinFET and TI-TG FinFET, respectively. The previous chapters have already modelled the other electrical parameters such as g_m, g_d, DIBL, ΔV_T, and SS.

7.3. Results and Discussions

The performances of RE-TG FinFET, TZ-TG FinFET and TI-TG FinFET are compared with respect to electrical and short channel parameters. The performance of the TI-TG FinFET has been mainly compared for two different dielectric materials, SiO_2 and HfO_2. The design parameters of this experiment is given in Table 7.1.

Table 7.1: Design Parameters Values for Fin Shaped Based Study

Sl.	Design Parameters	Value
01.	N_A → Uniform body doping concentration	10^{21} m^{-3}
02.	N_D → Source/ Drain doping concentration	10^{26} m^{-3}
03.	t_{ox} → Gate oxide thickness	1 nm
04.	t_{oxb} → Bottom oxide thickness	100 nm
05.	v_{fb} → Flat band voltage	0 V
06.	ε_{si} → Permittivity of Silicon	11.7
07.	ε_{ox} → Permittivity of Oxide (SiO_2/HfO_2)	3.9/22
08.	v_{sat} → saturation velocity	10^5 m/sec
09.	m_0 → Free electron mass	$9.1x10^{-31}$Kg
10.	m^* → Isotropic effective mass	$6.37x10^{-31}$Kg

11.	$H_{fin} \rightarrow$ Height of the fin	20 nm
12.	$W_{fin\_b} \rightarrow$ Fin bottom width	5 nm
13.	$W_{fin\_t} \rightarrow$ Fin top width	0 nm for TI-TG FinFET 3 nm for TZ-TG FinFET 5 nm for RE-TG FinFET

The consequence of fin shape on the V_T is portrayed in Fig.7.3. Fig.7.4 displays the influence of HfO_2 on the V_T . For the three different fin-shaped devices, the trends of variations in V_T for the two different oxides are the same. Using equation (7.1) W_{fin} of the RE-TG, TZ-TG and TI-TG has been calculated as 5 nm, 4.0833 nm and 3.333 nm respectively. The V_T rises when W_{fin} changes from higher to lower or from RE-TG to TI-TG. Lowest W_{fin} of TI-TG FinFET offers highest resistance as well as highest gate control, as a result it offers highest V_T . For HfO_2, this V_T increase is fairly noticeable. The difference in V_T between RE-TG FinFET and TI-TG FinFET at $L = 15$ nm, $v_d = 1$ V, $v_g = 0.4$ V, $H_{fin} = 20$ nm is roughly 18% for SiO_2 material and 9.3% for HfO_2.

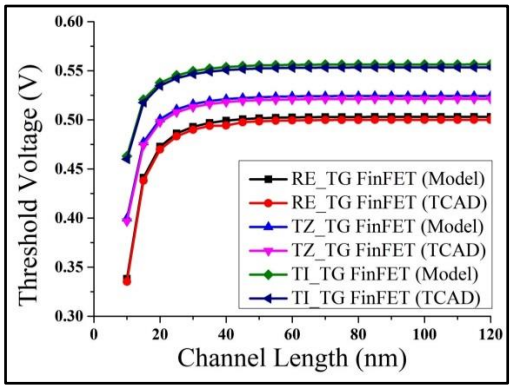


Fig.7.3: Change of threshold voltage with channel length for SiO_2

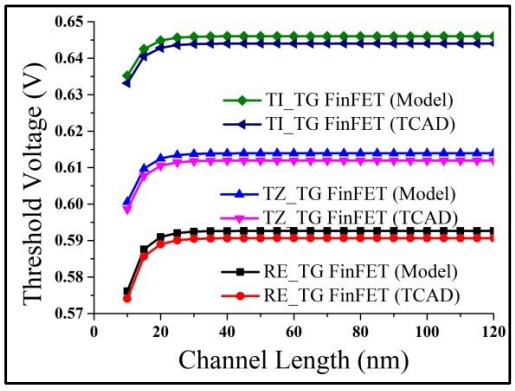


Fig.7.4: Change of threshold voltage with channel length for HfO_2

Fig.7.5 shows how the two different insulating materials affect the V_T for the TI-TG FinFET. Fig.7.5 shows that the HfO_2 material has a very low ΔV_T, indicating

better immunity against SCEs. The study is conducted on $v_d = 1\,\text{V}$, $v_g = 0.4\,\text{V}$, $H_{fin} = 20\,\text{nm}$

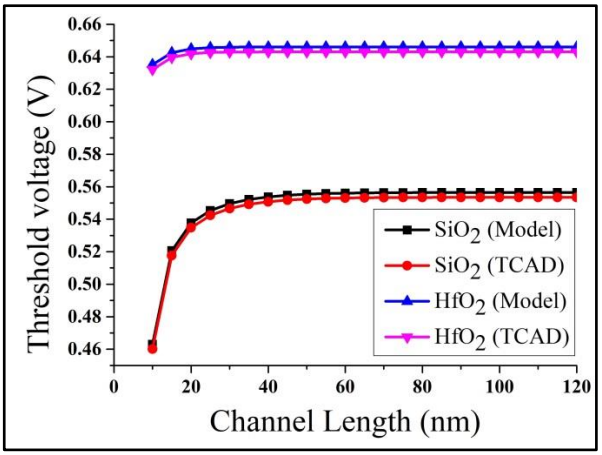


Fig.7.5: Comparison of threshold voltage of two dielectric materials for TI-TG FinFET

Non-uniform series resistance is produced at the source and drain by the non-rectangular cross-section of the fin (X. Wu et al., 2004). TI-TG FinFET offers the greatest source and drain resistance as the resistance is inversely proportional to the cross-sectional area of the fin. TI-TG FinFET should therefore provide the lowest I_d. Fig.7.6 shows the adjusted I_d with the corner effect. Fig.7.7 displays the I_d for a TI-TG FinFET with two distinct insulating materials. For these two studies the parameters are $v_g = 1\,\text{V}$, $L = 12\,\text{nm}$, $H_{fin} = 20\,\text{nm}$. In the instance of HfO_2, the I_d trends may become saturated at a greater value.

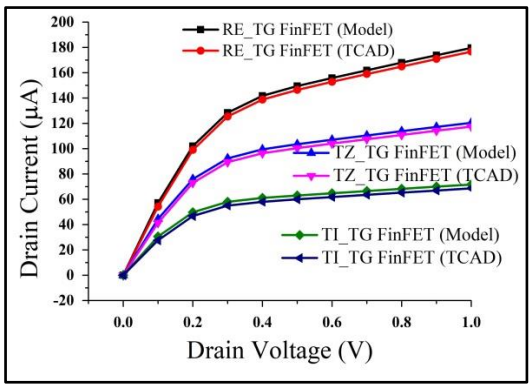


Fig.7.6: Drain characteristics for SiO_2

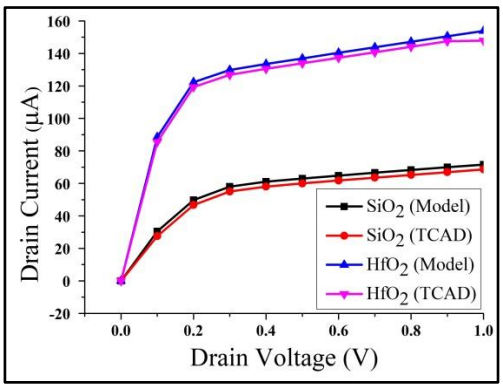


Fig.7.7: Comparison of drain characteristics of two dielectric materials for TI-TG FinFET

The I_d will rely on the inclination angle because this model indicates that the inclination angle influences the W_{eff}. As a result, Fig.7.8 shows how the I_d changes with an inclination angle. For this experiment the W_{fin_t} is kept at 3 nm and W_{fin_b} is calculated as function of inclination angle. Using the equation (7.1), $W_{non\_rectangular}$ is 9.504 nm for 15^0 inclination angle. In comparison, it is 4.964 nm for 5^0 inclination angle. As a result, it can be said that for a fixed top width, the overall width of the fin grows as the inclination angle increases, leading to a higher I_d for a larger inclination angle. Here, v_g is fixed at 1 V.

g_d is yet another crucial indicator of its quality. A precise measurement of the g_d is required for the accurate design of analogue ICs. While maintaining a constant gate-source voltage, the g_d qualifies the change of I_d with a drain-source voltage. Fig.7.9 displays the change of g_d with respect to v_d. RE-TG FinFET provides the greatest g_d. Fig.7.10 shows that when HfO_2 is used in place of SiO_2, the g_d rises. For Fig.7.9 and Fig.7.10 $v_g = 1$ V, $L = 12$ nm, $H_{fin} = 20$ nm.

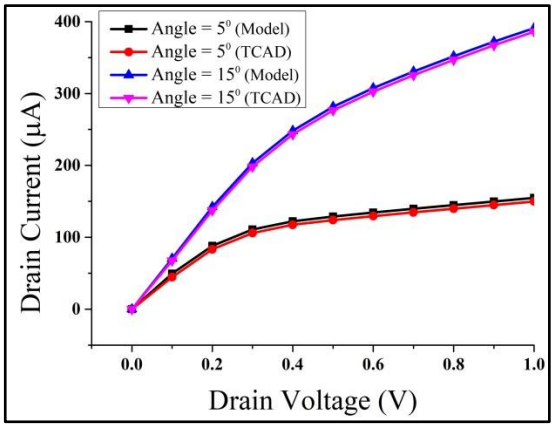


Fig.7.8: Drain current for SiO_2 as a function of inclination angle for TZ-TG FinFET

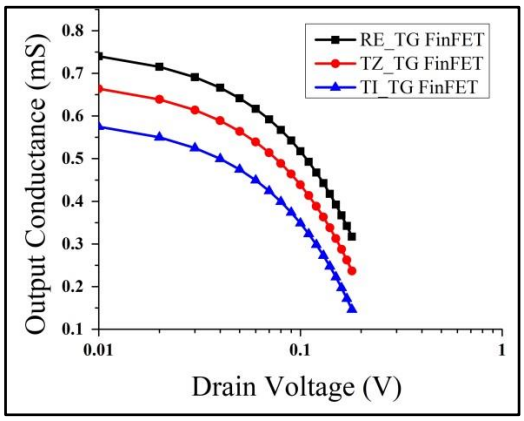


Fig.7.9: Change of output conductance with drain voltage for SiO_2

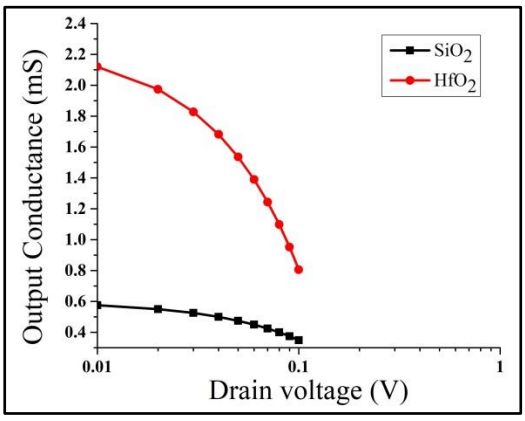


Fig.7.10: Comparison of output conductance of two dielectric materials for TI-TG FinFET

Fig.7.11 shows the transfer characteristics for SiO_2. HfO_2 can be used in place of SiO_2 to increase the on and off current ratio, which is supported by Fig.7.12 for TI-TG FinFET. From the plots, the off current and the on current are determined. The TI-TG FinFET can produce the least off current (8.87×10^{-17} A) compared to the other two-fin shaped devices since it has the smallest cross-sectional area and superior channel controllability. While RE-TG FinFET offers the widest fins, it also has the greatest I_{OFF} (1.47×10^{-14} A) and less gate control. Fig.7.13 describes the I_{ON}/I_{OFF} ratio for three distinct fin-shaped devices. I_{OFF} is measured at $v_g = 0$ V, while I_{ON} is measured at $v_g = 1.5$ V. For Fig.7.11, Fig.7.12 and Fig.7.13, $v_d = 1$ V, $L = 12$ nm, $H_{fin} = 20$ nm.

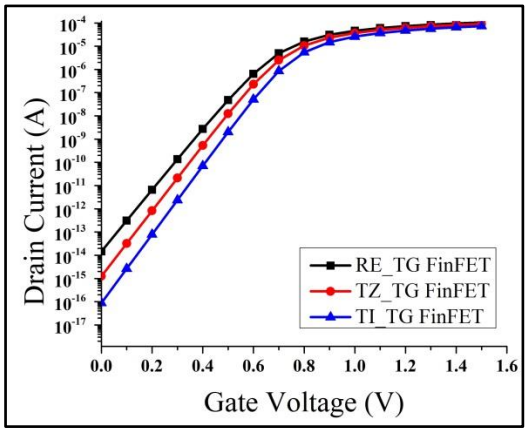


Fig.7.11: Transfer characteristics for SiO_2

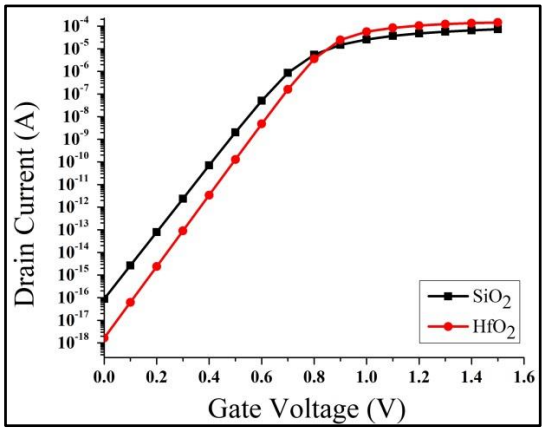


Fig.7.12: Comparison of transfer characteristics of two dielectric materials for TI-TG FinFET

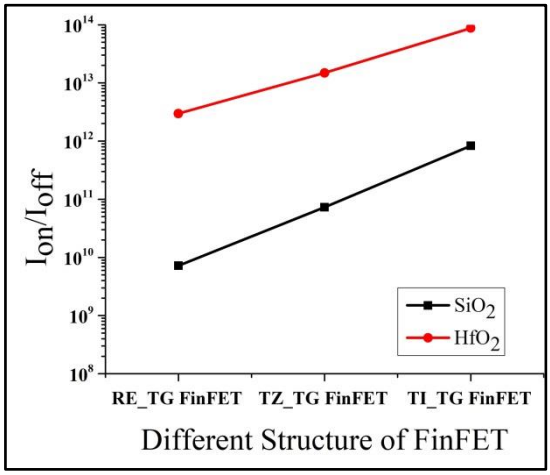


Fig.7.13: I_{ON}/I_{OFF} ***ratio for three fin shape structures.***

Basically g_m represents the device's gain. It shows the ratio of the change in gate-source bias voltage to the change in I_d for a fixed drain to source voltage. The channels' fields expand as the device size shrinks, and the levels of dopant impurities also rise (Dennard et al., 2007). Both modifications lower the μ and, consequently, the g_m. With a reduction in channel width, the source and drain resistance rises and the volume charge density falls. Since the g_m likewise decreases with a reduction in W_{eff}, the TI-TG FinFET is predicted to have the lowest g_m. The variation of g_m with respect to v_g is shown in Fig.7.14. HfO_2 has a greater g_m value, as shown in Fig.7.15. For these two studies $v_d = 0.1\,\text{V}$, $L = 12\,\text{nm}$, $H_{fin} = 20\ \text{nm}$.

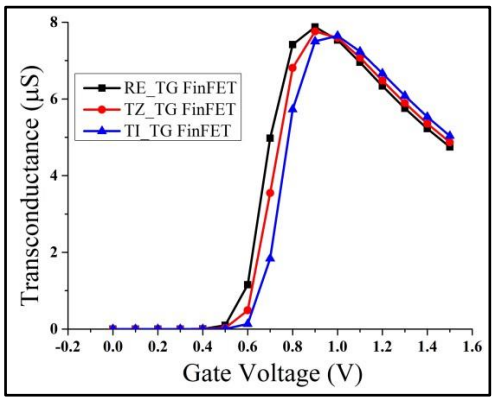


Fig.7.14: Change of transconductance with gate voltage for SiO_2

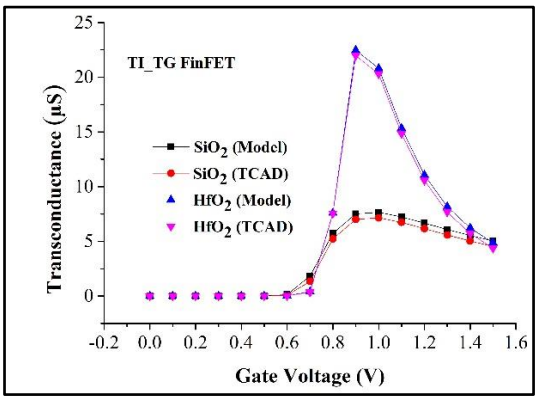


Fig.7.15: Comparison of transconductance of two dielectric materials for TI-TG FinFET

The SCE characteristics, which are crucial for such a small channel device, are also studied in this work after all the electrical parameters have been investigated. For SiO_2, DIBL is shown in Fig.7.16. The DIBL is plotted against L. The DIBL for TI-TG FinFET is lowest at $L = 10$ nm, and it is 0.05. Fig.7.17 demonstrates that DIBL can be enhanced by substituting HfO_2 for SiO_2. For Fig.7.16 and Fig.7.17 the parameters are $v_g = 0.4$ V, $L = 12$ nm, $H_{fin} = 20$ nm.

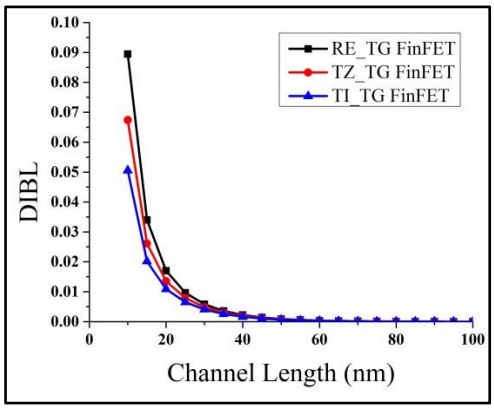


Fig.7.16: Change of DIBL with channel length for SiO_2

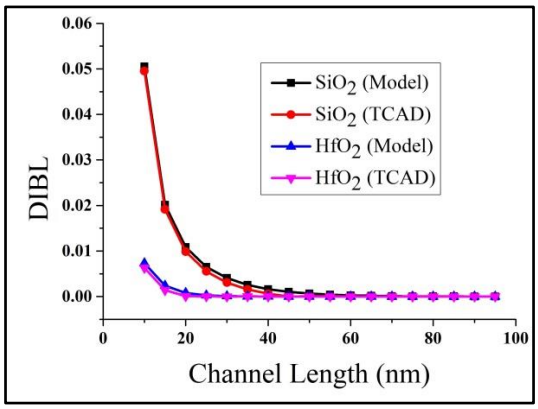


Fig.7.17: Comparison of DIBL of two dielectric materials for TI-TG FinFET

The SS for three distinct FinFETs are displayed in Fig.7.18. The TI-TG FinFET obtains the lowest, 72.7 mV/dec. For TI-TG FinFET, SS is improved by about 11% when using HfO_2 material. The two insulating materials for TI-TG FinFET are compared in Fig.7.19. For the study of SS, v_g and v_d are kept at 0.1V and 0.5 V respectively. Height of the fin is 20 nm.

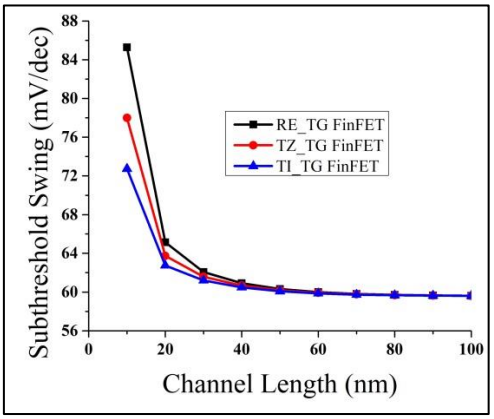


Fig.7.18: Change of subthreshold swing with channel length for SiO_2

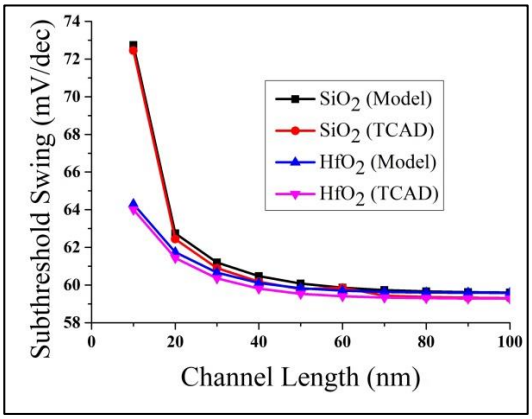


Fig.7.19: Comparison of sub threshold swing of two dielectric materials for TI-TG FinFET

In keeping with the other SCEs, the wide W_{fin} device, or RE-TG FinFET, has a more severe ΔV_T. Fig.7.20 shows how the L affects the ΔV_T of HfO_2. According to Fig.7.21, which compares the aforesaid parameter for TI-TG FinFET for the two dielectric materials, HfO_2 has a lesser g_m. This figure thus confirms that for such a short channel device, HfO_2 material has better electrical properties than SiO_2. For the study of ΔV_T, v_g and v_d are kept at 1.5 V and 0.5 V respectively. Height of the fin is 20 nm.

Therefore, from the above discussion it can be stated that the non-rectangular and somewhat smaller W_{fin} of the TZ-TG FinFET and TI-TG FinFET, has superior control over the channel, according to the SCE parameters. J.P. Colinge claimed that λ_{eff}, which denotes the penetration distance of the electric field lines from the drain to the channel of the device, can be used as a measure of SCE (J.-P. Colinge, 2008). The thickness of the silicon and gate oxide films affects this. In terms of λ_{sym} and λ_{asym} of DG-FinFET, it is given by,

$$\lambda_{eff} = \frac{2\lambda_{sym}\lambda_{asym}}{\sqrt{4\lambda_{asym}^2 + \lambda_{sym}^2}} \tag{7.7}$$

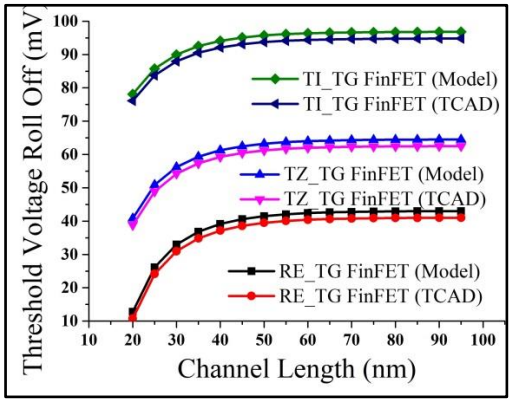


Fig.7.20: Change of ΔV_T with channel length for SiO_2

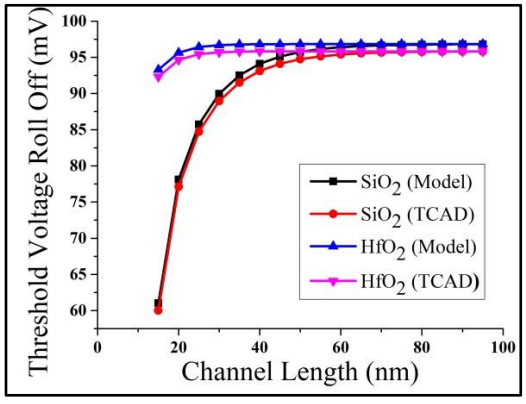


Fig.7.21: Comparison ΔV_T of two dielectric materials for TI-TG FinFET

Table 7.2 provides the value of the aforementioned parameter for three different shaped FinFETs. As a result, it can be shown that switching from RE-TG FinFET to TI-TG FinFET improves both the overall electrical properties and the SCEs.

Table 7.2: λ_{eff} for Three Different Shaped FinFET

Fin Shape	Value of λ_{eff}
RE_TG FinFET	2.2003 nm
TZ_TG FinFET	1.9480 nm
TI_TG FinFET	1.7292 nm

An analogy has been drawn between the proposed model and n-channel RE-TG FinFET that was created at IMEC (Leuven) on an SOI wafer. In (Collaert, Demand, et al., 2005), the fabrication process was detailed. Boron was used for the Si channel's background doping (10^{15} cm^{-3}). The concentration of doping at the source and drain was $2x10^{20}$ cm^{-3}. The RE-TG FinFET produced on current in the order of 10^{-4}A at $H_{fin} = 65\,\text{nm}$, $L = 910$ nm, and $W_{fin} = 875\,\text{nm}$, providing an excellent agreement with the model's predictions (Tsormpatzoglou, Tassis, et al., 2009).

7.4 Summary

The performance of three distinct cross-sectioned TG-FinFETs have been examined by simulating the V_T and I_d. CLM, μ_{eff}, and V_{def} have included this short-channel device's analytical model. For RE-TG FinFET, TZ-TG FinFET, and TI-TG FinFET, the electrical properties of V_T, I_d, g_d, and g_m are examined. Additionally, SCEs including SS, DIBL, and ΔV_T are explored. Comparing these factors reveals that the TI-TG FinFET achieves the lowest corner impact thanks to its highest inclination angle. As a result, TI-TG FinFET achieves the maximum current gain and lowest SCEs. Thus, it can be said that the TI-TG FinFET uses less energy than the other two cross-sectioned FinFET under consideration. For HfO_2, a similar but superior trend is seen. This suggests that using TI-TG FinFET will improve performance in an electronic circuit. The TCAD simulation compares all the

parameters and shows excellent agreement. The I_d of the RE-TG FinFET is fairly close to the experimental result that has been reported. As a result, our analytical model can accurately describe the I_d of three different TG-FinFET cross-sections.

CHAPTER - 8

Conclusion and Future Scope

8.1. Conclusion

The current dissertation entitled "Modeling, simulation and performance analysis of FinFET" focuses on the analytical modeling of TG-FinFET. An extensive effort has been given to developing the mathematical model for Φ, V_T, I_d and trans-capacitance. The present thesis contains eight chapters. The 1st chapter deals with an introduction through which the adverse effects of aggressive scaling can be understood. The various SCEs which are important to determine the device performance are illustrated. A substantial endeavour has been given to realize the necessity of transforming the planar structure to a vertical one. The implementation of the high-k material, specifically the advantages of the HfO_2 material, has been discussed. Hence, chapter 1 projects FinFET as a potential candidate for future VLSI technology. The indication that emerges from chapter 1 is the application of HfO_2 material in place of SiO_2.

With the extensive literature review of the FinFET, the study arrives at the modeling of the Φ, the fundamental parameter of the device. Without implementing very complex mathematical processes such as the Greens function, Poisson's equation has been solved using the parabolic potential function and Gauss's boundary conditions. The parabolic variation of the Φ offers its minima in the centre of the channel. The plot of Φ with the L shows that as the L reduces, the minimum value of Φ rises. This suggests that reduction of channel to source barrier height results

lower V_T which is supported by the short channel device physics. A lower amount of Φ has been observed for the high-k, which predicts the controlled V_T for the short channel device.

The V_T model has proved the prediction of the Φ model. It can be observed that V_T decreases with the decrement of the L. From the experimental results, it can be concluded that the V_T is a function of W_{fin} and H_{fin}. QME confinement is an integral part of $L = 10$ nm device and the V_T must be higher than the predicted value by classical mechanics. This QM approach has been successfully included in the analytical model, and the theoretical prophecy has been supported by TCAD simulation. Additionally, the slight fluctuation of DIBL and SS with L/W_{fin} for HfO_2 has been noted. These investigations revealed that HfO_2 offers a great degree of immunity in terms of SCEs. The V_T model has been verified with well-established TCAD simulation and published fabrication results.

The I_d of the TG-FinFET has been modelled by means of the LambertW function. The output characteristics satisfy the established theory. From the characteristics curves, it can be concluded that inversion charge density increases with the fin's volume, resulting in a higher saturation current. The g_m curve with respect to v_g suggested that wider W_{fin} provides larger amplification. The ratio g_m/I_d is very useful for analogue applications and it is almost constant up to V_T. The analytical model predicts that g_d is inversely proportional to the L and it has been confirmed by TCAD simulation. The lower value of the I_{OFF} is obtained for high-k material, which again indicates that HfO_2 will be a potential substitute for SiO_2 in short channel device technology. The published experimental results also verify the I_d model.

A trans-capacitance model has also been established. The charges at the gate, drain and source terminal have been calculated mathematically. The polarity of the charges supports the underlined physics of the n-FinFET device. The development of

the trans-capacitance model is noteworthy from this perspective since the modeling of the device capacitance is crucial for circuit simulation. The trans-capacitances are modelled using MATLAB software and verified by the TCAD simulator. It is clear from comparing the trans-capacitance of SiO_2 and HfO_2 that the capacitance value rises for high-k materials.

With the help of these aforesaid models, a comparative study has been done for RE-TG FinFET, TZ-FinFET and TI-TG FinFET. From the study, it can be concluded that a higher drive current is achieved for RE-TG FinFET. While the TI-TG FinFET offers a maximum current gain and lowest SCEs. Theory suggests that the corner effect reduces with the inclination angle. This theoretical estimation has been verified by the analytical model as well as TCAD simulation. A comparative bar graph for $L = 10$ nm device is given in Fig.8.1 for better understanding.

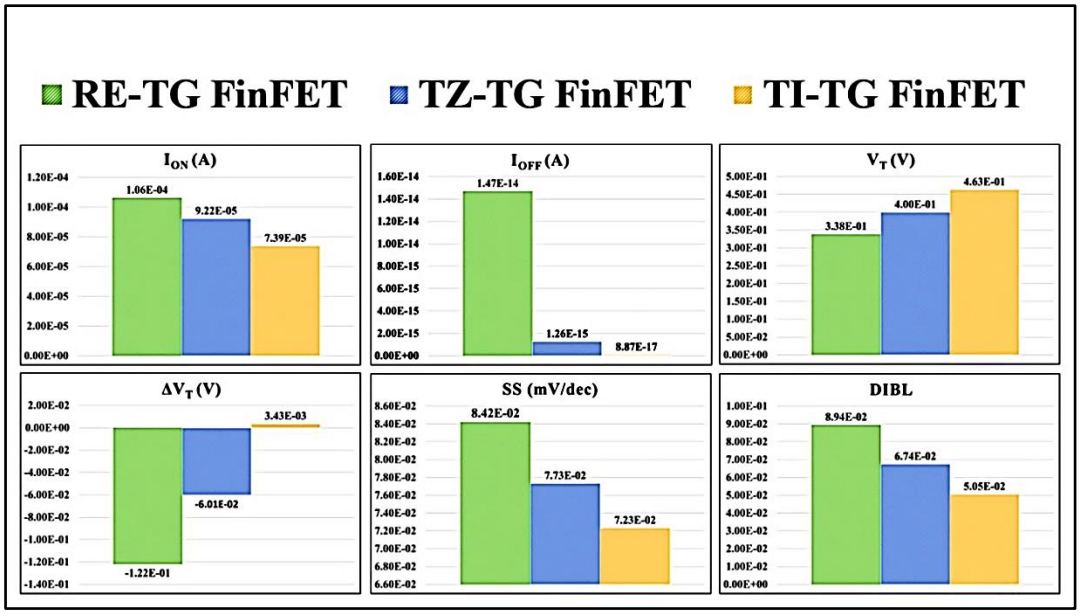


Fig.8.1: A comparative study of different parameters for RE-TG FinFET, TZ-TG FinFET & TI-TG FinFET

The overall comparison of the electrical and SCE parameters for SiO_2 and HfO_2 for RE-TG FinFET is depicted in Fig.8.2 and Fig.8.3.

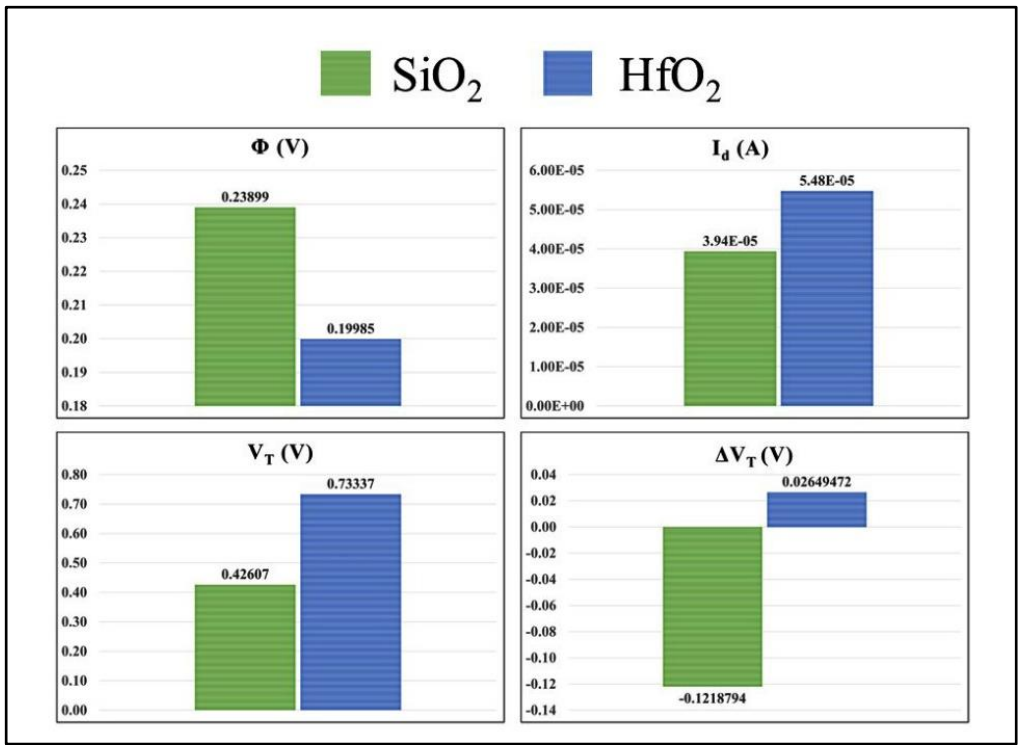


Fig.8.2: Comparison of different parameters of RE-TG FinFET for both dielectric materials

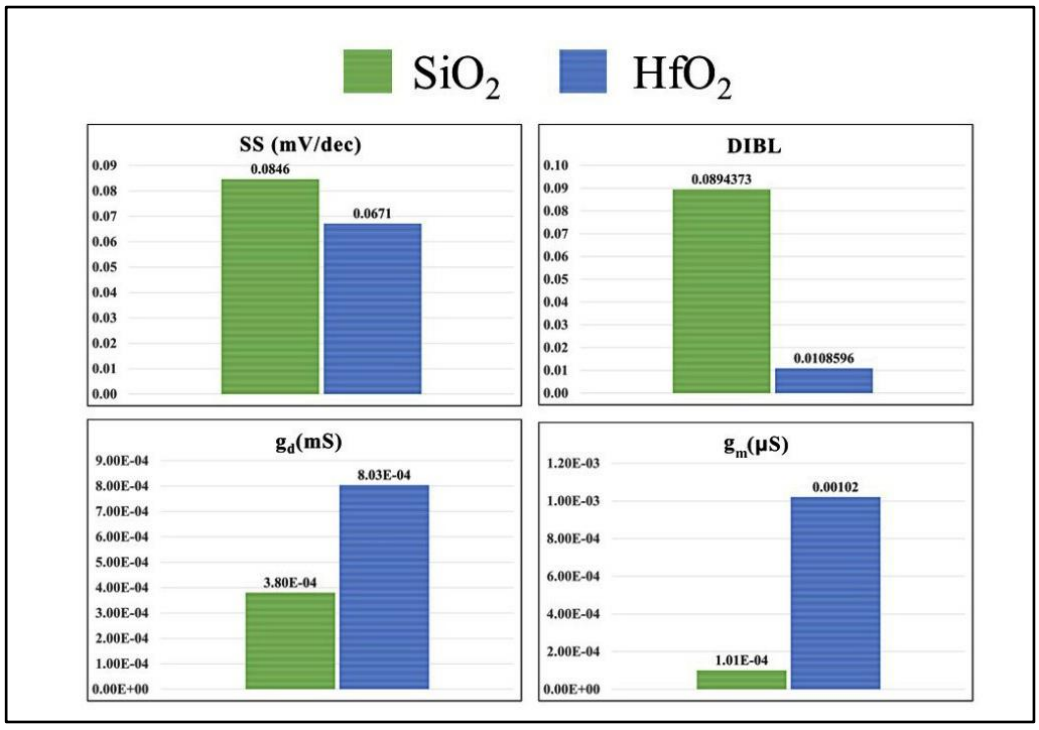


Fig.8.3: Comparison of rest of the parameters of RE-TG FinFET for both dielectric materials.

8.2. Future Scope

In nanoscale FinFETs, numerous modeling challenges need to be investigated. Exploiting a multidimensional Poisson-Schrodinger solution that views electrons as waves moving through the device is highly desirable. It is essential to model and characterize DT, GIDL, and FIBL. It was reported that FBIL increases with the application of high-k material. Therefore, modeling of FBIL is very much crucial for characterizing the device performance.

The device's performance can be better understood with the help of accurate modeling of parasitic capacitance and resistance. The gate capacitance determines the speed of operation of the device. The quantum capacitance is a consequence of the spatial distribution of the electrons in the short channel device. Therefore, there is significant scope for including quantum capacitance in the proposed mathematical model to obtain accurate gate capacitance.

Nearly all IC users place a high value on reliability. Statistical analysis such as bias temperature instability (BTI) and hot carrier deterioration may be required for precise circuit failure rate modeling. This work will be benefited from characterizing the device parameters in relation to temperature variation. The ideal oxide interface is considered for this current research work. Therefore, to make it a more practical interface, non-idealities will be added in future.

Ge and GaAs are currently possible contenders that can be employed as the channel. Hence, the same models can be investigated with Ge semiconductors. Therefore, a huge scope of inquiry is still left. In light of this, the study of this specific structure establishes its distinctiveness in every way.

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List of publications

Journal Publications

1. S. Panchanan, R. Maity, S. Baishya, N. P. Maity, "Modeling, Simulation and Performance Analysis of Drain Current for below 10 nm Channel Length Based Tri-Gate FinFET," *Silicon (Springer)*, pp. 1-12, 2022. DOI: 10.1007/s12633-022-01875-5.
2. S. Panchanan, R. Maity, S. Baishya and N. P. Maity, "A surface potential model for tri-gate metal oxide semiconductor field effect transistor: Analysis below 10 nm channel length," *Engineering Science and Technology, an International Journal (Elsevier)*, vol. 24, pp. 879–889, 2021. DOI: 10.1016/j.jestch.2020.12.020.
3. S. Panchanan, R. Maity, S. Baishya and N. P. Maity, "Modeling, Simulation and Analysis of Surface Potential and Threshold Voltage: Application to High-K Material HfO_2 Based FinFET," *Silicon (Springer)*, vol. 13, no. 10, pp. 3271-3289, 2021. DOI: 10.1007/s12633-020-00607-x
4. S. Panchanan, R. Maity, A. Baidya, and N. P. Maity, "Role of Fin Shape on Drain Current of SiO_2/HfO_2 Based Trigate FinFET Including Quantum Mechanical Effect," *Silicon (Springer), 2023. DOI: 10.1007/s12633-023-02288-8*
5. S. Panchanan, R. Maity, A. Baidya, and N. P. Maity, "Impact of Fin Width on Nano Scale Tri-Gate FinFET Including the Quantum Mechanical Effect," *Engineering Research Express, IOP Science*, Manuscript ID: ERX-102378R1 (Under Review).
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1. S. Panchanan, R. Maity and N. P. Maity, "A Novel Surface Potential for Tri-Gate Metal Oxide Semiconductor Field Effect Transistor," *2nd International Conference on Energy Systems, Drives and Automations, Kolkata*, 2019.
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ABSTRACT

MODELING, SIMULATION AND PERFORMANCE ANALYSIS OF FINFET

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SCHOOL OF ENGINEERING AND TECHNOLOGY

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MODELING SIMULATION AND PERFORMANCE ANALYSIS OF FINFET

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Submitted

In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Electronics and Communication Engineering of Mizoram University, Aizawl

Introduction

The development of integrated circuit (IC) technology in this electronic era dictates the development of almost all other technologies. The main factor influencing the evaluation of IC technology is improved performance in terms of size, cost and energy usage. Device scaling, which has been successfully used since the 1990s in response to the growing demand for high packing density, low power consumption, and excellent performance, is therefore advised. The benefits of the planer silicon (Si) metal oxide semiconductor field effect transistor (MOSFET) marque it the norm in the electronics industry. But over the past 20 years, Silicon-On-Insulator (SOI) has been the most booming research area because of its reduction ability of parasitic capacitance and series resistance. IBM utilised it for the first time in 2000. Physical parameters like channel lengths, widths, depths, etc. must be reduced to create a high-performance small-scale device. The energy barrier of these short-channel devices is affected by the drain voltage. All subthreshold parameters are impacted by short channel effects (SCEs), which also cause the threshold voltage (V_T) to decrease. Leakage current increases due to a decrease in V_T and a decline in subthreshold slope. Poor $\left(I_{ON}/I_{OFF}\right)$ is consequently seen in short-channel devices. As a result, the scalability of the parameters of each device is constrained by the SCEs.

Silicon dioxide (SiO_2) has been employed as gate oxide over the last few decades because it can be readily produced from Si with very few electrical flaws, creating an excellent interface. Nanometre-scale etching and patterning are also possible. However, insulator thicknesses less than 1.5 nm will result in large tunnelling gate currents, which raise power dissipation and produce extra heat, both of which harm the device. Scaling down SiO_2 thickness is thus constrained by the tunnelling current. Hence, IC technology adopts high-k gate dielectric mterial, which reduces leakage current and improves gate capacitance as an alternative to SiO_2.

Therefore, miniaturisation will not meet the criteria of modern high packing density, low power consumption, and high-speed IC technology. This stimulates the

development of new multi-gate structures. The multi-gate field effect transistors (MGFET) with more than one gate can improve the drain potential screening from the channel and improve the SCEs. In this regard, FinFET-based MGFET device is a potential technological alternative to the current technology. The vertical channel in FinFETs is called a fin. The merit of FinFET is being able to operate on the same principles as CMOS. Due to the low doping concentration in the channel, it is possible to extend the gate scaling beyond the limits of planar transistors, maintain a steep subthreshold slope, and perform better with bias voltage scaling. Due to their straightforward designs and simplicity in manufacture, triple-gate (TG) and double-gate (DG) FinFETs, common MGFETs have emerged as the most appealing alternatives to MOSFETs. In TG-FinFET, the third gate is added on top of the channel through an additional selective etching step of the hard mask. Although the third gate increases the complexity of the process, it also has certain benefits, such as decreased fringe capacitances and increased transistor width. The channel width of FinFET is a function of fin height $\left(H_{fin}\right)$ and this is known as width quantisation. Thus, the gate control can be improved by adding more fins to a structure. Though small fin heights lead to flexible structures when compared to lengthy fin structures, which is a measurable metric to define the stability of the structure.

To study the TG-FinFET behaviour, it has been imagined as a combination of two DG-FinFET. The symmetric DG-FinFET in the $\left(y,z\right)$ direction. Whereas the asymmetric FinFET in the $\left(x,y\right)$ direction. This research work is founded on the ideal condition, i.e., the metal-semiconductor work function is zero and the interface charge density is also zero. The analytical model is not only compared with the well-accepted TCD simulation but also with published experimental results. The outstanding agreement with simulation and fabrication results proves the potentiality of this research work.

Objectives

To keep up with the current IC technological trend, device size should be in the nm order. But the miniaturisation is restricted by SCEs. Therefore, structural

change is the most acceptable alternative to the current technology. Therefore, the gate control over the channel is improved by utilising MGFET technology to increase the concert in low-power VLSI logic circuits and decrease SCEs. FinFET is a potential candidate among the MGFET structures. Before using a device in an analogue or digital application, it must first be precisely characterised. Hence, mathematical modelling of the device comes into the picture. A properly constructed analytical model can forecast the outcomes that closely match the actual measurements made on the practical device. This method offers a thorough understanding of the device's underlying physics, and simultaneously being less expensive and less time-consuming. Therefore, the requirement of mathematical modelling is the stimulus of this research work.

To study the device's behaviour, the surface potential (Φ), electric field (E), V_T, drain current (I_d) and trans-capacitance are modelled. The SCEs, the small frequency parameters such as drain/output conductance (g_d) and transconductance (g_m) are also formulated from the analytical model. A comparative study has been done between SiO_2 and hafnium dioxide (HfO_2). The electrical characteristics are derived by varying the structural parameters such as H_{fin}, fin width (W_{fin}), channel length (L) and gate oxide thickness (t_{ox}). The effect of drain voltage (v_d), gate voltage (v_g), acceptor concentration (N_A) and donor concentration (N_D) on the device performance are rigorously examined for both gate oxide materials. The model incorporates the quantum mechanical effect (QME) to characterize the device more exactly. At a glance-

- The 2D Poisson's equation for the DG-FinFET must be solved separately with the aid of boundary conditions in order to produce the analytical model of Φ. The Φ of TG-FinFET has been calculated by combining Φ of the DG-FinFET using the perimeter weighted sum approach. The E has also been calculated from the modeled Φ equation.

- Evaluate V_T using the inversion charge method. Here also, the V_T is modeled separately for two DG-FinFETs and then combined them using the perimeter weighted sum approach to find out the V_T of the TG-FinFET. The SCEs, namely threshold voltage roll-off (ΔV_T), drain induced barrier lowering (DIBL) and subthreshold swing (SS) are discussed.
- The I_d model discusses the drain and the transfer characteristics. The I_{ON}/I_{OFF} ratio will be calculated from the transfer characteristics. The g_m and g_d are directly obtained by differentiating the I_d equation.
- The trans-capacitance is calculated at each node of the device.
- The effect of the shape of the FinFET on the device characteristics is explored.
- The model examines the effect of HfO_2 as a gate oxide material on the same structure.
- The models are validated using TCAD simulation and the results are also compared with the published experimental results.

Summary

The electrical properties of the TG-FinFET structure has been studied based on Φ, E, V_T and I_d. The SCEs has been examined in terms of ΔV_T, DIBL, transconductance generation factor (TGF) and SS. The response of the device characteristics is compared for SiO_2 and HfO_2.

Chapter 1 discusses IC technology's development, starting from bipolar junction transistor (BJT) to FinFET. There is also a quick explanation of the various SCEs. The application of high-k materials is also conferred. The justifications for selecting HfO_2 as the gate oxide material is also mentioned.

Chapter 2 provides an extensive review of FinFET. The different structures of the FinFET and their attributes are explored. This chapter briefly overviews many

short channel FinFET models and their results. It also reports the widespread usage of high-k materials, particularly the most favourable high-k which is compatible with MOSFETs.

Chapter 3 covers the Φ model. The Φ of the TG-FinFET is formulated by combining the Φ of the DG devices which are calculated separately. For this, the perimeter-weighted sum approach is employed. The simulation results are used to validate every analytical result. A comparative study of Φ between SiO_2 and HfO_2 produces lower Φ for high-k material. This indicates that oxide thickness can be raised for high-k material to maintain an equivalent Φ. It will resolve the current tunnelling issue in a certain degree. Φ can be increased for a fixed oxide thickness by adjusting N_A, N_D, v_g, v_d. The minima of the parabolic Φ increases with the reduction of the L. Φ can also be modified with the modification of structural parameters such as H_{fin}, W_{fin}. The results indicate that SCEs can be better handled by a high-k dielectric material.

Chapter 4 offers the V_T modelling of TG-FinFET. The V_T is computed individually for symmetric and asymmetric DG-FinFETs using the inversion charge method. They are combined with the help of perimeter-weighted sum method to find V_T of the TG-FinFET. The increment of V_T due to the quantum mechanical confinement is explained by including the quantum mechanical correction in the model. The study also investigates the SCEs, namely ΔV_T and DIBL. The effect of high-k material on V_T is also analysed.

Chapter 5 formulates the I_d with the help of the LambertW function. An accurate model is created by including channel length modulation, effective drain voltage, and effective mobility. The g_m and g_d are the small frequency parameters covered in this chapter. The impact of SiO_2 and HfO_2 are also examined.

Chapter 6 models the trans-capacitance of the TG-FinFET. The charges are calculated at the three terminals and plotted against v_g and v_d. The trans-

capacitances are formulated using the MATLAB. It can be seen that SiO_2 and HfO_2 have a similar trans-capacitance pattern.

Chapter 7 discusses the influence of the fin shape on the device characteristics. This chapter compares the performance of the rectangular, trapezoidal, and triangular TG-FinFET in terms of V_T, I_d, g_m and g_d. The SCEs viz., ΔV_T, SS and DIBL are also contrasted for the three forms. The device parameters of the triangular-shaped FinFET are examined in light of a comparative study of SiO_2 and HfO_2. It can be stated that among all shapes, triangular-shaped FinFET with HfO_2 as a gate dielectric material provides better immunity against the SCEs.

Chapter 8 draws an overall conclusion of research works. This chapter also considers the model's limitations and future prospects.