INVESTIGATION OF ADIABATIC AND QUASI-ADIABATIC LOGIC TECHNIQUES FOR DIGITAL CMOS CIRCUITS

A THESIS SUBMITTED IN PARTIAL FULLFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILLOSHOPHY

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Ph.D. REGN NO: MZU/Ph.D./1293 of 03.08.2018

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SCHOOL OF ENGINEERING AND TECHNOLOGY

JULY 2025

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In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in

Electronics & Communication Engineering of Mizoram University, Aizawl

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CERTIFICATE

This is to certify that the thesis entitled " **Investigation of Adiabatic and Quasi-Adiabatic Logic Techniques for Digital CMOS Circuits**" submitted to Mizoram University for the award of the degree of Doctor of Philosophy in Electronics and Communication Engineering **Reginald H. Vanlalchaka**, Ph.D. Registration No. **MZU/Ph.D./1293 of 03.08.2018**, is Ph.D. scholar in the Department of Electronics and Communication, under my guidance and supervision and has not been previously submitted for the award of any degree in any Indian or foreign University. He has fulfilled all criteria prescribed by the UGC (Minimum Standard and Procedure governing Ph.D. Regulations). He has fulfilled the mandatory publication (Publication enclosed) and completed Ph.D. course work. It is also certified that the scholar has been admitted in the Department through an entrance test, followed by an interview as per UGC Regulation of 2016.

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DECLARATION

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I **Reginald H. Vanlalchaka**, hereby declare that the subject matter of this thesis is the record of work done by me, that the contents of this thesis did not form basis of the award of any previous degree to me or to do the best of my knowledge to anybody else, and that the thesis has not been submitted by me for any research degree in any other University/Institute.

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Acknowledgement

First and foremost, I am deeply thankful to the **Almighty God** for bestowing upon me wisdom, health, and apportionment throughout the course of this research. His blessings have guided and sustained me. I express my profound gratitude to my supervisor, **Prof. Niladri Pratap Maity**, for his expert guidance and directions. His support and insights have been crucial in the development of this thesis. I sincerely thank **Prof. Reshmi Maity**, Head of the ECE Department, for granting me access to the department's laboratory and resources. Her cooperation has been instrumental in the advancement of my research. I am immensely grateful to my parents for their moral support, encouragement, and prayers. Their unwavering belief in me has been my greatest source of strength and motivation. Special thanks are due to my dear sister, **Dr. Vanlalruatkimi**, for her assistance in thesis writing and editing. Her contributions have been invaluable to refining this thesis. I extend my deepest appreciation to my wife, **J. Vanlalhriatpuii**, for her constant encouragement and understanding. Her support has been a cornerstone of my perseverance. I also wish to acknowledge my eldest brother, **Dr. Vanlalhmuliana**, for his inspiration and financial support. His contributions have been vital to my academic journey. I am deeply thankful to my family for their unwavering support, which has been a source of immense comfort and motivation. I would like to express my gratitude to **Dr. Lalthanpuii Khiangte** for her assistance with the software I acquired, which has played a significant role in my research.

Lastly, I extend my thanks to the teaching and non-teaching staff of the ECE Department, MZU, for their assistance and cooperation. Your dedication has greatly contributed to the completion of this thesis. I also appreciate any other individuals who have provided direct or indirect assistance throughout this journey.

(REGINALD H. VANLALCHAKA)

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Abbreviation

A

ADCL	Adiabatic Dynamic CMOS Logic
ADCVSL	Adiabatic Differential Cascode Voltage Switch Logic
ADL	Adiabatic Dynamic Logic
ALA	Adiabatic Logic Array
ALU	Arithmetic Logic Unit
APDL	Adiabatic pseudo-domino logic

C

CAL	Clocked CMOS Adiabatic Logic
CCAL	Clocked CMOS Adiabatic Logic
CDCAL	Clocked Differential Cascode Adiabatic Logic
CEPAL	Complementary Energy path Adiabatic Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CPAL	Complementary Pass-Transistor Adiabatic Logic
CPU	Central Processing Unit
CTGAL	Clocked Transmission Gate Adiabatic Logic

D

DCPAL	Differential Cascode Pre-resolve Adiabatic Logic
DFAL	Diode-Free Adiabatic Logic Circuit
DTGAL	Dual Transmission Gate Adiabatic Logic

E

ECRL	Efficient Charge Recovery Logic
EEL	Energy Efficient Logic
EFAL	Energy-Efficient Adiabatic Logic
EPFAL	Enhanced Positive Feedback Adiabatic Logic

G

GFCAL	Glitch-Free and Cascadable Adiabatic Logic

H

HEERL	High-Efficient Energy Recovery Logic

I

IAPDL	Improved Adiabatic Pseudo-Domino Logic
IAPDL-2	Improved Adiabatic Pseudo-Domino Logic 2
ICAL	Improved Clocked Adiabatic Logic
IDFAL	Improved Diode Free Adiabatic Logic
IECRL	Improved Efficient Charge Recovery Logic
IPGAL	Improved Pass-Gate Adiabatic Logic

N

NERL	NMOS Energy Recovery Logic

P

PAL	Pass-transistor Adiabatic Logic
PFAL	Positive Feedback Adiabatic Logic
PSAL	Pre-resolve and Sense Adiabatic Logic

Q

QCA	Quantum Dot Cellular Automata
QSERL	Quasi-Static Energy Recovery Logic
QSSERL	Quasi-Static Single-phase Energy Recovery Logic

R

REL	Recovered Energy Logic
RERL	Reversible Energy Recovery Logic

S

SCAL	Source Coupled Adiabatic Logic
SCRL	Split-level Charge Recovery Logic
SPGAL	Symmetric Pass Gate Adiabatic Logic
SQAL	Secured Quasi Adiabatic Logic

T

TSEL	True Single-Phase Energy Recovery Logic

2PADCL	Two Phase drive Adiabatic Dynamic CMOS Logic
2PADL	Two-phase adiabatic dynamic logic
2PASCL	Two-phase clocked adiabatic static CMOS logic
2PC2AL	Two-Phase Clocked CMOS Adiabatic Logic
2P-PFAL	Two-Phase Positive Feedback Adiabatic Logic

CHAPTER-1

Introduction

1.1. Background

The history of semiconductors is a attractive journey that has revolutionized the field of electronics. Since the discovery of the transistor in the mid-20th century, the semiconductor industry has undergone remarkable advancements. The foundations of semiconductor technology were laid in the early 20th century. In 1904, the physicist John Ambrose Fleming invented the vacuum diode, which allowed the unidirectional flow of electric current. This marked the beginning of active electronic components. Later, in 1947, William Shockley, invented the transistor, which proved to be a significant breakthrough in semiconductor technology. The transistor supplanted cumbersome vacuum tubes and facilitated the development of compact, more proficient electronic equipment (Bardeen & Brattain, 1948).

1.1.1. Small-Scale Integration (SSI)

The concept of integrating multiple transistors onto a single semiconductor substrate emerged in the late 1950s. Jack Kilby created the first germanium-based integrated circuit (IC) in 1958. This initial IC, consisting of a few transistors and passive components, typically around 3 to 30 components, was the precursor to SSI technology. Simultaneously, Robert Noyce, from Fairchild Semiconductor, independently developed a comparable integrated circuit utilizing silicon. These ground-breaking developments set the stage for the rapid advancement of semiconductor technology (Kilby, 1964).

1.1.2. Medium-Scale Integration (MSI)

The 1960s witnessed further progress in integrated circuit technology, leading to the birth of medium-scale integration (MSI). By using improved manufacturing processes and techniques, engineers were able to fit hundreds of transistors on a single chip, typically ranging from 30 to 100 components. In 1961, Fairchild Semiconductor introduced the first commercial IC, which contained multiple transistors, resistors, and capacitors. This development marked the transition from SSI to

MSI technology. MSI circuits found applications in various fields, including the military, aerospace, and early computers (Drummond, 2013).

1.1.3. Large-Scale Integration (LSI)

As the semiconductor industry continued to evolve, researchers and engineers sought to increase the complexity and density of integrated circuits. Large-scale integration (LSI) emerged as a significant milestone in this pursuit. Gordon Moore, made the legendary prediction in 1965, which represents as Moore's Law. This observation became a driving force for the development of LSI technology (Moore, 1975; Dennard et al., 1974). The transition from MSI to LSI was facilitated by advances in semiconductor manufacturing processes, such as the introduction of planar technology and the use of photolithography. This marked the beginning of a new era where more complex circuits could be realized on a single chip.

1.1.4. Very Large-Scale Integration (VLSI)

VLSI technology emerged in the late 1970s as a result of the desire to achieve greater degrees of integration and enhanced performance. VLSI technology marked a substantial advancement, enabling the incorporation of millions of transistors into a single die. This marked the birth of modern microprocessors and advanced digital systems (Abed & Siferd, 2003). The VLSI era was characterised by advancements in semiconductor fabrication processes, including the complementary metal-oxide semiconductor (CMOS) technology. It delivers reduced power usage, increased packing density, and improved performance, making it the dominant technology for VLSI designs. Additionally, computer-aided design (CAD) tools contribute significantly to the design and verification of complex VLSI circuits. By the 1990s, VLSI technology had become the foundation of modern computing, enabling the development of powerful microprocessors, memory devices, and system-on-chip (SoC) designs (White, 1982). The continuous progress in VLSI technology made it possible to realise ever more intricate and sophisticated electronic systems (Moore, 1975).

1.1.5. Ultra-Large-Scale Integration (ULSI)

ULSI refers to the process of placing an extremely large number of transistors—typically millions or billions—onto a single integrated circuit. This technology is key to modern electronics, enabling compact, high-performance devices like microprocessors and memory chips. As ULSI

circuits become more advanced, challenges such as managing heat dissipation, reducing power consumption, and improving signal transmission efficiency arise. Recent innovations include the use of materials like copper and low-dielectric insulators to optimize performance. Additionally, research into new interconnect technologies, such as carbon nanotubes, aims to address limitations of traditional materials and further enhance the scalability and speed of ULSI circuits (Li et al., 2024; Shacham-Diamand, 2024).

1.2. Problem Description

The history of semiconductors has witnessed remarkable advancements, from the innovation of the transistor to emergence of VLSI technology. The evolution from SSI to MSI, LSI, and ultimately VLSI has enabled the integration of an ever-increasing transistors on a single chip, resulting in electronic gadgets that are more compact, potent, and energy-efficient. According to Moorse's Law, a single chip can now contain billions of transistors. Due to the high number of transistors, ICs offer remarkable processing capabilities. The historical, contemporary, and projected device transistor counts are shown in Fig. 1.1. For the first 40 years, we were able to expand largely due to advancements in our manufacturing method. However, the increasing power density of these tightly packed IC chips prohibits designers from utilising these capabilities. Therefore, even though it is possible to place nearly a billion transistors on a single die, circuit designers for low-power applications cannot do so, as they are extremely limited by these power concerns (Rabaey, 1999).

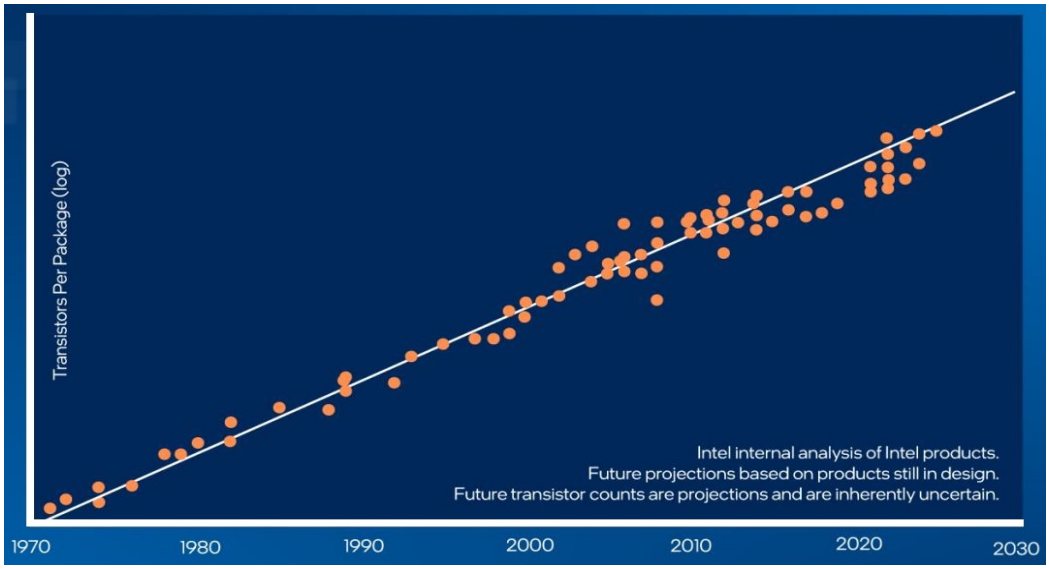

Fig.1.1: Number of transistors per device: past, present, future (Intel Corporation, 2023)

1.3. Motivation

The implementation of low-power design is of utmost significance in order to prolong the lifespan of batteries, particularly considering the constrained advancements in battery technology (Kuroda & Hamada, 2000). The prevalence of high-speed systems, including microprocessors, has become increasingly widespread, resulting in heightened power consumption, concerns over reliability, and the emergence of heat-related complications. The consideration of low-power design is of utmost importance for portable and high-performance systems since an increase in clock frequency leads to a corresponding rise in power dissipation. A range of methodologies, encompassing device features and algorithm selection are employed in order to mitigate power usage (Alioto, 2012). The development of integrated circuits has witnessed advancements in transistor density and enhanced switching rates, resulting in improved overall system performance. Nevertheless, the endeavour to achieve optimal performance has resulted in heightened power and energy dissipation, hence requiring more expensive cooling and packaging solutions (Bellaouar & Elmasry, 2012). It is anticipated that high-end microprocessors will consume a considerable amount of power in the future, thereby highlighting the imperative for the development of creative solutions aimed at reducing power consumption.

1.4. Low-Power Design Methodology

To enhance digital systems' energy dissipation capabilities, it is crucial to incorporate low-power approaches across the whole design continuum, which encompasses the system-level as well as the process-level (Rabaey & Pedram, 2012). This task should be implemented with a simultaneous focus on maintaining optimal performance. In the context of this optimization quest, a basic prerequisite is a deep understanding of power distribution within a processor (Bearden et al., 1995). Therefore, it is crucial to carefully tune the individual components or modules that contribute significantly to power consumption to accomplish power conservation. Figure 1.2 illustrates a low-power design methodology across several hierarchical levels, such as system, algorithm, architecture, circuit, and device (Unsal & Koren, 2003). Every level of design is thoroughly examined in terms of its unique concerns, difficulties, and methodological methods. By incorporating these strategies, designers can achieve optimal power efficiency while maintaining the system's performance integrity. The dominant usage of portable gadgets and the growing prevalence of the occurrence of Internet of Things (IoT) have required the creation of energy-efficient VLSI

design processes. These methodologies are designed to extend battery life and attain maximum power optimization.

1.4.1. System Level Design

The primary objective at the system level is to augment the overall power efficiency of VLSI system. Methods like dynamic voltage and frequency scaling (DVFS) are applied to modify operating voltage and clock frequency dynamically based on the system workload. Power management schemes like power gating and body-biasing are also used to minimise leakage power. Furthermore, system-level optimizations involve careful system partitioning and resource allocation to exploit parallelism and reduce power consumption (Unsal & Koren, 2003).

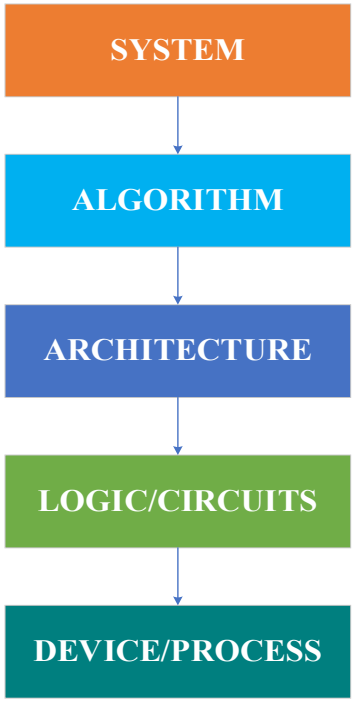

Fig.1.2: Low Power Design Methodology

1.4.2. Algorithm Level Design

At the algorithm level, power optimization techniques aim to reduce computational complexity and data movement. Algorithmic modifications, such as algorithmic-level parallelism, can distribute the workload across multiple processing units, enabling power-efficient execution. Furthermore, we can optimize algorithms to minimize memory access, thereby reducing power

consumption. Techniques such as algorithmic pruning and approximation algorithms can trade off accuracy for reduced computational requirements and power consumption (Benini & Micheli, 2000).

1.4.3. Architecture Level Design

At the architecture level, power optimization techniques involve designing efficient hardware structures that perform computations with minimal power consumption. Approaches such as instruction-level parallelism and pipelining exploit parallelism within the processor architecture to attain better throughput as well as increase power optimization (Raghunathan et al., 2012). To reduce power use, architecture-level improvements also include using energy-efficient interconnects, memory hierarchies that work well, and specialized circuits like application-specific integrated circuits (ASICs) (Chen & Kucukcakar, 1997).

1.4.4. Circuit-Level Design

Circuit-level techniques focus on reducing power dissipation through circuit-level optimizations. These techniques rely on design strategies such as clock gating and voltage scaling to minimize dynamic power loss. Transistor sizing, power gating, and the use of low-leakage transistors are also employed to reduce leakage power (Macii et al., 1997). Furthermore, circuit-level optimizations consider the reduction of parasitic capacitance and resistance to minimize power dissipation (Rabaey & Rabaey, 2009).

1.4.5. Device Level Design

At the device level, power optimization techniques aim to enhance the efficiency of individual transistors. These techniques include the utilisation of sophisticated process technology, like FinFET, which offers better control over leakage power and improved performance. Additionally, Kim et al. (2010) suggest using techniques like threshold voltage adjustment and advanced packaging technologies like through-silicon vias (TSVs) to lessen power usage. Low-power VLSI design is a multidimensional challenge that requires careful consideration at various design levels. System, algorithm, architecture, circuit, and device-level designs collectively contribute to achieving optimal power efficiency while maintaining system performance. By integrating these levels of design techniques, designers can achieve substantial power savings in VLSI systems for a wide range of applications. These strategies ensure efficient transistor operation, minimized leakage

power, and enhanced interconnectivity, resulting in comprehensive power optimization and improved energy efficiency.

1.5. Different Power Consumptions in Digital CMOS Circuit

In a CMOS circuit, the overall power consumption, denoted as, P_{total}, has two primary constituents: dynamic power, referred to as $P_{dynamic}$ and static power, denoted as, P_{static}. Mathematically (Wiltgen et al., 2013):

$$P_{total} = P_{dynamic} + P_{static} \tag{1.1}$$

The term $P_{dynamic}$ pertains to the electrical power used by a circuit while it is engaged in productive tasks during the active mode. On the other hand, P_{static} denotes the power dissipated, once the circuit is idle, known as leakage current (Rabaey, Chandrakasan, & Nikolic, 2003; Jan et al., 2003). Fig. 1.3 presents a comprehensive overview of the many categories of power use (Ng et al., 2022).

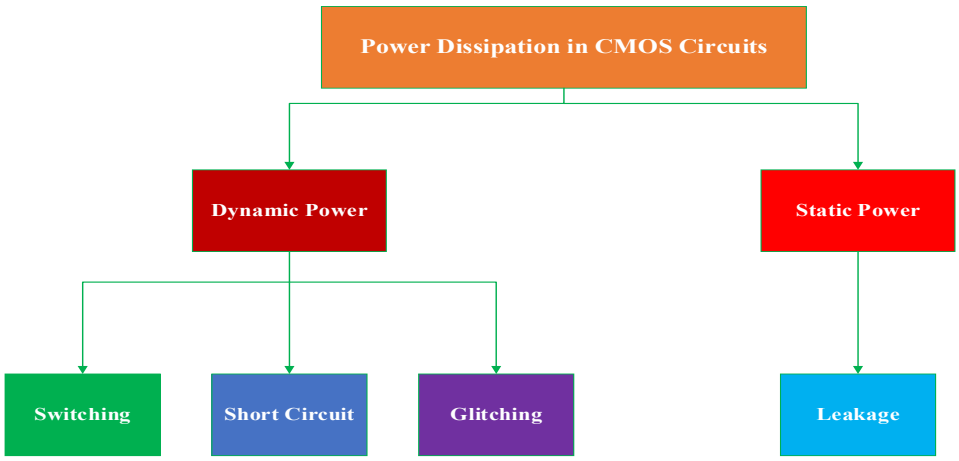

Fig.1.3: Classifications of Various Power Consumptions in CMOS Circuits.

1.5.1. Dynamic Power Consumption

In CMOS, dynamic power dissipation refers to energy consumption as a result of the parasitic capacitors' charging or discharging energy, depending on the input of the logic circuits. This effect is observed during the process of transitioning between two logical states and is directly influenced by both the operating frequency and the magnitude of capacitance. The fundamental composition of dynamic power dissipation "includes three" distinct constituents (Liu & Svensson, 1994).

1.5.1.1. Switching Power Consumption

During the charging phase, as shown in Fig. 1.4(a), the output logic changed from a LOW to HIGH state because the PMOS and NMOS path transistors were ON and OFF, correspondingly. Current $I(t)$ flows to the output capacitor C_L and, as a result, charges up and stores energy. This energy-stored E_D can be evaluated as given below (Ng et al., 2022).

$$E_D = \int_0^\infty i(t) \, . \, V_{DD} dt \tag{1.2}$$

To get the capacitor voltage charged, the corresponding current is given as,

$$i(t) = C_L \frac{dV_{DD}}{dt} \tag{1.3}$$

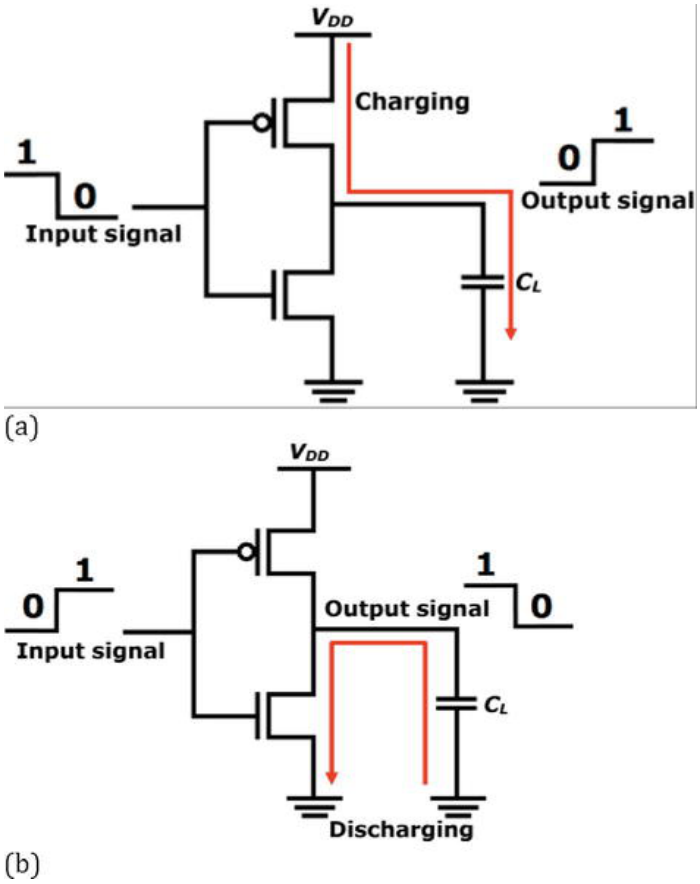

Fig.1.4: CMOS inverter (a) Charging from VDD to CL
(b) Dis-charging from CL to GND

E_D in Eq. (1.2) can, therefore, be expressed as (Jan et al., 2003).

$$E_D = C_L {V_{DD}}^2 \tag{1.4}$$

Therefore, it is possible to determine the energy E_C stored in C_L during each transition's charging phase as (Bartiromo & De Vincenzi, 2016),

$$E_C = \int_0^\infty i(t).v(t)\,dt = \frac{1}{2} C_L V_{DD}^2 \tag{1.5}$$

$i(t)$ represents the instantaneous charging current as a function of time during charging or discharging process. During charging, as depicted in Fig. 1.4 (a), $i(t)$ is the current flowing from V_{DD} to the capacitor, and $v(t)$ represents the instantaneous voltage across the capacitor C_L as a function of time during the charging process. Hence $v(t)$ is voltage across the capacitor, which increases over time from 0 to V_{DD}.

Equations (1.4) and (1.5) illustrate the distribution of energy in a CMOS circuit. The phenomenon, known as switching activity, requires prioritizing Eq. (1.5) over Eq. (1.4) when evaluating switching power consumption. The main objective of Eq. (1.4) is to focus solely on an individual state transition. However, it is important to recognize that real-world situations often involve more complex interactions of signal changes at the circuit node. The complexity in question arises due to the possibility of many transitions occurring within a specified time span within the incoming signal. Therefore, in order to calculate the total delivered power, referred to as E_{Dt}, it is necessary to scale Eq. (1.4) by a factor N, which represents the total number of transitions. Consequently, (Pal, 2015)

$$E_{Dt} = N.C_L {V_{DD}}^2 \tag{1.6}$$

Consider a node within a circuit that alternates at a frequency f_{switch} throughout a period T, then N may be defined as,

$$N = T.f_{switch} \tag{1.7}$$

From eq. (1.7) into eq. (1.6), the overall energy may be described as (Cutitaru, 2014).

$$E_{Dt} = T.f_{switch} C_L {V_{DD}}^2 \tag{1.8}$$

Now switching power P_{switch} and total energy E_{Dt} can be characterized as,

$$P_{switch} = \frac{E_{Dt}}{T} \tag{1.9}$$

Using Eq. (1.8) into (1.9), we can write,

$$P_{switch} = f_{switch}.C_L{V_{DD}}^2 \tag{1.10}$$

Equation (1.10) is applicable for precise computation of P_{switch}, provided that the assumption stated in Eq. (1.7) remains valid. In most CMOS circuits, it is crucial to recognize that the switching behaviour of logic components does not display a uniform frequency. Hence, it is more compelling to articulate the concept of f_{switch} in relation to the multiplication of $AF$and the clock frequency f_{clk} (Weste & Harris, 2015).

$$f_{switch} = AF.f_{clk} \tag{1.11}$$

Therefore, Eq. (1.10) may be expressed as (Leblebici, 2004),

$$P_{switch} = AF.f_{clk}.C_L{V_{DD}}^2 \tag{1.12}$$

The variable C_{dyn}, sometimes referred to as the dynamic effective capacitance, is used to denote the product of C_L, and AF, or $\left(AF.C_L = C_{dyn}\right)$. Therefore, Eq. (1.12) may be reformulated as (Roy & Malik, 1994),

$$P_{switch} = f_{clk}.C_{dyn}.{V_{DD}}^2 \tag{1.13}$$

The probability of a circuit node moving from logic 0 to 1 state is the definition of the activity factor, (AF) given by Weste and Harris (2015). Hence, the inclusion of (AF) in the estimation of a circuit's power consumption has significant importance. The probability of a circuit node migrating to logic state 0, designated ${P_f}^0$, and logic state 1, designated ${P_f}^1$, can be multiplied to find the AF value for a circuit node exhibiting irregular switching patterns. When expressed mathematically, AF is,

$$AF = P_f^0 \times P_f^1 \tag{1.14}$$

As an illustration, consider an XOR-gate with the expression $Y = A\overline{B} + \overline{A}B = A \oplus B$ for a switching function. Table 1.1 presents the function's truth table (Norouzi & Heikalabad, 2019). Only two of the four possible input values result in logic 1 at output Y, while the other two all result in logic 0, as depicted in the truth table. As a result, we may write ${P_f}^0$ as $\frac{2}{4}$ and ${P_f}^1$ as $\frac{2}{4}$. Using these numbers in Eq. (1.14), we obtain a value for (AF) of 0.25. This means that there is just a 0.25

percent chance that the circuit is actually on. By contrasting this figure with the occurrence of a high state in the Boolean table, we are able to notice that the activity factor is an effective measure of the circuit's operational rate.

Table 1.1: Truth Table of XOR-gate

Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

1.5.1.2. Short Circuit Power Consumption

When loading and discharging the parasitic capacitance, the circuit delays its transitions in the logic state. Employing NMOS and PMOS transistors during switching events results in power loss due to short circuits. Both types of transistors conduct at the same time during logic state transitions, making a straight current channel from V_{DD} to ground. The short-circuit current going through the transistors thru the transitional stage as depicted in Fig. 1.5. This characteristic renders the operation inefficient and unpredictive. The mathematical expression for short-circuit power, symbolized as (P_{short}), can be obtained using the following derivation (Veendrick, 1984).

$$P_{short} = T_{sc}.V_{DD}.I_{peak} \tag{1.15}$$

The parameter T_{sc} represents the duration of the ascending or descending edge of the input signal, while I_{peak} corresponds to the peak current. The estimation of I_{peak} can be inferred from the characteristics of the transistor, such as its dimensions and the technological technique used (Nose & Sakurai, 2000).

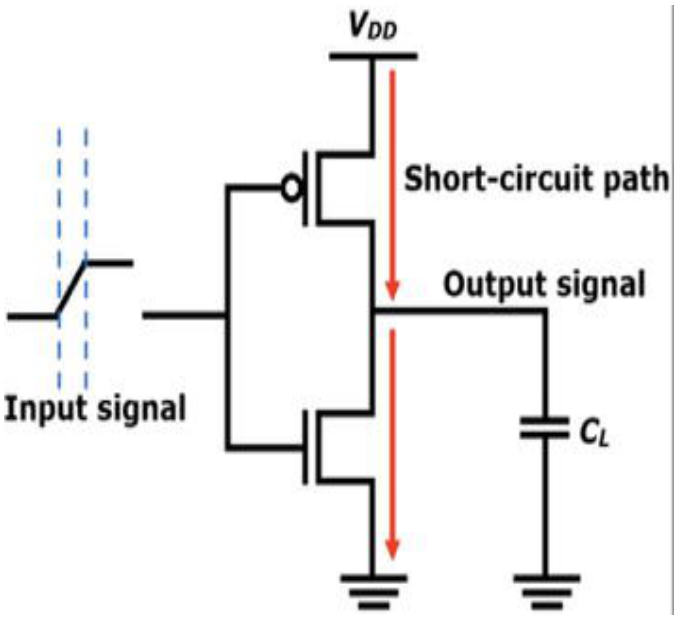

Fig. 1.5: Graphical representation of short-circuit path in CMOS inverter.

1.5.1.3. Glitching Power Consumption

The term "glitches" refers to short and unintentional aberrations in the logical states present within a digital circuit (Raghunathan et al., 1996). The presence of these events can be attributed to a range of causes, encompassing signal reflections, noise coupling, and inherent delays in signal transmission. When a fault arises, it triggers temporary shifts between logical states, resulting in the production of dynamic power dissipation within the CMOS circuit (Choi et al., 2001). It is well acknowledged that in real-world applications, every logic gate demonstrates finite delays, resulting in the manifestation of glitches as a consequence of these intrinsic delays. When the input variables A, B, and C change from 010 to 111, as shown in Fig. 1.6, the associated output values exhibit the following evolution: Initially, with input values 0 and 0, the respective output values are O1 = 1 and O2 = 1 (Safaiezadeh et al., 2021). Nevertheless, when the input is modified to 111, the resulting output undergoes a transformation such that O1 becomes 0 and O2 becomes 1. In all instances, it is assumed that an ideal scenario is present, wherein gate delays can be considered insignificant. Nevertheless, the incorporation of gate delays results in divergent consequences. The inclusion of gate delays in output replies becomes necessary when even a slight delay is present, resulting in the occurrence of glitches (Raghunathan et al., 1999).

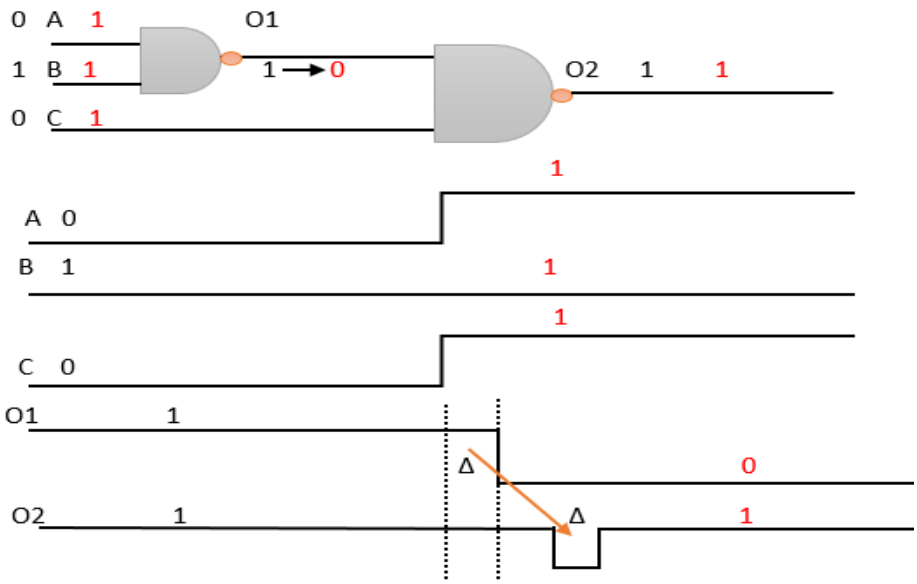

Fig. 1.6: Transition of signals through logic gates

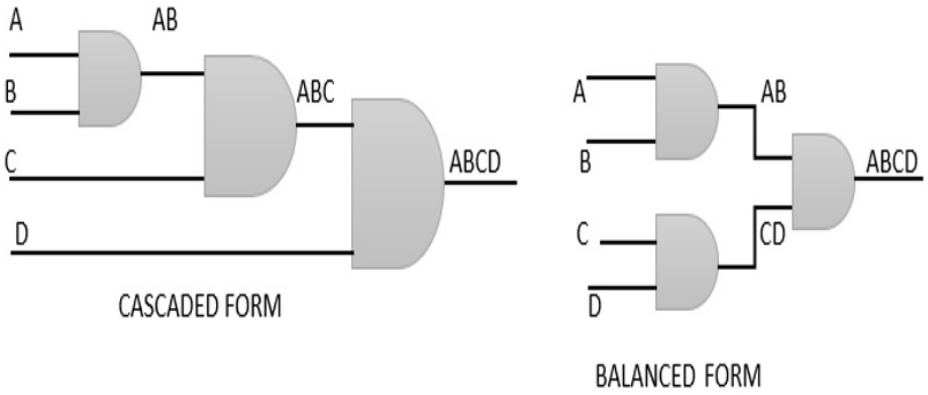

Fig.1.7: Reduction of glitching using gates

The output exhibits consistent behaviour across all contexts, and the quantity of logic gates remains constant (Zhou & Roy, 2020). By ensuring that signals arrive simultaneously at both the terminals of the first and second circuits shown in Fig. 1.7, we mitigate glitch intensity and eliminate any latency discrepancies. Upon comparing the two figures, it becomes evident that there is an added benefit, namely, a decrease in the latency of the critical path. In the initial diagram, the attainment of outputs necessitates the use of three gates, but in the subsequent diagram, the outputs are attained through the utilization of only two gates. The mitigation of power dissipation related to the glitch can be achieved by implementing the circuit in a balanced configuration as opposed to a cascaded configuration (Raghunathan et al., 1999).

1.5.2. Static Power Consumption

In simple terms, "static power" is the amount of energy that a circuit or gadget uses even when it's not performing anything (Zhou & Liu, 2020). The term is most often used to describe the power drain of a CMOS circuit during its idle state. A major challenge, exemplified by the worsening of leakage current, has emerged with the shrinking of the technological node to sub-nanometre scales. Intel Corporation introduced the $22nm$ tri-gate transistor, also known as the $FinFET$ because of its structural likeness to the fin of a fish, in 2011 when the severity of leakage current reached a crucial juncture (Zhang & Smith, 2023).When comparing $FinFET$ to planar MOSFETs, it is clear that the former provides more precise regulation of current flow, hence reducing leakage (Yeap et al., 2019). According to Jacob et al. (2010), the loss of static power is greatly influenced by short-channel phenomena, including gate leakage and sub-threshold currents. The impact is audible at gate voltages below V_{th} (Kuo & Lin, 2002), which represents the threshold voltage. According to the referenced paper (Sharroush, 2020), sub-threshold leakage increases at an exponential rate with decreasing feature size. The main component that determines this phenomenon is the decrease in threshold voltage, V_{th}. As the size of transistors decreases, thickness of oxide film also decreases. This trend stays the same until a threshold voltage is applied to the gate terminal. At that point, a negative electric field appears at point where oxide layer meets the substrate. This event culminates in the emergence of gate leakage current, as seen in Chinta (2007). Current leakage worsens when technology nodes move into the nanometric domain, despite the common belief that sub-threshold leakage has a greater impact. Static power loss may be represented by the following equation:

$$P_{static} = V_{DD}.I_{leakage} \tag{1.16}$$

where $I_{leakage}$ denotes the total leakage current.

1.5.2.1. Leakage Currents

The fundamental leakage currents observed in Metal-Oxide-Semiconductor (MOS) transistors are graphically illustrated in Fig. 1.8 (Bikki & Karuppanan, 2017). Considering the device's channel is not conducting at this time, three distinct categories of leakage currents manifest (Wang & Yin, 2024), namely the sub-threshold (I_{Sub_th}), gate-induced drain leakage (I_{GIDL}), and punch-through (I_{Punch}), as documented by a previous study (Roy et al., 2003). Additionally, the

realm of non-conduction-related leakage currents encompasses two further entities: the gate tunnelling current $(I_{tunnel})$and the reverse bias leakage across the pn junction $(I_{junction})$, both of which emanate from a band-to-band tunnelling phenomenon (Calimera et al., 2012; Tanizawa et al., 1993).

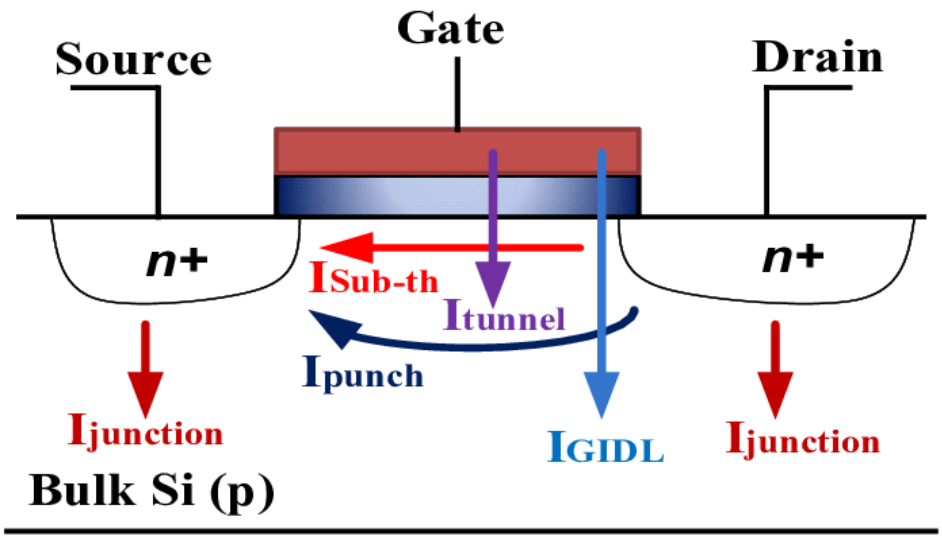

Fig.1.8: Leakage currents in a MOSFET (Bikki & Karuppanan, 2017)

1.5.2.2. Sub-Threshold Current

A small sub-threshold current, passes through source and drain of a MOSFET once its gate voltage is lower than its V_{TH} $(V_{GS} < V_{TH})$. Minority carrier concentration is tiny and channel length dependent inside this weak inversion region. While diffusion current is predominant in mild inversion regions, drift current is prominent in strong inversion regions (Antognetti et al., 1982; Narendra et al., 2002). Considering a non-volatile bipolar transistor (NMOS) that has a drain-to-source voltage greater than 1V and a source voltage less than zero $(V_G < V_{TH})$. As mentioned in citations (Rao et al., 2004), the existence of an opposite-biased p-n junction at substrate-drain connection causes weak inversion current to completely disappear under these circumstances. In the weak inversion zone, the following formula governs the drain current of the NMOS transistor (Pavasovic et al., 1994; Chang et al., 2010; Jadav & Chandel, 2018)

$$I_{D(weakinversion)} = I_{on}.e^{\left(\frac{V_{GS}}{V_T}\right)} \quad (1.17)$$

Where, η is sub-threshold slope coefficient;

V_T is thermal voltage equal to q/KT (Alioto & Palumbo, 2000; Alioto & Palumbo, 2003)

; and I_{on} is $\mu_0 C_{ox} \left(\frac{W}{L}\right) {V_t}^2 . e^{1.8}$.

Where q denotes elementary charge of an electron, which is nearly 1.602×10^{-19} C, T denotes the absolute temperature in Kelvin, k is Boltzmann's constant, which has a value of nearly $1.381 \times 10^{-23} J / K$, , and q / kT is part of the expression for thermal voltage, V_t, which represents the potential difference caused by the temperature-driven movement of charge carriers. The thermal voltage is important for calculating various parameters in sub-threshold operation. I_{on}, the current flows among the drain and source of MOSFET when the transistor is "on," even though it's operating in sub-threshold region($V_{GS} < V_{TH}$).

This current depends on several factors:

μ_0: This signifies the mobility of charge carriers (NMOS) in the absence of electric field.

C_{ox}: Gate-oxide capacitance per unit area, which plays a acute role in controlling the MOSFET's behaviour, as it determines how much charge is stored at the gate.

W / L: Width-to-length ratio of MOSFET channel, which influences the current flowing through device.

V_t: Threshold voltage.

The exponential term $e^{1.8}$: This represents a factor related to the sub-threshold conduction and accounts for the exponential nature of current flow in this region.

1.5.2.3. GIDL

In occurrence of a strong electric field, band-to-band tunnelling takes place at the overlapped area of the gate and drain, leading to GIDL. As the depletion layer nearby to surface thins, electric field grows stronger. GIDL is more noticeable when a single-diffused drain is used instead of a double-diffused one. The GIDL current can flow via the drain depletion zone underneath the gate area when the subtract voltage is low (Guo et al., 1998). A simple mathematical model showing the consequence of gate work function on electric field at gate-drain overlap is given by Eq. (1.18)

(Gupta & Shukla, 2015; Mohanty & Kougianos, 2010). Figure 1.9 illustrates the gate-source voltage with the drain current.

$$E_{Total}^2 = \frac{\frac{V_{DG}}{T_{ox}}\left(1-\frac{V_{FB}-\psi_S}{V_{DG}}\right)^2+\frac{V_{DG}^2}{\gamma h}}{T_{ox}} \tag{1.18}$$

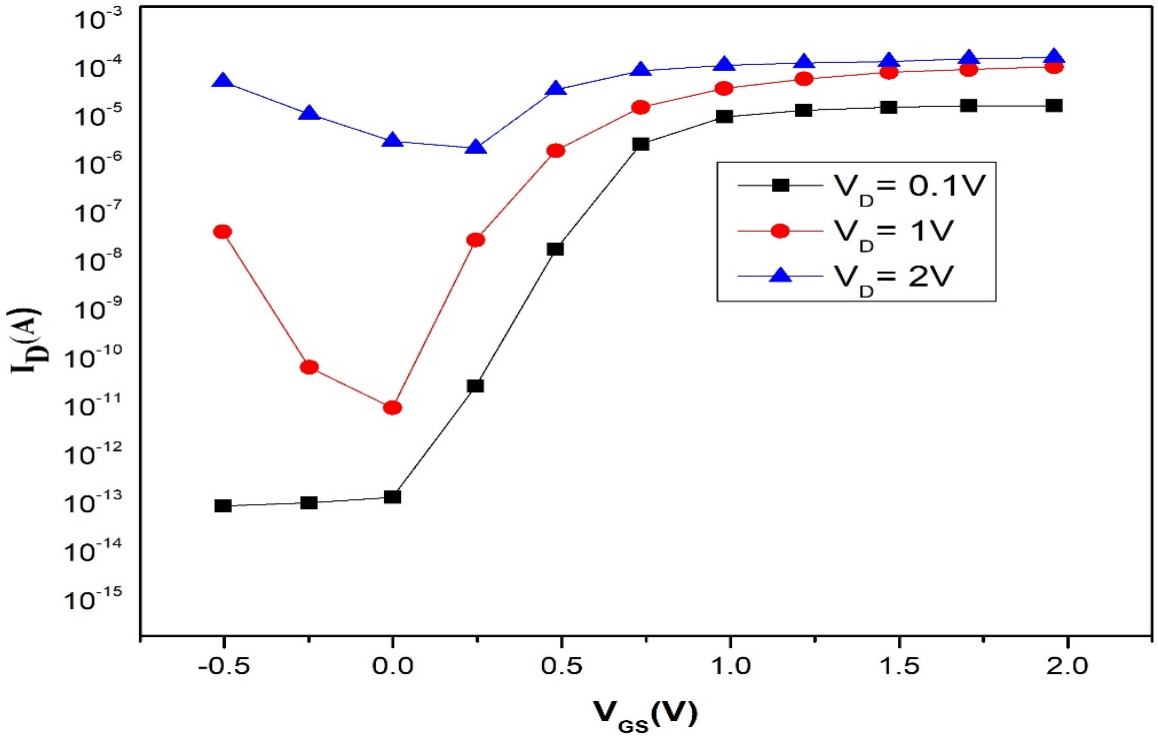

Fig.1.9: Gate-source voltage vs. drain current (Bikki & Karuppanan, 2017)

From a tunnelling theory perspective, the I_{GIDL} current may be expressed as (Ghodsi et al., 1998)

$$I_{GIDL} = AE_{GIDL}^2 \exp\left(\frac{-B}{E_{GIDL}}\right) \tag{1.19}$$

In this context, ψ_S represents the $BTBT$ potential drop over silicon, h is a parameter connected to the depth of the junction, E_{GIDL} means the electric field responsible for the $GIDL$ current, and A and B are constants that help with tunnelling (Yuan et al., 2008; Ana & Najeeb, 2012).

1.5.2.4. Punch-Through Current

When the sum of the two widths, x_{dS} (depletion width on source side) and x_{dD} (depletion width on the drain side), equals the channel length, L, or $x_{dS} + x_{dD} = L$, in MOS transistors, the punch-through current happens (Tanizawa et al., 1993). The depletion zone boundaries are narrowing due to the constant short-channel doping concentration (Gupta & Lahiri, 1990). In submicron technology, there was a noticeable difference in doping concentration between the surface and substrate. Due to the expansion of the depletion zone towards the substrate, punch-through current below the surface increased (Fu & Tsang, 1997). There are many methods for lowering the punch-through current; some of them include raising the substrate doping level, using thinner oxide layers, introducing moderately sized junctions, and, of course, using longer channel lengths. In devices with short channels, two voltages—the drain-to-source voltage V_{DS} and the gate-to-source voltage V_{GS}—influence the potential barrier (Gupta & Lahiri, 1990). Increases in the drain voltage cause a decrease in the short channel's potential barrier, a process called drain-induced barrier lowering (DIBL) (Fu & Tsang, 1997a). Dimensions of the drain and source junctions are often denoted as below (Dennard et al., 1974; Fu & Tsang, 1997).

$$x_{dD} = \sqrt{\left[\frac{2\varepsilon_{Si}}{qN_A}\right]\left(V_{DS} + \phi_{si} + V_{SB}\right)} \tag{1.20}$$

Where:

- x_{dD} refers to the depletion width on the drain side.
- ε_{si} represents the permittivity of silicon.
- q , is elementary charge, approximately 1.602×10^{-19} C.
- N_A , is substrate doping concentration.
- ϕ_{si} , is silicon surface potential.
- V_{SB} , is source-to-bulk voltage.

$$x_{ds} = \sqrt{\left[\frac{2\varepsilon_{Si}}{qN_A}\right](\phi_{si} + V_{DB})} \tag{1.21}$$

Where:

- x_{dS} refers to the depletion width on the source side.
- V_{DB} refers to the drain-to-bulk voltage.

The saturation level of the sub-threshold surface diffusion current $\left(I_{Sdif}\right)$ for the short channel $\left(|\mathrm{Vds}| > \frac{4\mathrm{kT}}{\mathrm{q}} \approx 0.1\mathrm{V}\right)$ can be expressed as (Barron, 1972; Borkar, 2011).

Where:

$$\mathrm{I_{Sdif}} = \frac{\mathrm{Dn_i^2 e^{\left(\frac{q\Delta\phi_s}{kT}\right)}}}{\mathrm{L_{eff}}} \tag{1.22}$$

Where:

- D represents the constant associated with the surface diffusion of minority carriers. (Keshavarz et al., 1997).
- n_i, is intrinsic carrier concentration in material (Keshavarz et al., 1997).
- $\Delta\phi_s$ denotes the change in surface potential caused by variations in V_{GS} and V_{BS}.
- L_{eff}, is the effective channel length.

Additionally, $\Delta\phi_s$ is further defined as:

$$\Delta\phi_s = \Delta\phi_{so}\left(V_{gs}, V_{bs}\right) + m\left|V_{ds}\right| \tag{1.23}$$

Where:

- $\Delta\phi_{s0}$ refers to the change in surface potential under zero bias conditions.
- m, is a dimensionless constant factor.

The terms DS and ds, though closely related, refer to different aspects of the MOSFET. DS refers to V_{DS}, that is the voltage difference between the drain and source terminals. On the other hand, ds refers to the source-to-drain distance, related to the length of the channel. Additionally, $\Delta\phi_s$ stands for the alteration in surface band structure (surface-band-bending) resulting from

variations in V_{gs} and V_{bs}. The parameter m represents a unitless constant factor. Beyond these, two distinct forms of leakage currents exist that remain unaffected by the device's conduction characteristics (Calimera et al., 2012). The current which passes through gate and the reverse bias that leaks out of the pn junction due to the band-to-band tunnelling effect (I_{BTBT}) are described in the references (Wright & Saraswat, 1990; Tanizawa et al., 1993).

1.5.2.5. Gate Tunneling Current

Gate tunneling current arises as a consequence of the substantial electric field that develops across the thin oxide layer. Magnitude of gate tunneling current is contingent upon both the configuration of the device and the specific biasing circumstances. While the electric field is strong enough, a process called quantum electron tunneling takes place, utilizing the oxide layer among the gate and the bulk to transport electrons in both directions. The wave pattern associated with a charged carrier in quantum mechanics explains this behavior (Srikantaiah & DasGupta, 2012). Because the potential barrier is extremely small, charged electrons may efficiently pass through the oxide layer, which significantly increases the gate current (Chen et al., 1998; Yang et al., 2000). The magnitude of gate tunneling current is contingent upon both the configuration of the device and the specific biasing conditions. Within a miniaturized device, gate tunneling current encompasses not only a gate-to-channel current (I_{gc}) but also direct tunneling currents at the device edges (I_{gso}) and (I_{gdo}) (Maikusiak & Badri, 2000; Stadele et al., 2001).

$$I_g = I_{gc} + I_{gso} + I_{gdo} \tag{1.24}$$

Fowler-Nordheim (FN) and direct tunneling are the two main forms of gate tunneling current. According to Larcher et al. (2001) and Yang et al. (2001), electrons in the FN tunneling process are directly injected into the conducting band via hopping over the oxide layer's potential barrier ϕ_{ox}. The source-drain extension and gate overlap occur, and in the midst of this overlap, the direct tunneling current emerges. This type of tunneling predominantly proceeds through electron tunneling from both conduction and valence bands. Notably, this phenomenon's sensitivity is greatly reliant on the thickness of the gate oxide (Wang & Roy, 2021). The FN current expression characterizes tunneling by crossing a triangular potential barrier and holds true when $V_{ox} > \phi_{ox}$ and the electric potential difference across an oxide layer is represented by V_{ox}. The mathematical description of current density of FN tunneling is given by (Saheb & El-Masry, 2015),

$$J_{FN} = \frac{q^3 E_{ox}^2}{16\pi^2 h\phi_{ox}} exp\left(-\frac{4\sqrt{2m}\phi_{ox}^{\frac{3}{2}}}{3hqE_{ox}}\right) \quad (1.25)$$

The symbols E_{ox} and ϕ_{ox} represent the electric field across the gate oxide's surface and the dimension of the potential barrier for electrons, respectively. According to many studies (Bowman et al., 2001), the parameter m represents the mass of an electron located in the band associated with conduction (Choi et al., 2001).

1.5.2.6. Junction Leakage

It is common for a reverse bias situation to occur at the body-to-source and body-to-drain connections. A reverse bias leakage current is made across the pn junction as a result of this. Devices with tiny geometries experience leakage due to BTBT when the p and n regions exhibit strong doping. In a reverse-biased pn circuit, the depletion area also forms pairs of electrons and holes. According to Murakami and Shingyouji (1994), the amount of doping and the size of the depletion zone are the primary factors that determine the amount of reverse bias pn junction leakage current. The BTBT current density J_{S-B} (source to body) is expressed as follows (Wang & Zhang, 2020; Xu et al., 2013; Rosar et al., 2000).

$$J_{S-B} = A\frac{E.V_{app}}{E_g^{0.5}}.\mathrm{e}^{\left(-B\frac{E_g^{3/2}}{E}\right)} \quad (1.26)$$

Here, A is the prefactor related to material properties and B is associated with the tunneling probability and is dependent on the material's band structure, particularly the band gap E_g. The E_g is typically expressed in electron volts (eV), and for materials like silicon, it is approximately $1.12\,eV$, V_{app} is reverse bias potential crossways the junction, E is electric field at junction.

1.6. Reductions of Power consumptions

The number of functions integrated into a microprocessor is directly proportional to the computing power of electronic equipment. So, while designing CMOS circuits, power consumption has become an important factor to consider. To reduce power usage in microchips, efficient techniques are required. Optimizing power use begins with measuring a CMOS circuit's total power

consumption. By plugging (1.13), (1.15), and (1.16) into Eq. (1.1), we get the following formula, which represents the entire power dissipation, abbreviated as P_{total} (Weste & Harris, 2015; Chang et al., 2010).

$$P_{total} = \left(f_{clk}.C_{dyn}.V_{DD}^2\right) + \left(T_{sc}.V_{DD}^2.I_{peak}\right) + \left(V_{DD}^2.I_{leakage}\right) \quad (1.27)$$

After doing a more thorough analysis, it becomes apparent that the overall power, P_{total} is influenced by six unique power factors, namely: V_{DD}, f_{clk}, T_{sc}, C_{dyn}, $I_{leakage}$, and I_{peak}(Chen & Huang, 2020). By employing careful and suitable design techniques for the logic circuit, it is frequently feasible to prevent or perhaps eradicate the presence of P_{short} and P_{static}. Therefore, it is common practice to adjust the critical values stated in Eq. (1.27), in order to optimise the circuit's power usage, such as the supply voltage (V_{DD}), dynamic effective capacitance $\left(C_{dyn}\right)$, and clock frequency (f_{clk}). Power dissipation reduction is a critical consideration in CMOS design, encompassing various techniques to minimize both dynamic and static/leakage power consumption. Here's an overview of some common techniques along with their limitations.

1.6.1. Voltage Scaling (Gonzalez et al., 1997)

Diminishing the power source (V_{DD}) directly reduces the dynamic power by reducing the square of the voltage. This method is often used for gadgets that run on batteries and are portable.

Limitation: Decreased performance may result from slower operating speeds caused by reducing the power source voltage.

1.6.2. Clock Gating (Wu et al., 2000)

For reducing dynamic power usage, it is important to disable clock signals in areas of the circuit that are inactive or not in operation.

Limitation: Complex clock gating structures can introduce additional overhead and design complexity.

1.6.3. Multi-Vt (Threshold Voltage) Design (Kursun & Friedman, 2006)

When it comes to important routes, using low-V_t transistors keeps performance stable, while using high-threshold voltage transistors for less essential circuits helps to decrease leakage power.

Limitation: Mixing different V_t transistors complicates the design process and can lead to challenges in maintaining timing margins.

1.6.4. Power Gating (Shin et al., 2010)

Completely powering down inactive blocks or functional units when not in use. This reduces both dynamic and leakage power.

Limitation: Power gating introduces additional control circuitry and can impact the overall system's responsiveness due to power-up delays.

1.6.5. Static/Leakage Power Dissipation Reduction (Borah et al., 1996)

Transistor Sizing: Using larger transistors (increased width) for critical paths reduces leakage current by effectively reducing sub-threshold leakage.

Limitation: Larger transistors occupy more area, which can limit overall circuit density and increase chip size.

1.6.6. Reverse Body Biasing (Keshavarzi et al., 2001)

Transistors may have their sub-threshold leakage current and power significantly reduced by using reverse body bias.

Limitation: Implementing reverse body biasing requires additional circuitry and complicates design considerations.

1.6.7. Leakage Control Cells (Roy et al., 2003)

Adding special cells designed to minimize leakage, like sleep transistors, reduces leakage paths when the circuit is idle.

Limitation: Incorporating leakage control cells can increase area and design complexity.

1.6.8. Sub-Threshold Logic (Wang et al., 2006)

While operating in the sub-threshold area slows down effectiveness, it decreases leakage power.

Limitation: The operation below the threshold necessitates meticulous design deliberations and may not be optimal for every application.

It is crucial to acknowledge that every technique is accompanied by its own set of compromises, and the most suitable combination is contingent upon the particular demands of the design, encompassing factors like performance, power consumption, area limitations, and design intricacy. In addition, with the progression of semiconductor technology, there is a continuous development of novel techniques and procedures aimed at tackling the ever-changing issues associated with reducing power dissipation.

1.7. Thesis Organization

Chapter 1: The history of semiconductors and the evaluation of VLSI technology, starting with SSI, MSI, and LSI, are discussed. The needs of low-power devices are emphasized, and the different power consumptions in digital CMOS designs, such as dynamic power consumption and static power, are elucidated. Different techniques for the currently available low-power design methodologies are discussed, and their limitations are acknowledged.

Chapter 2: This chapter reviews existing adiabatic logic design techniques in chronological order. Quasi-adiabatic design techniques with cross-couple structures are described with diagrams. Analytical explanations of adiabatic switching technology and the benefits of the adiabatic logic approach for low-power digital CMOS architecture were covered.

Chapter 3: This chapter presents improved diode-free adiabatic logic (IDFAL), an approach that obviates the necessity for diodes through the utilization of two-phase, complementary sinusoidal power supply. The circuit functions are maintained through the implementation of the adiabatic switching principle. To establish the efficacy of several CMOS technology nodes, an extensive number of inquiries were conducted. The IDFAL inverter circuit exhibits a 91.59 percent reduction in power delay product (PDP) when associated to the corresponding CMOS inverter that utilizes a 16 nm HP_PTM. (High Performance Predictive Technology Model).

Chapter 4: This chapter examines the performance of Improved Diode Free Adiabatic Logic (IDFAL), an adiabatic circuit, in comparison to conventional CMOS logic and alternative approaches. A split-level sinusoidal power source and a dual-phase timing mechanism are both components of the IDFAL circuit. The research investigates various sequential and combinational

logic circuits at a 45 nm scale by employing the IDFAL. Particular emphasis is placed on SR, D and T flip-flops. In comparison to extant adiabatic design methodologies, the IDFAL circuit exhibits the smallest energy delay product (EDP) and PDP, as evidenced by specter simulators and simulations with Cadence Virtuoso software.

Chapter 5: This chapter presents the single-phase diabatic logic technique, an innovative approach to logic design. Furthermore, the chapter provides a comprehensive blueprint of a 16-bit arithmetic logic unit (ALU), utilizing MOSFET and FinFET fabrication techniques. Notably, the design incorporates the principles of adiabatic switching. The analyses revealed power savings of 67.14%, 39.47%, 34.65%, 8.73%, and 4.16% for MOSFET technology, whereas FinFET technology shows power savings of 95.22%, 21.34%, 20.75%, 15.66%, and 8.69%.

Chapter 6: This chapter introduces Enhanced Positive Feedback Adiabatic Logic (EPFAL), a low-power adiabatic logic that uses sense-amplifier-structured quasi-adiabatic circuits and dual-rail encoded circuits driven by two-phase sinusoidal power-clock sources. EPFAL is affected by charge recovery and restoration of adiabatic and non-adiabatic losses per operating frequency, unclaimed charge, charge sharing, and draft effects. Furthermore, odd and even parity generators and checker circuits utilizing EPFAL-based technology conserve an average of 77.53% and 82.14% of power, respectively, in comparison to CMOS architecture.

Chapter 7: This chapter introduces a completely adiabatic binary-coded-decimal (BCD) 8421 code to Excess-3 (XS-3) code converter prototype that uses less power than standard CMOS and other famous fully adiabatic logic families. The suggested logic demonstrates the promise of BCD in VLSI design by achieving significant power savings at 500 MHz, surpassing CMOS logic.

Chapter 8: This concludes the research and covers all findings and implications. A thorough analysis of the pros and cons of adiabatic logic is conducted. This chapter also discusses adiabatic switching's shortcomings and possible solutions. Future investigations are also addressed.

CHAPTER-2

Literature Review

2.1. Introduction

In digital circuit design, adiabatic logic represents a cutting-edge paradigm, offering a novel approach to address the challenges posed by power dissipation and energy efficiency in modern electronic systems. It is a transformative concept that diverges from traditional, energy-hungry digital logic circuits, introducing a unique design philosophy that places a primary focus on energy conservation. The ingenious engineering of adiabatic logic circuits minimizes the dissipation of energy as heat, thereby unlocking substantial energy savings and reducing environmental impact in the electronics industry. The thermodynamic concept of adiabatic processes, where the system neither gains nor loses energy, gives this pioneering approach to digital circuitry its name. Adiabatic logic circuits mimic this principle by conserving energy, allowing them to operate with minimal power consumption and heat generation. This attribute is especially critical in the era of mobile devices, IoT (Internet of Things) applications, and energy-efficient computing, where power efficiency and extended battery life are of paramount importance. The concept of reversible computation serves as the fundamental philosophy behind adiabatic logic. In traditional digital circuits, the dissipation of energy through resistive components like transistors results in significant power losses. Adiabatic logic, on the other hand, minimizes these losses is recovered or reused. This novel approach leverages energy conservation by employing specialized clocking schemes, clever energy storage mechanisms, and innovative circuit topologies. Adiabatic logic offers a compelling solution to the challenges of power dissipation, making it an attractive candidate for energy-efficient computing in various applications. Investigating and using adiabatic logic in digital circuit design has the potential to significantly impact the electronics industry and bring about improvements in sustainability as technology keeps getting better.

2.2. The Charging Process in Adiabatic Logic

The primary focus in classic CMOS circuits is the dissipation of power, which is mostly caused by the dynamic switching of electrical devices. The approach involves using an adiabatic

switching technique, as depicted in Fig. 2.1(a), to condense the circuit's energy dissipation by substituting a time-varying supply of PCK for a direct current power source. There are defining characteristics of the setup circuits. PCK stands for the input voltage that changes over time, and N is an NMOS transistor used as a switch that takes input V_{in}. Where, C is the symbol for the load capacitor. In response to a boost in input voltage, the NMOS transistor becomes conductive, allowing the power source to charge the load capacitance. Notably, this specific configuration allows for the depiction of both transistors, with the ON state resistance being denoted as R_{ON}. Figure 2.1(b) illustrates the RC equivalent representation of Fig.2.1(a).

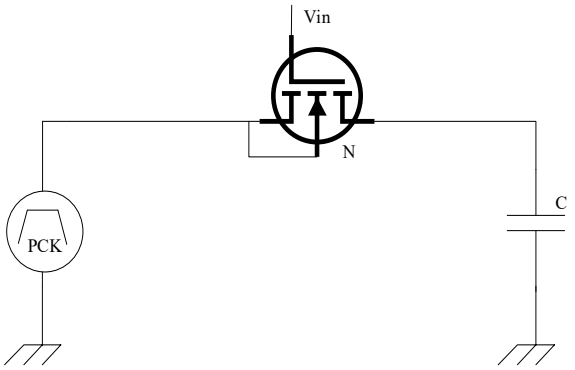

Fig. 2.1 (a): Adiabatic Switching Technique.

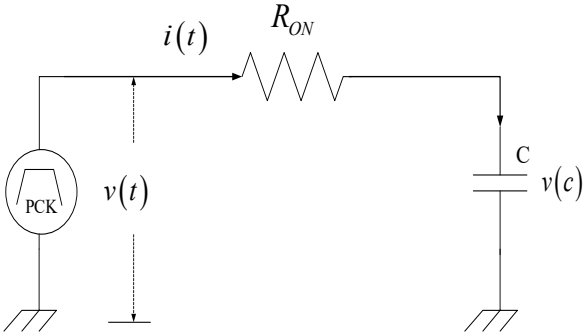

Fig. 2.1 (b): RC equivalent representation

.

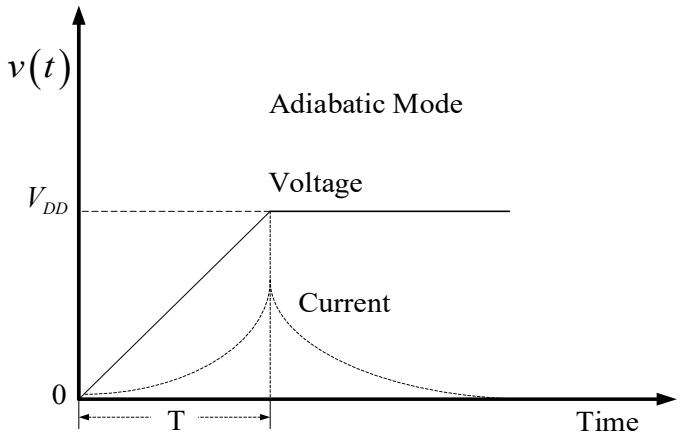

Fig. 2.1 (c): Input voltage and current vs. time.

The adiabatic mode, which differs from static CMOS, utilizes a time-varying voltage $v(t)$ and a power supply source capable of assuming sinusoidal, triangle, ramp, or trapezoidal waveforms. Minimizing the circuit's total energy usage was the chosen strategic objective. Input

voltage $v(t)$, current $i(t)$, and time period T are graphically shown in Fig. 2.1(c). To measure the energy loss that happens when a capacitor is charged adiabatically, one uses the circuit depicted in Fig. 2.1(b), which is termed the corresponding design of the adiabatic gate. In this specific context, the ON resistance of a transistor is represented by the symbol R_{ON}. To simplify the calculation, let's replace R_{ON} with R in the charging path resistance. The voltage is gradually increased from 0 to V_{DD} during a time period T (Fig. 2.1(c)). The voltage over the capacitor $v_C(t)$ and the instantaneous input signal $v(t)$closely match because the voltage-rising mechanism is progressive. Therefore, it follows that $v(t)$ is a good approximation for the function $v_C(t)$. Hence, employing the subsequent approach facilitates the computation of the electric current traversing the circuit.

$$v_C(t) \approx v(t) \tag{2.1}$$

$$i(t) = C\left(\frac{dv(t)}{dt}\right) = \frac{CV_{DD}}{T} \tag{2.2}$$

Evaluating the power $p(t)$ at the moment of transition T results in the energy of the charging event.

$$E = \int_0^T p(t)dt = \int_0^T v(t).i(t)\,dt = \int_0^T \left(v_R(t) + v_C(t)\right).i(t)\,dt \tag{2.3}$$

Since no energy is lost in the capacitance during the course of a single clock cycle, zero will be the integral of $v_C(t).i(t)$. Therefore, replacing $v_R(t) = i(t).R$ in (2.3) and substituting $i(t)$ value of (2.2) to (2.3) yields,

$$E = \int_0^T R\left(\frac{C^2V_{DD}^2}{T^2}\right)dt = \left(\frac{RC}{T}\right)CV_{DD}^2 \tag{2.4}$$

It is possible to calculate the overall energy loss in adiabatic logic (AL) by assuming that the amount of energy dissipated during recovery is identical as

$$E_{AL} = 2\left(\frac{RC}{T}\right)V_{DD}^2 \tag{2.5}$$

In contrast, a static CMOS inverter circuit's dissipated energy is shown as,

$$E_{CMOS} = \alpha \frac{1}{2} C V_{DD}^2 \tag{2.6}$$

By analysing (2.5), we see that the operational speed affects the energy loss. A circuit's energy dissipation drops in tandem with the rate at which it works. Adiabatic logic has the potential to significantly reduce energy usage through tactics like adjusting the supply voltage or limiting capacitive loads. The physical dimensions of the switch transistor are also an important factor in adiabatic logic, since the energy consumption equation incorporates the resistance component (R) in comparison to static CMOS. By utilizing Eqs. (2.5) and (2.6), one can determine the threshold value of T at which adiabatic circuits outperform static CMOS circuits in terms of efficiency. More precisely, the requirement $T > 4\frac{RC}{\alpha}$ must be satisfied for this to occur. Adiabatic logic is well-suited to scenarios with moderate to high activity factors, as seen by the activity factor α in equation $T > 4\frac{RC}{\alpha}$. To thoroughly evaluate the loss of energy in static CMOS and adiabatic logic, it is vital to introduce the Energy Saving Factor (ESF). To quantify the additional energy use of a static CMOS gate or device in comparison with the adiabatic logic counterpart, the ESF is used. What follows is the formulation of an ESF definition that has gained widespread acceptance:

$$ESF = \frac{\sum_{CMOS} E}{\sum_{AL} E} \tag{2.7}$$

Equation (2.7) shows that for a given logic architecture, the total energy consumption while utilizing the static CMOS design approach is in the numerator, and when using the adiabatic switching methodology, it is in the denominator. When utilizing the Energy Scaling Factor (ESF), it is crucial to gather all relevant energy dissipation fractions for analysis, regardless of whether the comparison is at the gate-level or the system-level.

2.3. Adiabatic logic families

Numerous methodologies for adiabatic logic have been devised over the course of time. The complexity of circuit designs has exhibited a notable escalation throughout time, including considerations such as the quantity of clock operations, the utilization of single or dual rails, and the existence or nonexistence of charging and discharging channels. The completely adiabatic method and the quasi-adiabatic method are two separate types of adiabatic logic operations. The

goal of completely adiabatic logic circuits is to achieve behavior that is as close as possible to perfect adiabaticity, meaning that no energy is lost as heat during transitions. To achieve the lowest possible energy usage, these circuits employ adiabatic charging and discharging procedures. The emphasis is on maximizing energy efficiency, even if it means sacrificing some speed or performance. Fully adiabatic logic is typically suited for applications where power efficiency is critical, but it may come at the cost of slower operation. It is also known as standard adiabatic logic, which focuses on minimizing energy dissipation during logic state transitions but may not achieve ideal adiabatic behavior. It often involves using complementary adiabatic switching techniques where logic gates are designed to minimize power consumption. These circuits are somewhat more practical. Quasi-adiabatic logic circuits primarily aim to approach adiabatic operation as closely as possible, while maintaining practicality. They strive for high energy efficiency while recognizing that ideal adiabatic behavior may be challenging to achieve in real-world applications. Quasi-adiabatic logic often involves advanced charging and discharging techniques to reduce energy loss during transitions. Sometimes it is also referred to as partially adiabatic logic, in which the logic circuits combine adiabatic and non-adiabatic (conventional) techniques. They offer flexibility by transitioning between low-power states (adiabatic) and high-power states (non-adiabatic) as needed based on the specific requirements of a task. Partially adiabatic logic can provide a balance between power efficiency and speed, making it suitable for various applications. There have been numerous proposals over the years for new families of adiabatic or quasi-adiabatic logic. Some popular methods for designing adiabatic logic are listed below, in chronological order. The following chapter of this thesis discusses the other well-known quasi-adiabatic logic design approaches.

2.3.1. Hot Clock NMOS

Referring specifically to NMOS technology, the phrase "Hot Clock NMOS" (Seitz et al., 1985) describes a unique approach to digital circuitry design. In order to adapt the clock signal's frequency and phase to the circuit's operating needs, the "Hot Clock NMOS" technology first suggested the idea of dynamic clocking. When compared to static clocking, dynamic clocking enhances clock signals to make them more effective. Dynamic clocking systems have reduced clock skew, which is the delay in occurrence of clock signals in different parts of a chip. Reducing clock skew is essential for ensuring the synchronized and reliable operation of circuits.

The "Hot Clock NMOS" method aims to increase circuit speed and performance by effectively regulating the clock signal, thereby enabling faster transistor switching. "Hot Clock" techniques, which seek to optimize clocking and control signals, have been implemented in an effort to decrease power consumption. Despite the fact that NMOS technology has historically been associated with higher power consumption, these strategies have been established to mitigate this difficult. The implementation of the dynamic synchronization technique significantly contributed to the improvement of system dependability by maintaining the stability of data signals during critical periods and meeting the required setup and hold time criteria. Briefly, the introduction of the "Hot Clock NMOS" concept has resulted in the development of dynamic synchronization techniques designed to enhance the act of digital circuits based on NMOS technology. By actively regulating clock signals and minimizing clock skew, this technique aimed to mitigate certain disadvantages of NMOS technology, such as its decreased operational speed and higher power consumption.

2.3.2. Recovered Energy Logic (REL)

Recovered Energy Logic (Hinman & Schlecht, 1993) is a methodology developed to improve energy efficiency in digital circuits. It focuses on conserving energy and minimizing power dissipation, primarily through the retrieval and application of heat dissipated during transistor switching.

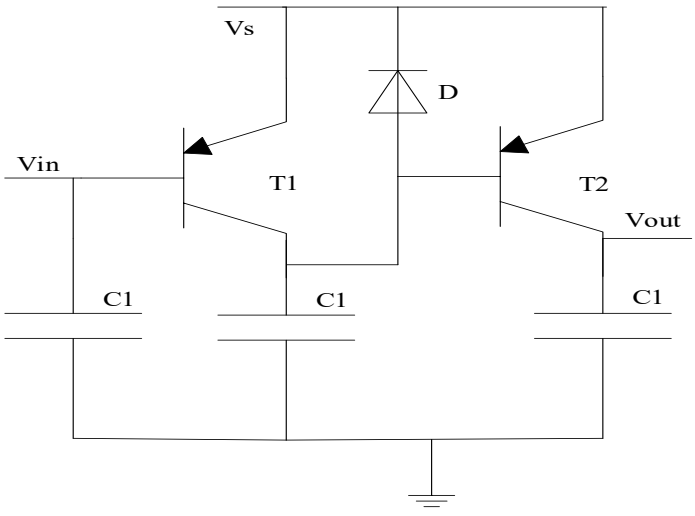

Fig.2.2: Recovered Energy Logic (REL) inverter

REL incorporates energy recycling and energy storage devices, reducing energy waste during logic operations. It is widely used in digital systems like microprocessors, memory devices, and integrated circuits. However, REL has trade-offs, including increased circuit complexity and potential impacts on operational speed. Despite these challenges, REL has the potential to enhance battery longevity, mitigate heat generation, and contribute to ecologically sustainable electronic systems. Fig.2.2 show the basic inverter schematic of a REL.

2.3.3. Split-level Charge Recovery Logic (SCRL)

SCRL exemplifies a legitimate adiabatic logic family by virtue of its integration of a feedback path that facilitates logical restoration (Younis & Knight, 1994; Younis, 1994).

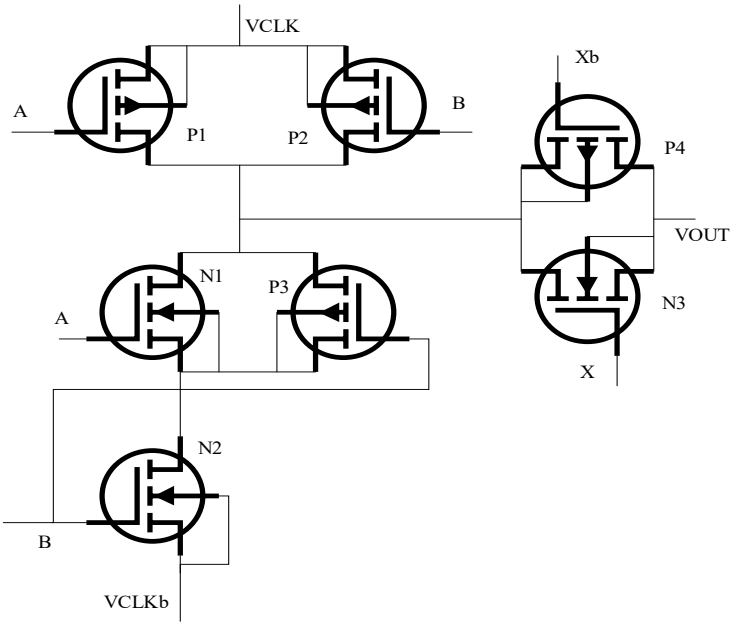

Fig.2.3: SCRL Invereter

Its structural configuration is reminiscent of static CMOS gates, augmented by a transmission gate. Notably, SCRL distinguishes itself by employing power-clock signals to replace both of its power rails, thereby earning its nomenclature as a "split-level" logic family. Furthermore, it features a complex clocking scheme, often characterized by the presence of eight distinct phases. Younis and Knight (1993) introduced the Charge Recovery Logic (CRL) family of adiabatic

logic, which this architecture serves as an extension of. The essential inverter circuit of SCRL is illustrated in Fig. 2.3.

2.3.4. 2N-2N2D

A subset of the complementary logic family known as the 2N-2N2D arrangement uses diode technology (Kramer et al., 1994). The presence of diodes in this particular design results in the occurrence of non-adiabatic losses, hence establishing it as primarily a quasi-adiabatic system. The nomenclature utilized for this specific logic family indicates the usage of paired NMOS devices, represented by the symbol "2N," in combination with dual diodes indicated by "2D." Figure 2.4 clearly illustrates the fundamental inverter setup within the 2N-2N2D framework.

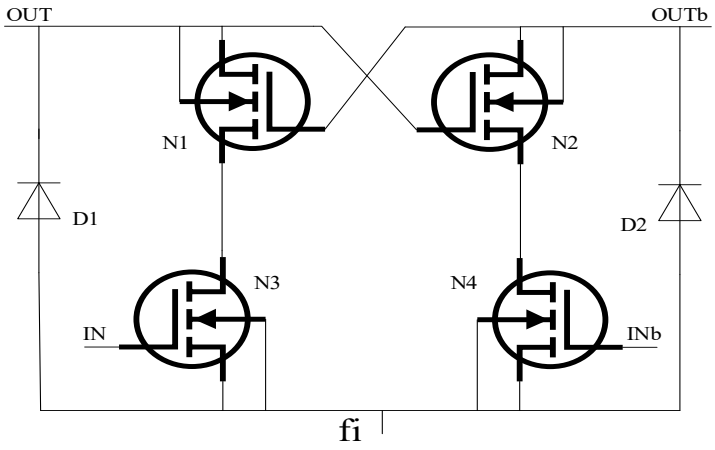

Fig.2.4: 2N-2N2D Inverter.

2.3.5. Adiabatic Dynamic Logic (ADL)

ADL is a concept that combines adiabatic principles with traditional CMOS dynamic logic (Dickinson & Denker, 1994). The ADL gates possess attributes like as simplicity, adaptability, ease of cascading, and compatibility with common CMOS fabrication techniques. The ADL phases are constructed by utilizing both NMOS and PMOS devices in an alternating manner, similar to the 2N-2N2D technique. The recovery process is helped by the inclusion of diodes, which leads to a quasi-adiabatic behaviour. Concurrently, the reduced field strengths that are inherent in adiabatic operation may have prospects for optimizing the design of Field-Effect Transistor (FET) devices.

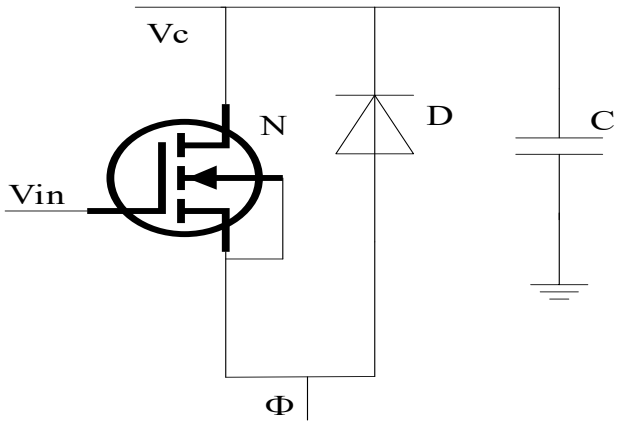

Fig.2.5: ADL Inverter.

2.3.6. 2N-2N2P

According to (Denker, 1994: Kramer et al., 1995), the 2N-2N2P adiabatic logic family was created as an alternative to ECRL with the main objective of mitigating the unfavorable coupling impact. A schematic depiction of this family of logic at a high level is depicted in Fig. 2.6. Crucially, 2N-2N2P employs cross-coupled PMOS switches, resulting in non-floating outputs over a considerable portion of the recovery period.

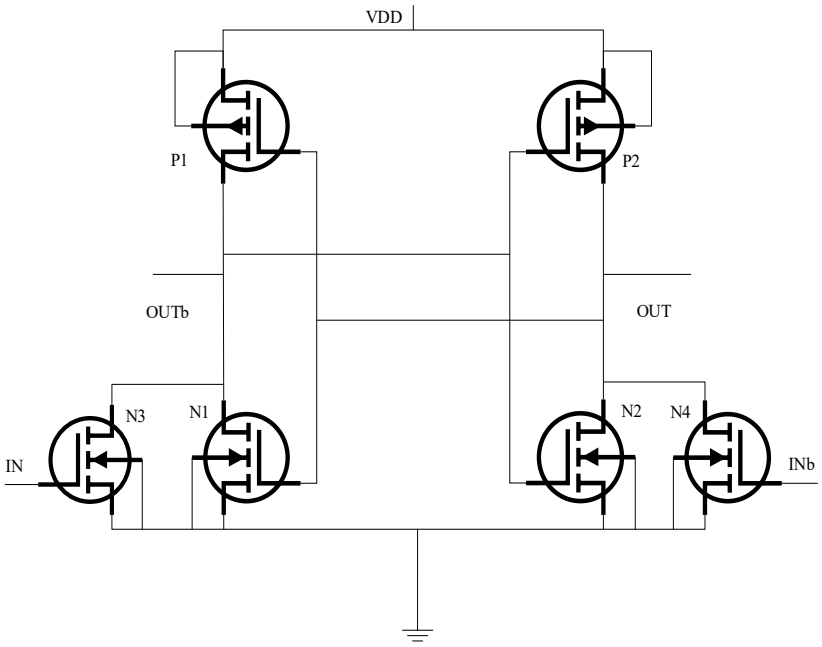

Fig.2.6: 2N-2N2P Inverter

While it does not use as much power as standard CMOS logic, you should be aware that the load generated by the output charge will not be completely recovered since the amount of energy dissipated is inversely related to the capacitor that comprises the load.

2.3.7. Efficient Charge Recovery Logic (ECRL)

ECRL was consistently called "2N-2P" by Kramer et al. (1995) and was considered an independent discovery (Moon & Jeong, 1995; Moon & Jeong, 1996). Heller et al. (1984) states that the Differential Cascode Voltage Switch Logic (DCVSL) family of conventional CMOS is the mother of both ECRL and 2N-2P. A "2N," or pair of pull-down NMOS devices, is used to determine the operation of this system, while a "2P," or cross-coupled PMOS device pair, is used to maintain the states. Many related families of adiabatic logic can trace their roots back to this framework, making it an extremely influential piece of literature. This logic style is considered quasi-adiabatic because it is unable to fully restore the power clock with only PMOS devices. In the next chapter, ECRL/2N-2P is discussed in further depth.

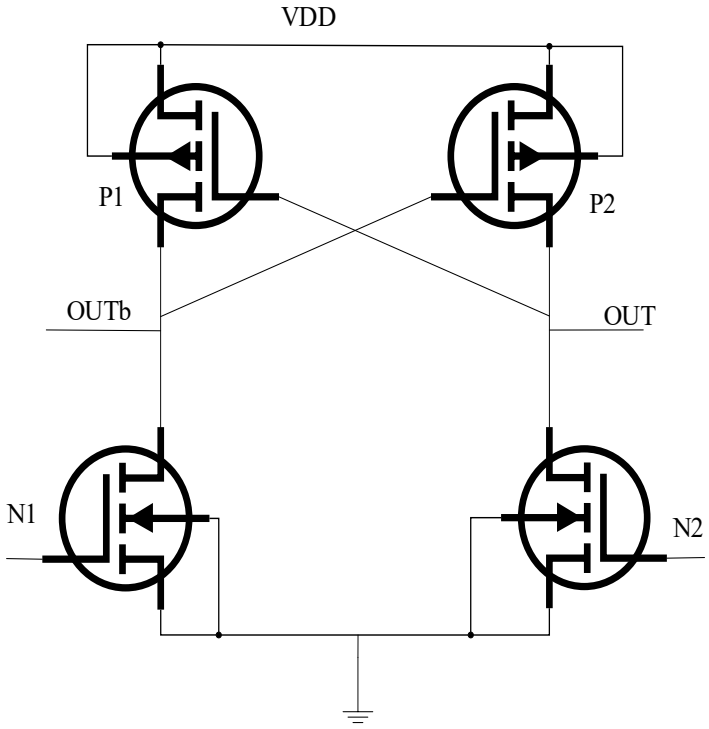

Fig.2.7: ECRL Inverter.

2.3.8. Adiabatic pseudo-domino logic (APDL)

Wang and Lau (1995) proposed APDL, which combines adiabatic theory with CMOS domino logic concepts. When contrasted to other adiabatic logic configurations, APDL circuits has a number of benefits, such as being smaller, easier to cascade, and having more stable outputs. For basic gates, the dimensions of APDL gates are on par with traditional static CMOS gates, while significantly reduced dimensions are observed for intricate logic structures. The inherent stability of the output signals in APDL eases the process of cascading logic stages and enables the convenient construction of complex logical functions. Furthermore, through simulation, it has been demonstrated that APDL circuits can attain operating frequencies of up to 200 MHz while maintaining acceptable power dissipation levels (Wang & Lau, 1995).

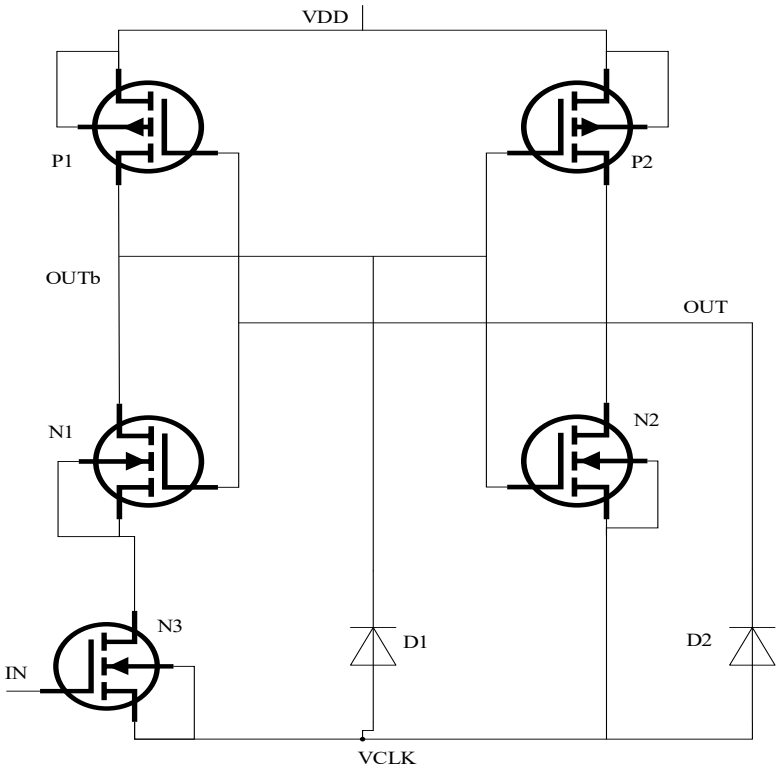

Fig.2.8: Adiabatic pseudo-domino logic (APDL)

2.3.9. Clocked CMOS Adiabatic Logic (CAL)

Similar to the 2N-2N2P logic design, timed CMOS Adiabatic Logic (CAL) has timed NMOS components, which are placed within the NMOS decision structure and the output stage (Maksimovic & Oklobdzija, 1995). The assessment of logic may be more easily accessed and

fewer clock phases are needed when using these NMOS components, which are actuated by a square-wave clock signal. This approach does, however, need the inclusion of supplementary control signals. Figure 1 depicts a schematic of the inverter, a key component of CAL schematic. The memory functionality of this inverter is achieved by using transistors N1, N2, and cross-coupled CMOS inverters P1, P2, and P2. It is often possible to evaluate any binary function by substituting NMOS logic trees for NMOS devices N5 and N6, which handle the switching procedures.

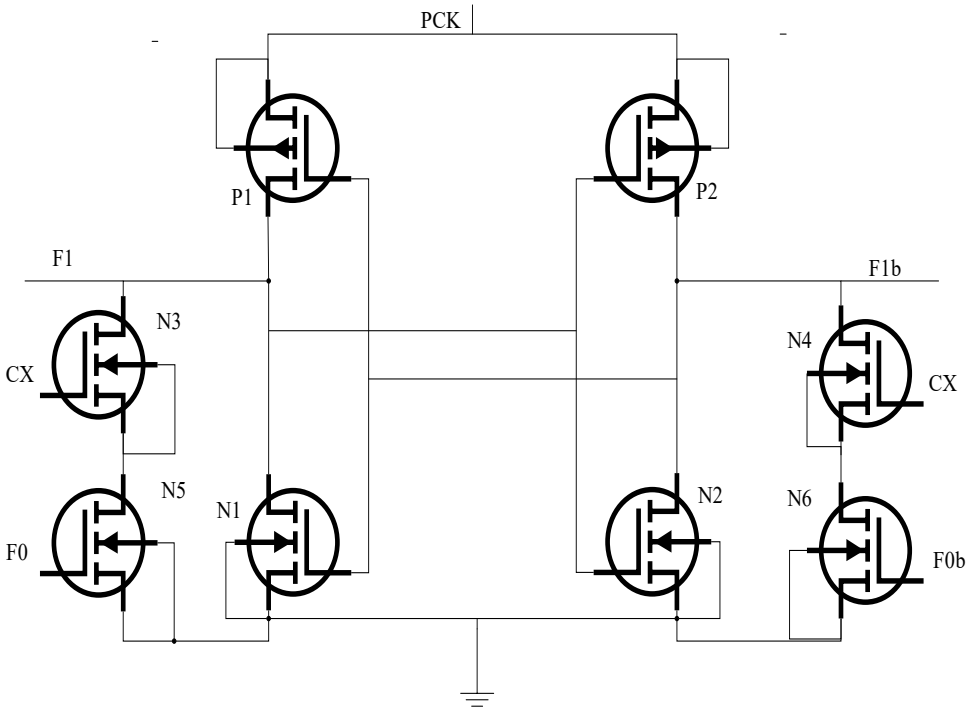

Fig.2.9: CAL Inverter.

2.3.10. Positive Feedback Adiabatic Logic (PFAL)

Vetuli et al. (1996) presented PFAL, which uses an assessment tree interposed over the power clock and execution nodes. In order to execute a complete adiabatic procedure, a recovery channel is necessary. Following this, Liu and Lau (1998) renamed it PAL-2N. With its two n-trees, PFAL logic can perform logical operations and provide positive and negative outputs. ECRL utilizes a single pair of PMOS transistors in its latch, while PFAL uses a combination of two PMOS and two NMOS transistors. In addition, the PFAL functional blocks work in tandem with the transmission PMOS to lower the associated resistance while the capacitor is being

charged. In Fig. 2.10, we can see a simple PFAL circuit diagram for the inverter. By reducing the amount of energy provided, capacitance under load returns it to the power source during the period of recovery.

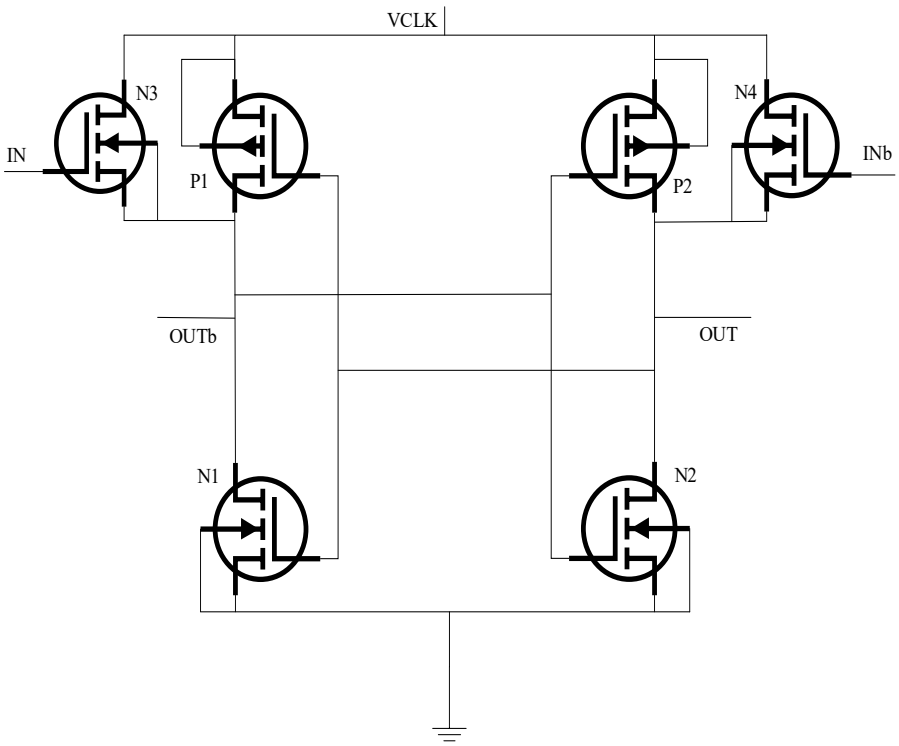

Fig.2.10: PFAL Inverter

2.3.11. Energy Efficient Logic (EEL)

As an postponement of the ECRL, Yeh et al. (1997) presented the Energy Efficient Logic (EEL). The EEL-proposed approach comprises connecting the power clock and output nodes with externally controlled pulsed NMOS devices. With this method, we want to make complete charge restoration easier. But remember that EEL can't achieve true adiabatic behavior, mainly due to its intrinsic lack of logical reversibility. N1 and N2 are NMOS transistors that are integrated into the EEL circuit along the route that links the output node to the CK (Clock) supply, in contrast to the ECRL design. N1 and N2 are activated when the PULSE signal is in its upper range.

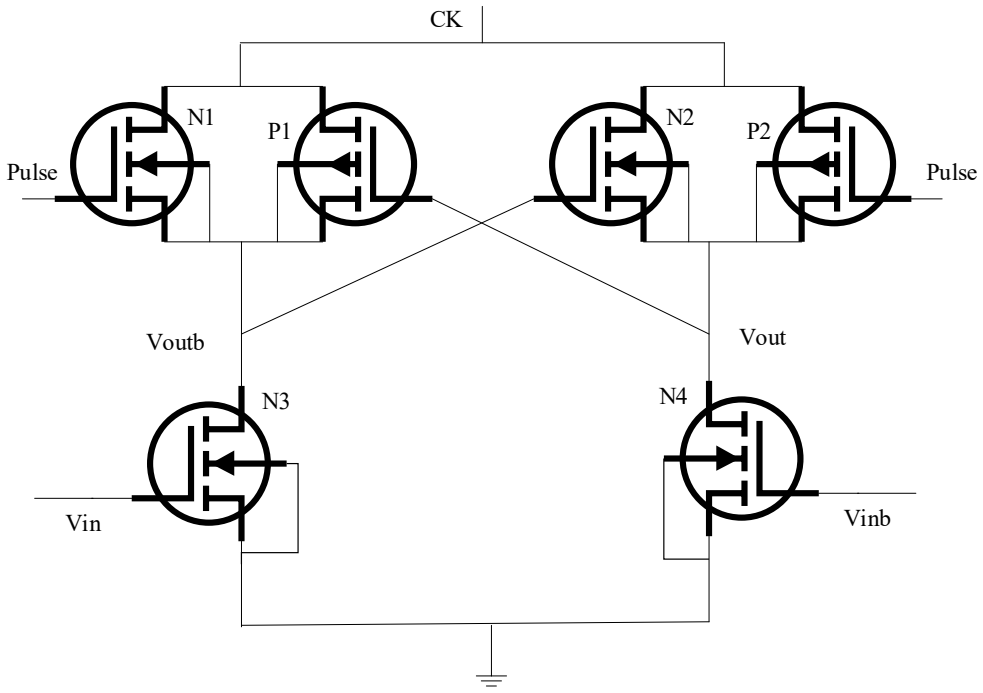

Fig.2.11: Energy Efficient Logic (EEL)

Which is why, while we wait, N1 and N2 effectively dissipate any residual charge at the output node that the PMOS device is unable to discharge correctly to the CK supply. Because of this setup, the circuit's output voltage may reach its full swing at the Vout. So, the EEL circuit gets a full-swing output. With this new design, the EEL circuit is able to return a larger amount of charge to the CK supply, which in turn improves the circuit's energy usage.

2.3.12. Pass-transistor Adiabatic Logic (PAL)

PAL has a related basic layout to a PFAL gate; however, it differs in that it does not include any cross-coupled NMOS components. There is a built-in shortcoming in creating an effective ground connection since this logic family does not have pull-down NMOS transistors. A two-phase power clock and very simple gates define PAL, a model of dual-rail adiabatic logic (Oklobdzija et al., 1997). P1 and P2 are the cross-coupled PMOS latches that make up a PAL gate, which also includes genuine and complementary pass-transistor NMOS functional components. The schematic representation of the construction of an AND-OR gate, namely Q=A.B+C, is shown in Fig. 2.12, which depicts this structural configuration.

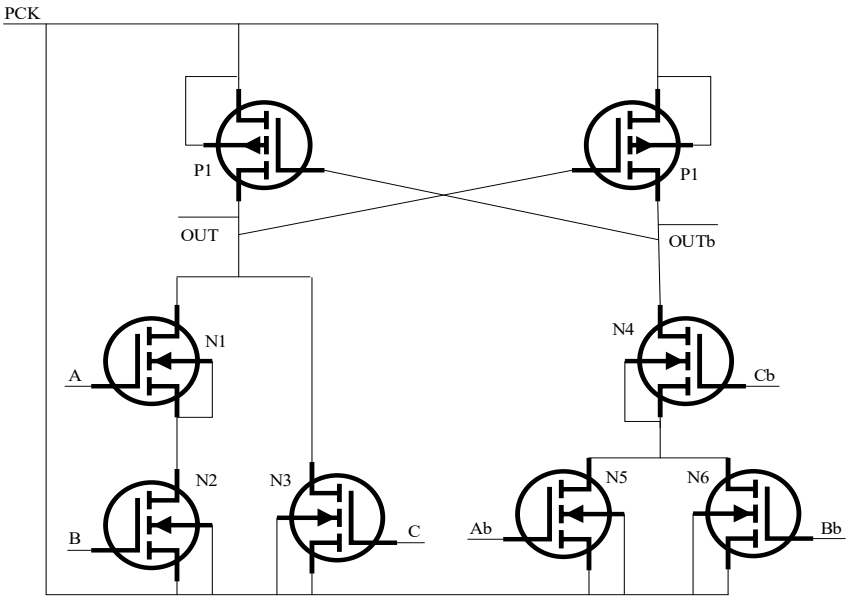

Fig. 2.12: Implementation of Q=A.B+C in PAL

2.3.13. Improved Adiabatic Pseudo-Domino Logic (IAPDL)

Despite retaining a simplified clocking mechanism, the IAPDL has exceptional performance at high frequencies, exceeding the 1 GHz barrier. On the other hand, previous studies have shown that traditional APDLs dissipate almost twice as much power and have an optimal operating frequency of 100 MHz (Lau & Liu, 1997).

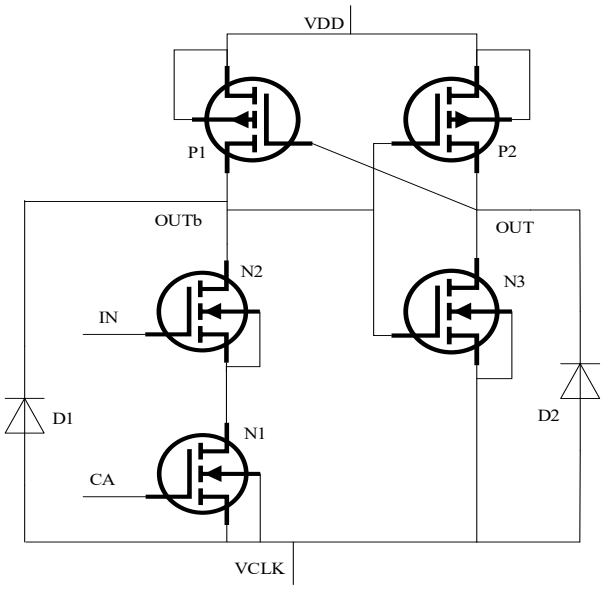

Fig.2.13: IAPDL Buffer

IAPDL exhibits a more streamlined configuration when compared to T-APDL (Transmission Gate-Interfaced APDL), and its power consumption is consistently lower than that of APDL. the output nodes from fluctuations at the input node during the hold phase is the job of an NMOS transistor N1 inside the APDL design. Because N1 relies on the OUT signal in the APDL structure, its operating speed is limited.

2.3.14. Improved Efficient Charge Recovery Logic (IECRL)

With regard to optimizing power consumption, the IECRL (Liu & Lau, 1998) performs better than both ECRL and EEL.

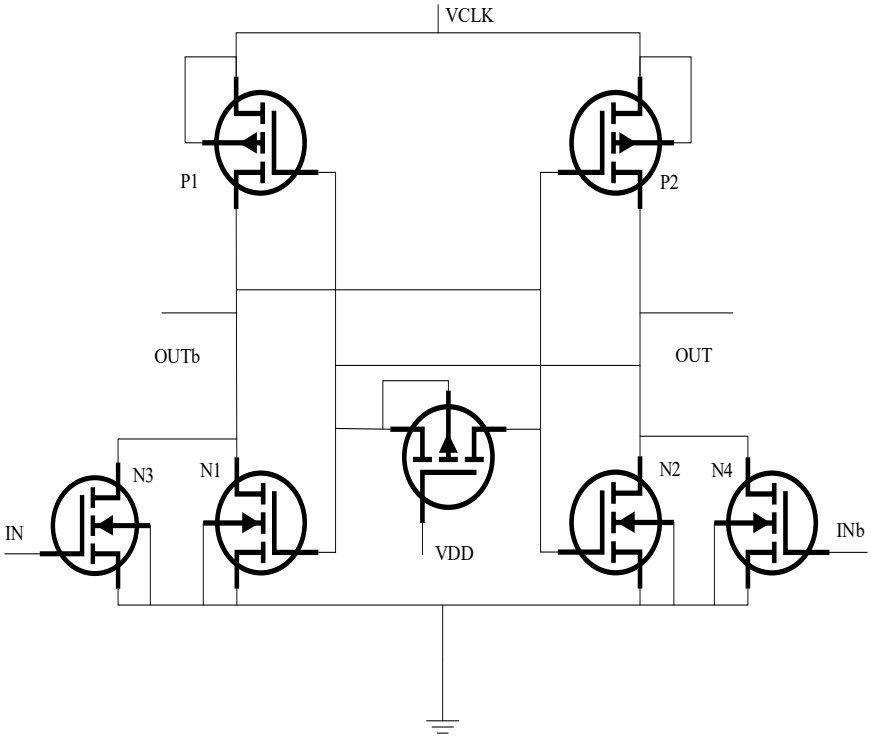

Fig.2.14: IECRL Inverter.

Figure 2.14 shows an architectural concept that enables efficient use of energy recovery by using a PMOS P3 transistor to establish two cooperating junction diodes. During the recovery phase of an IECRL circuit, two pulldown transistors, N1 and N2, are used to lessen the negative voltage drop. In general, energy efficiency is improved as a result of this engineering strategy's decrease in power losses.

2.3.15. Reversible Energy Recovery Logic (RERL)

In a logic framework outlined by Lim et al. (1998) as "Reversible Energy Recovery Logic (RERL)," two NMOS devices that are mutually connected keep the logic state intact. Nevertheless, a sophisticated eight-phase synchronization mechanism is required to coordinate RERL's assessment and recovery operations using transmission gates, much like the SCRL approach. RERL stands out because it does not experience any non-adiabatic energy losses; instead, it only experiences adiabatic loss of energy and leakage current losses. RERL is an eight-phase synchronized architecture that uses reversible logic in a dual-rail adiabatic circuit. Relative to other modern adiabatic logic circuits and traditional static CMOS circuits, simulation-based empirical research shows that RERL consumes much less power when operating at slower rates.

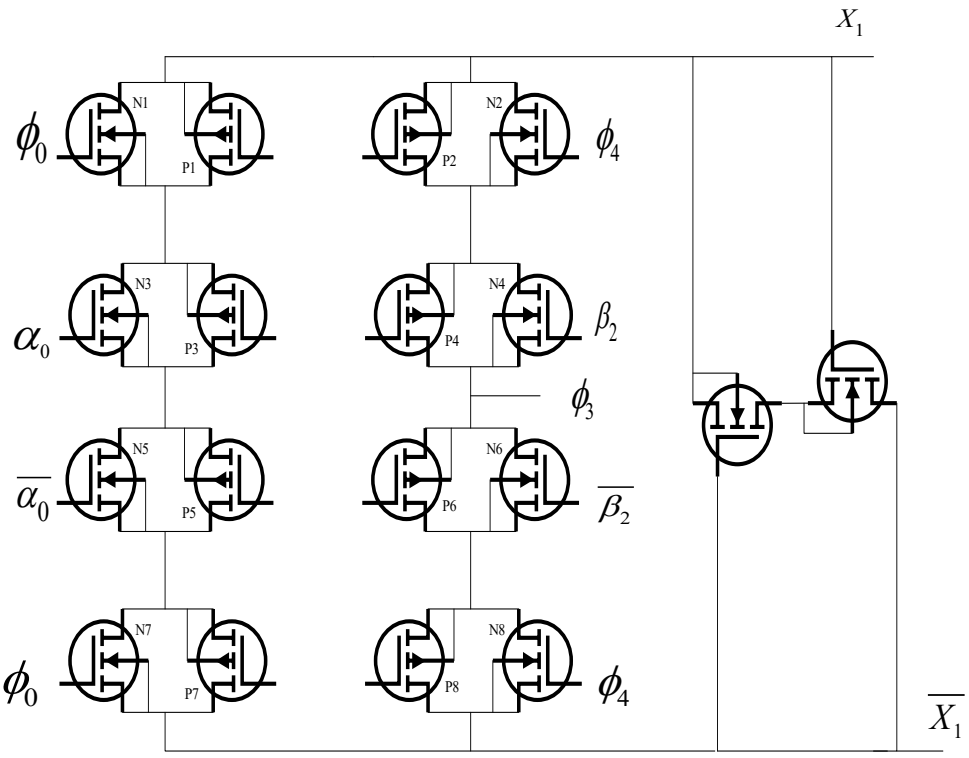

Fig.2.15: RERL Inverter.

2.3.16. True Single-Phase Energy Recovery Logic (TSEL)

Some partial adiabatic circuit families include TSEL (Kim & Papaefthymiou, 1998), 2N-2N2P, and CAL. To power the TSEL gates, a single-phase sinusoidal power clock is used. In

TSEL designs, the cascades use NMOS and PMOS gates that alternate with one another. An NP-domino type of cascading TSEL gates is made possible by using two DC reference voltages. When compared to similar adder circuits in other logic types and operating in low supply voltage situations, TSEL shows better energy efficiency across a broad range of frequencies. This efficacy is particularly noticeable for clock frequencies between 10 MHz and 200 MHz. One unique aspect of TSEL technology is that it is the first family of energy-recovering logic gates that only operate under a single-phase sinusoidal clocking paradigm. No matter what computations are running, TSEL's dual-rail structure ensures that the clock generator is always presented with an equal load.

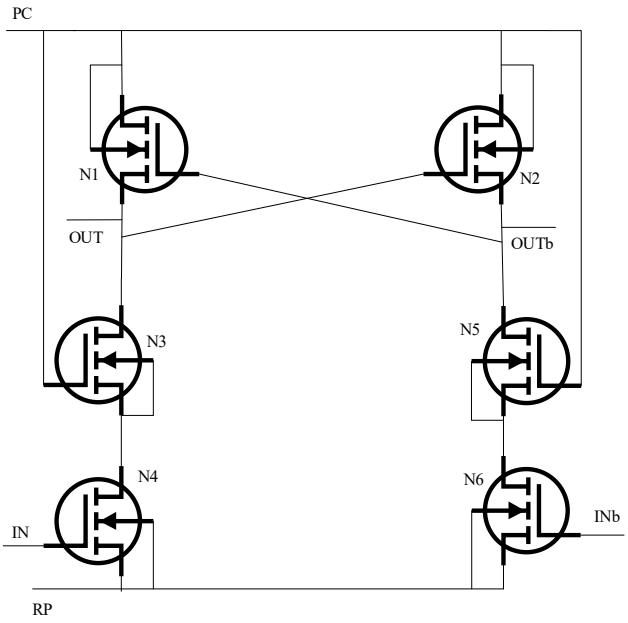

Fig.2.16: TSEL NMOS Inverter

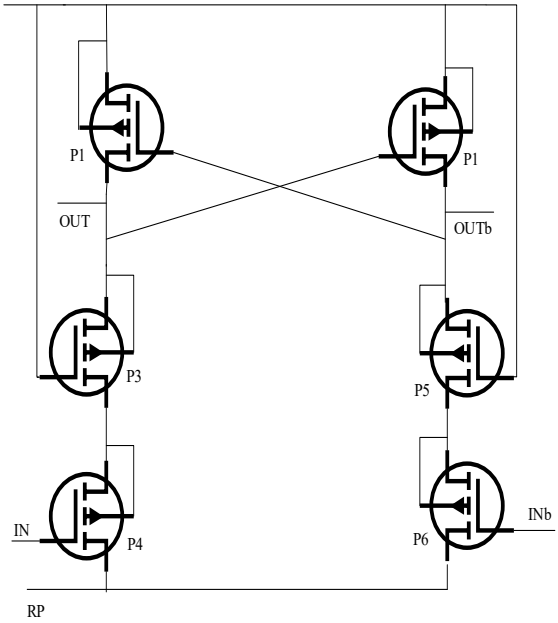

Fig.2.17: TSEL PMOS Inverter

2.3.17. Source Coupled Adiabatic Logic (SCAL)

A family of dynamic logics exhibiting partial adiabatic properties was proposed by Kim and Papaefthymiou (1999) and is known as Source Coupled Adiabatic Logic (SCAL). SCAL keeps all the good things about TSEL, such as being able to use a single-phase power clock. As an added bonus, it uses independently adjustable current sources at each gate to provide improved energy efficiency across a broad range of operating frequencies. With a variable current source to control the charge flow rate into or out of each gate, SCAL improves the effectiveness of its energy usage. Several problems with multi-power-clock methods may be

reduced by using adiabatic circuits. These include higher energy dissipation, clock skew concerns, and the need for several power-clock sources. The construction of SCAL NMOS and PMOS inverters is shown graphically in Figs. 2.18(a) and 2.18(b).

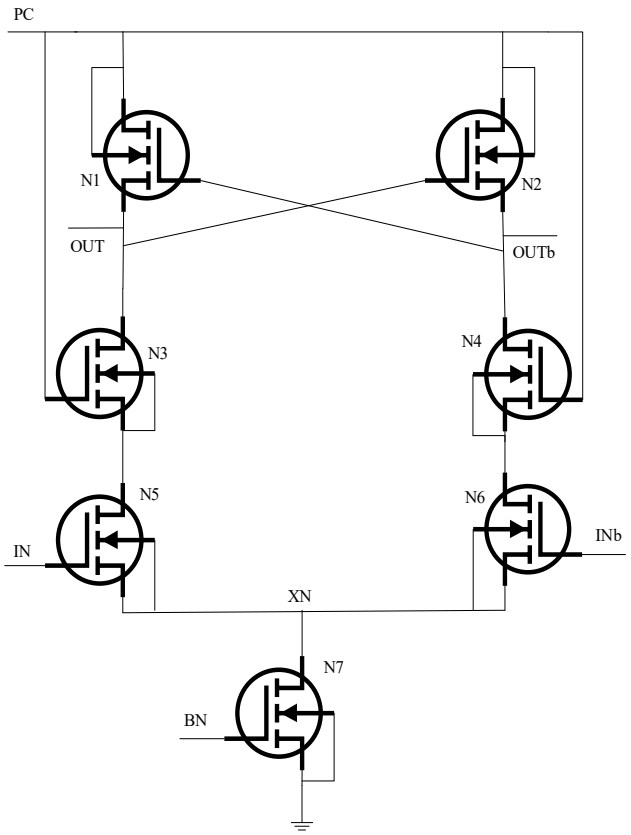

Fig.2.18(a): SCAL NMOS Inverter

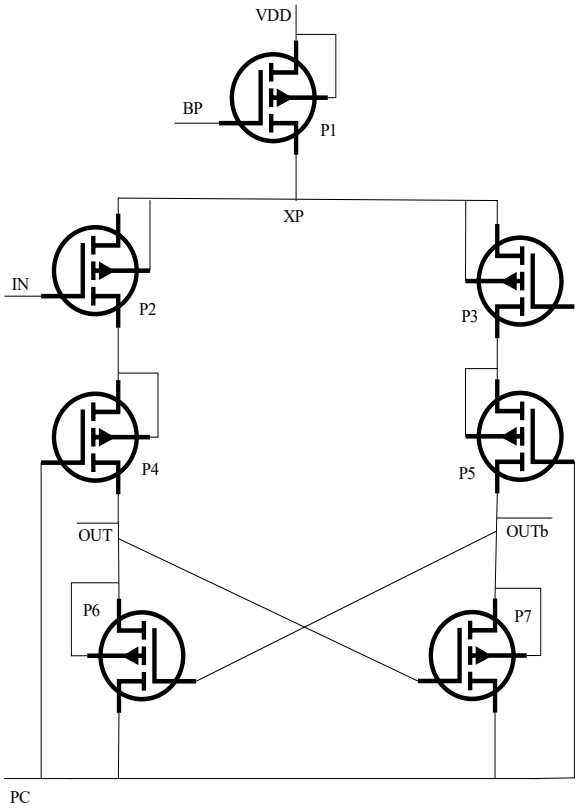

Fig.2.18(b): SCAL PMOS Inverter

2.3.18. NMOS Energy Recovery Logic (NERL)

The NERL is a unique paradigm that uses just NMOS transistors and has a simpler six-phase-clocked power architecture (Kim & Yoo, 2000). In comparison to alternative fully adiabatic logic approaches, NERL exhibits diminished spatial requirements and reduced energy utilization. The integration of bootstrapped NMOS switches streamlines the architecture of NERL circuits. The empirical investigations, conducted on a full adder, substantiate the significant disparity in energy consumption favoring the NERL circuit when operating at low speeds, relative to other adiabatic logic circuits. NERL manifests superior suitability for applications characterized by an emphasis on energy conservation, as opposed to demanding high performance.

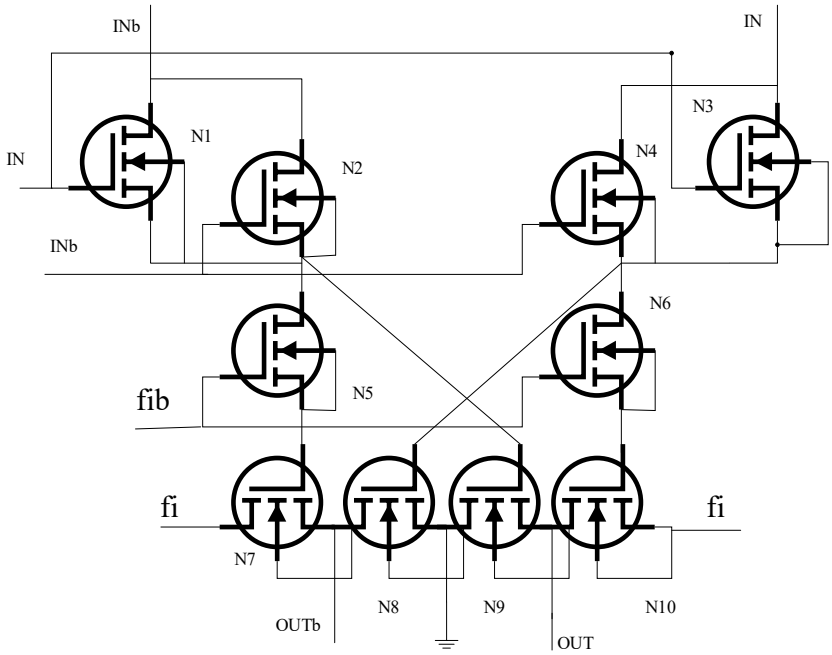

Fig.2.19: NERL Inverter

2.3.19. High-Efficient Energy Recovery Logic (HEERL)

According to Hongyu et al. (2001), the HEERL inverter buffer cascades power using a four-phase trapezoidal power clock.

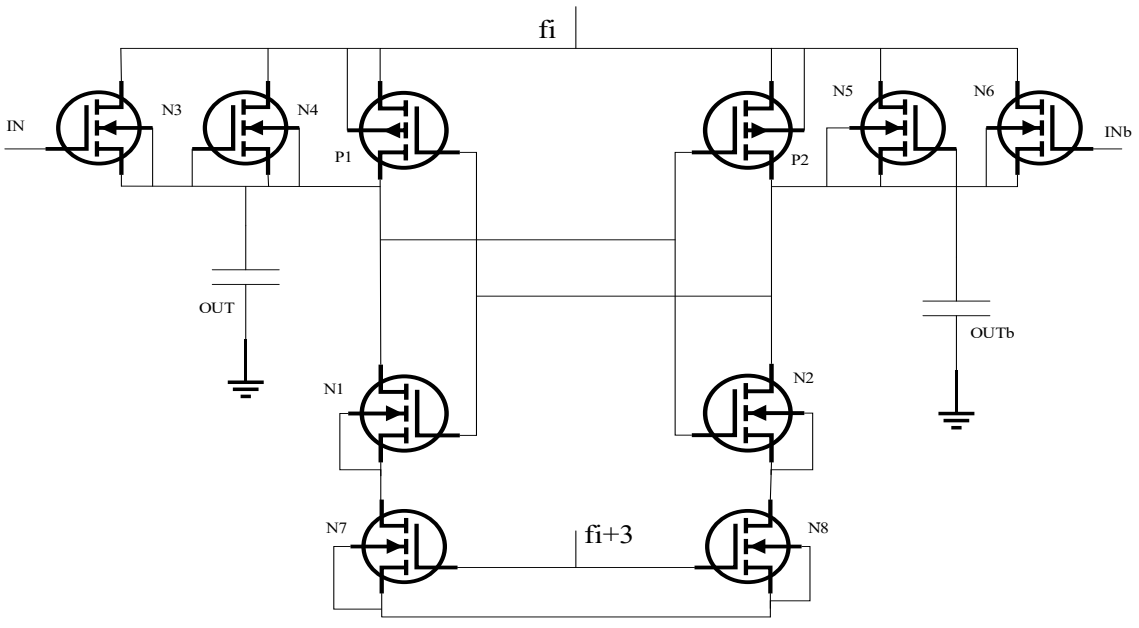

Fig.2.20: HEERL Inverter

It all begins with a legitimate input, which turns on N3 and turns off N6. N2 turns conductive as the input increases, clamping the OUTb-node to the ground. In this state, P1 is active, and NMOS and PMOS devices charge the OUT-node. When the output voltage drops beyond a recovery threshold, N4 is activated. Effective charge recovery and high energy recovery efficiency are made possible when the OUTb node drops below the voltage threshold level.

2.3.20. Improved Adiabatic Pseudo-Domino Logic 2 (IAPDL-2)

IAPDL-2 is defined and explained by Widjaja and Lau (2003). Like the traditional IAPDL, this structural base incorporates a trapezoidal power clock and significantly reduces the number of diodes. Under low supply voltage circumstances, this invention reduces device count, spatial footprint, and power loss. In Fig. 1, the basic IAPDL-2 inverter is shown in operation; this contrasts with the IAPDL, which uses two diodes to pre-charge the output node. An important feature of the clock signal is its trapezoidal waveform. One key difference between this clock signal and the standard IAPDL clock is the inclusion of a constant voltage stage between the pre-charge and evaluation stages. By strategically including this element, the design ensures a safe input voltage change and avoids non-adiabatic transitions within the circuit.

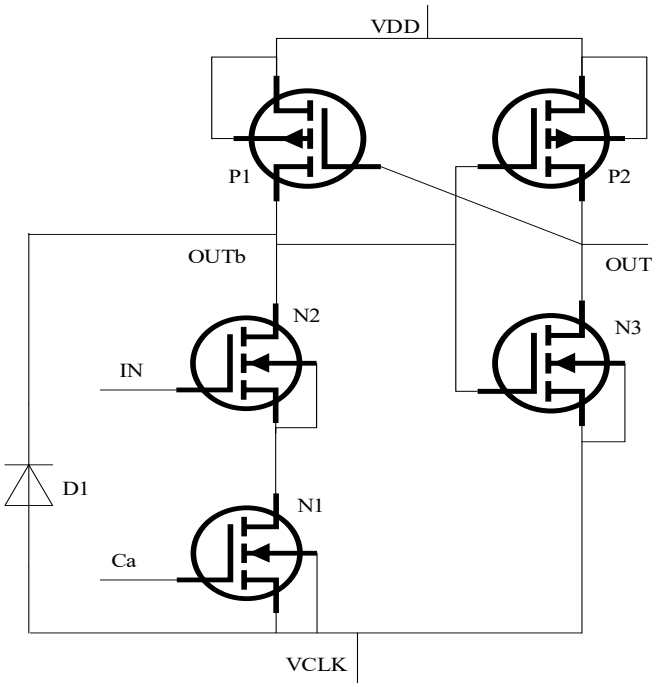

Fig.2.21: IAPDL-2 Inverter

2.3.21. Complementary Pass-Transistor Adiabatic Logic (CPAL)

The core element of CPAL, first proposed by Jianping et al. (2003), is a PFAL inverter or buffer. By connecting the gates of NMOS pull-ups to the pass-transistors, the primary framework of the evaluation tree is laid out. By using transmission gates for energy restoration and complementing pass-transistor logic for evaluation, CPAL circuitry is able to completely eliminate non-adiabatic energy loss in output loads, leading to more efficient transferred energy and recovery. In Fig. 2.22, we can see the CPAL inverter schematically shown.

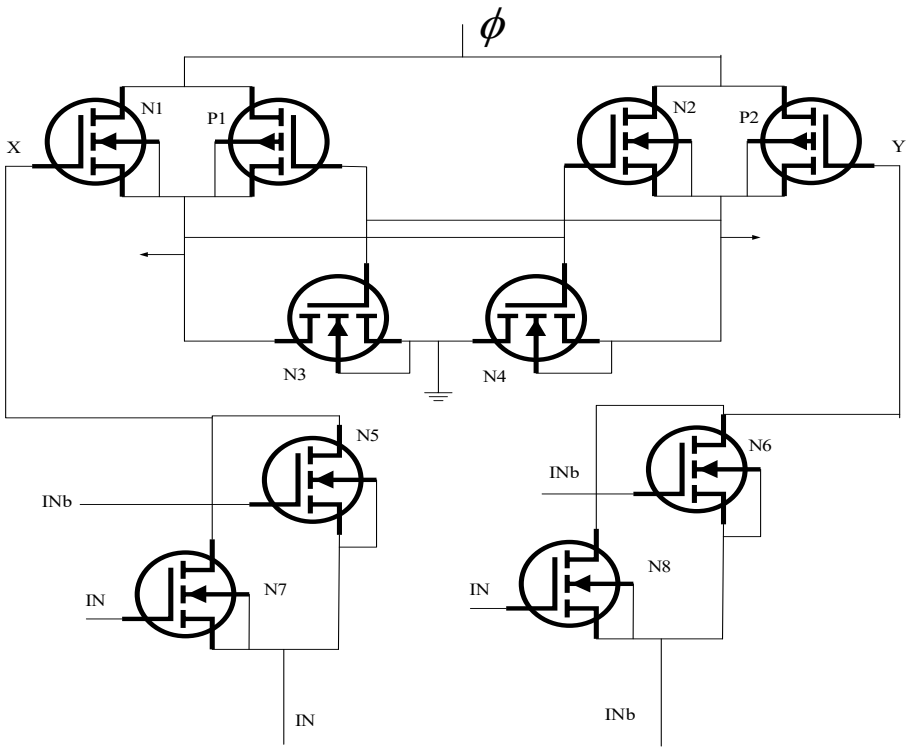

Fig.2.22: CPAL inverter

2.3.22. Dual Transmission Gate Adiabatic Logic (DTGAL)

The DTGAL topology described by Jianping et al. (2004) is shown in Fig. 2.23. Logical assessment and energy recovery circuits are the two mainstays of this setup. Transmission gates (Ni, P1) and (Nib, P2) make up the logic analysis circuit, while (N1, P1) and (N2, P2) are the transmission gates that make up the energy recovery circuit. By using N3 and N4, two cross-coupled transistors, the un-driven output node is properly grounded. By using feedback control methods that originate from the outputs of the following stages, DTGAL helps to reduce non-adiabatic energy usage on output loads.

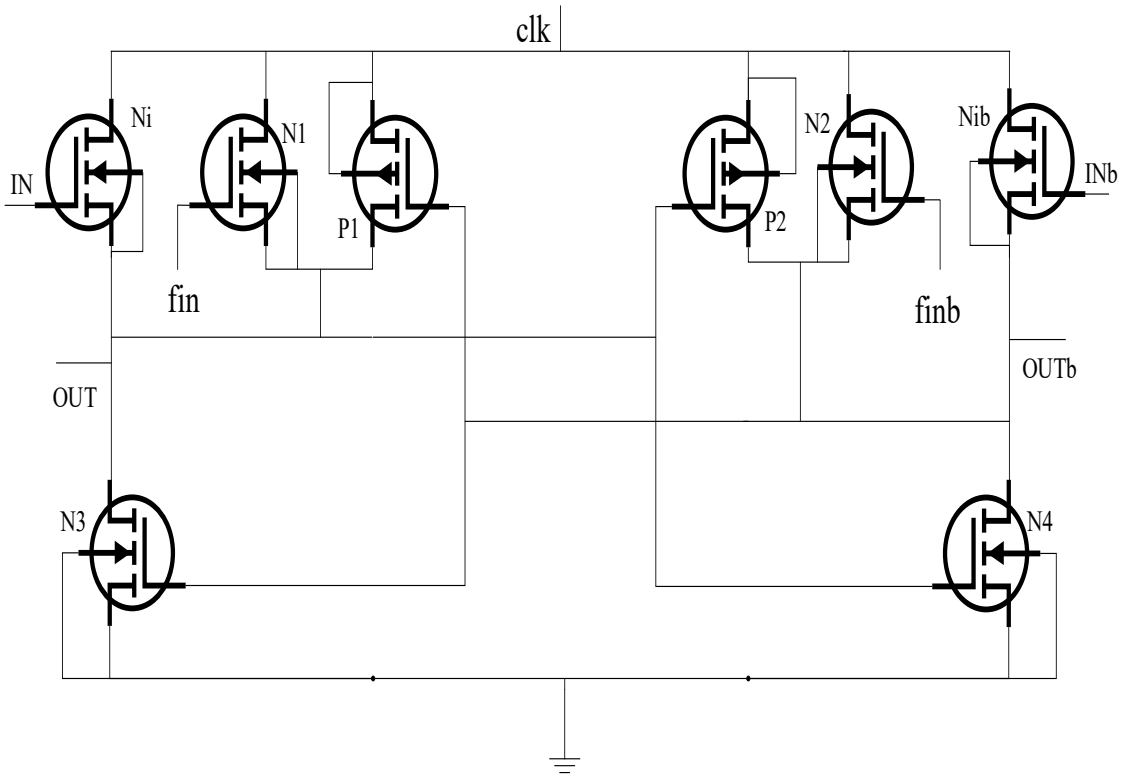

Fig.2.23: DTGAL Inverter

2.3.23. 2N-2N2P2D Logic

In 2006, He et al. presented a new family of quasi-static adiabatic logics called "2N-2N2P2D." This group of quasi-static logics offers significant improvements in power conservation over its forerunner, dynamic adiabatic logic. To do this, it improves compliance with standard CMOS circuits and gets rid of the repetitive charging and discharging of capacitive nodes. This one-of-a-kind quality reduces energy loss by eliminating unnecessary switching operations. In addition, the 2N-2N2P2D logic family is better than the APDL and CAL families since it is inherently simple and has a symmetric layout, which means that additional clock signals along with control signals are not needed. Figure 2.24 shows the 2N-2N2P2D inverter's basic architecture.

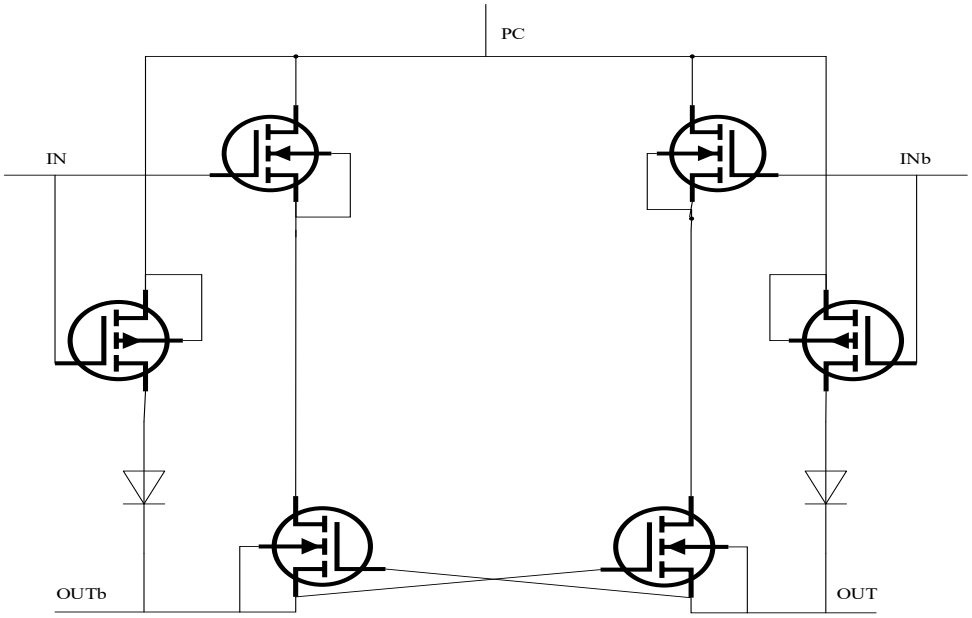

Fig.2.24: 2N-2N2P2D Inverter

2.3.24. Quasi-Static Single-phase Energy Recovery Logic (QSSERL)

To reduce power loss and simplify clock design, a novel logic paradigm called QSSERL (Li et al., 2007) employs an individual sinusoidal supply-clock. Its performance in terms of speed is equivalent to that of traditional two-phase energy recovery logic. Because of its quasi-static properties, QSSERL simplifies the design of clock networks for synchronous systems and gets rid of the requirement for auxiliary timing control clocks by reducing switching activity and power consumption.

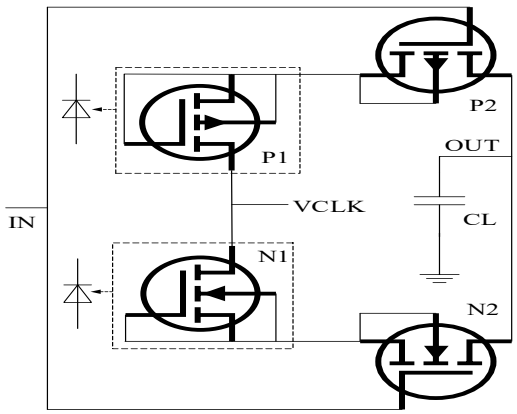

Fig.2.25: QSSERL Inverter

2.3.25. Clocked Transmission Gate Adiabatic Logic (CTGAL)

Figure 2.26 shows the CTGAL circuit, which was presented by Jian et al., (2007) and is a novel low-power adiabatic circuit which utilizes a two-phase power clock technique. Whereas VCLK is used as the clock-controlled clock in this setup, VCLK is the main power clock. It is noted VCLK, the clock-controlled clock, is half a period ahead of VCLK, the local power clock, or T/2. Thus, the clock-controlled clock may be replaced with an alternate power clock that complements the local power clock; this eliminates the need for extra clocks. In Fig. 2.26, we can see the CTGAL circuit shown symbolically.

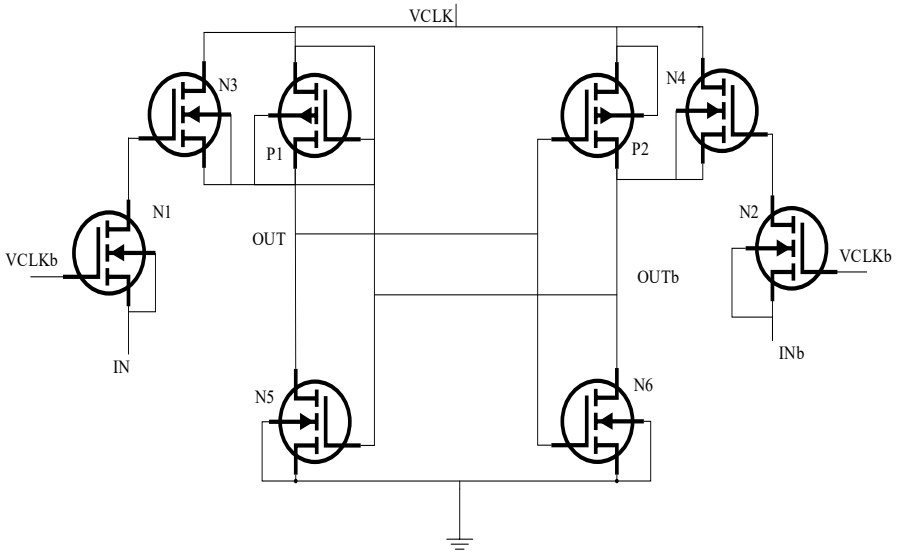

Fig. 2.26: CTGAL circuit

2.3.26. Glitch-Free and Cascadable Adiabatic Logic (GFCAL)

Figure 2.27 shows the fundamental layout of a GFCAL inverter, which is made up of two types of MOSFETs: one with a P-channel and one with an N-channel, connected in parallel (Reddy et al., 2008). Each of these parts is linked to the load in sequence. The charging and discharging paths in the GFCAL circuit are provided by diodes and a triangular power clock, as shown in Fig. 2.27. Triangle power clocks show less power waste than sinusoidal and split-level sinusoidal power clocks, which is an essential point to remember. However, there is a noticeable delay at the output node with the current power clock design. Furthermore, while current flows through diodes, voltage decreases across them, causing non-adiabatic losses. The output amplitude degradation that diode-based circuits are known to experience degrades the total

efficacy of GFCAL. One may argue that compared to other families of adiabatic logic, GFCAL circuits dissipate less power. More care must be taken while using these devices because of the significant delays and loss of amplitude they exhibit when producing their output.

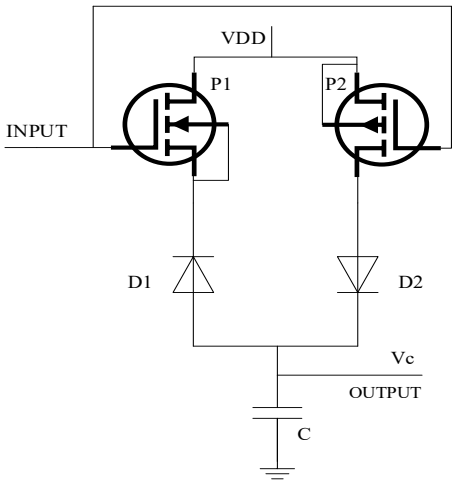

Fig.2.27: GFCAL inverter

2.3.27. Two-Phase Clocked CMOS Adiabatic Logic (2PC2AL)

According to Takahashi et al. (2009), this design uses two trapezoidal-wave pulses and behaves like static CMOS circuits.

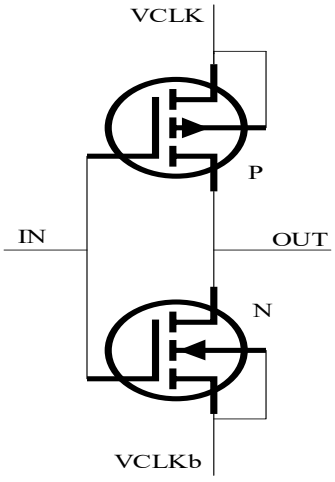

Fig.2.28: 2PC2AL Inverter

Regular static CMOS logic circuits are quite similar to the 2PC2AL in architecture. Further, we have proposed a 2PC2AL-compatible trapezoidal-wave generator. A switched capacitor circuit is

the basis of this new clock generator. Figure 2.28 shows the inverter in a 2PC2AL arrangement; in this setup, the inverter is shown working in conjunction with the corresponding phases of the power supply signals. The 2PC2AL's impressive performance is highlighted by its low switching latency and comparatively high throughput. At frequencies around 100 MHz, simulations of circuits using the 2PC2AL design have shown an energy usage decrease of almost two times.

2.3.28. Improved Clocked Adiabatic Logic (ICAL)

The schematic of the ICAL inverter/buffer may be seen in Fig. 2.29. The circuit uses P1, N1, P2, and N2 cross-coupled transistors to provide a memory operation and keep the output stable. As an auxiliary clock, the CX works in tandem with the PCLK to provide power. Both the evaluate and hold stages are essential to the functioning of this inverter/buffer circuit, as is the case with the majority of adiabatic logic topologies. The first phase involves logic devices N3 and N4 actively engaging with the CX, while logic devices N5 and N6 assess the states of OUT and OUTb. During the subsequent hold stage, signals OUT and OUTb keep the values stored in the memory element, namely P1, N1, P2, and N2, while signal CX is low and signals N3 and N4 are inactive. By substituting the logic devices (N5 and N6) with NMOS mutually exclusive logic trees that match each expression, the other Boolean expressions may be fulfilled (Ni & Hu, 2011).

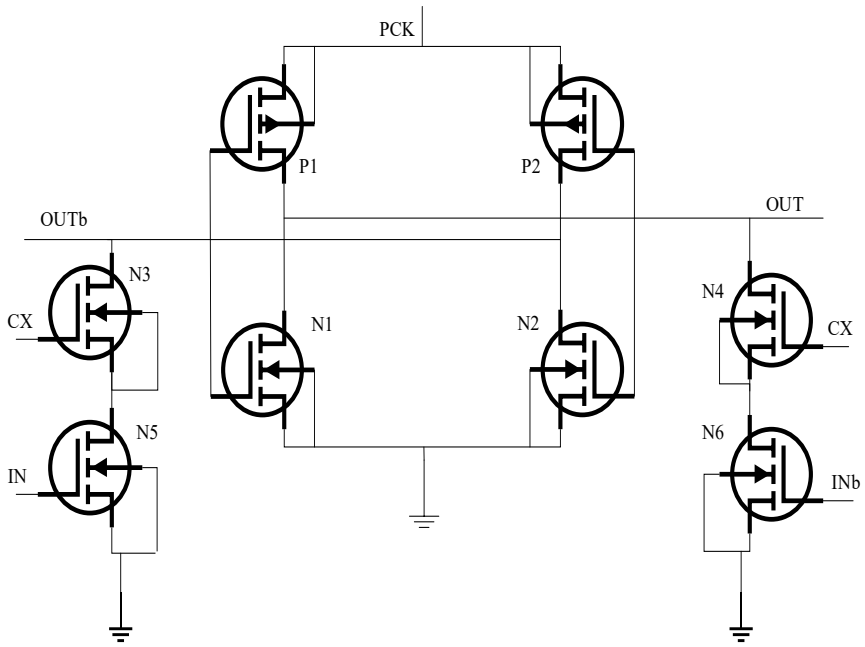

Fig.2.29: ICAL Inverter/Buffer

2.3.29. Energy-Efficient Adiabatic Logic (EFAL)

The principles underlying energy-efficient adiabatic logic (Chanda et al., 2012) are derived from differential cascode voltage swing (DCVS) logic, wherein a solitary sinusoidal source functions as the supply clock.

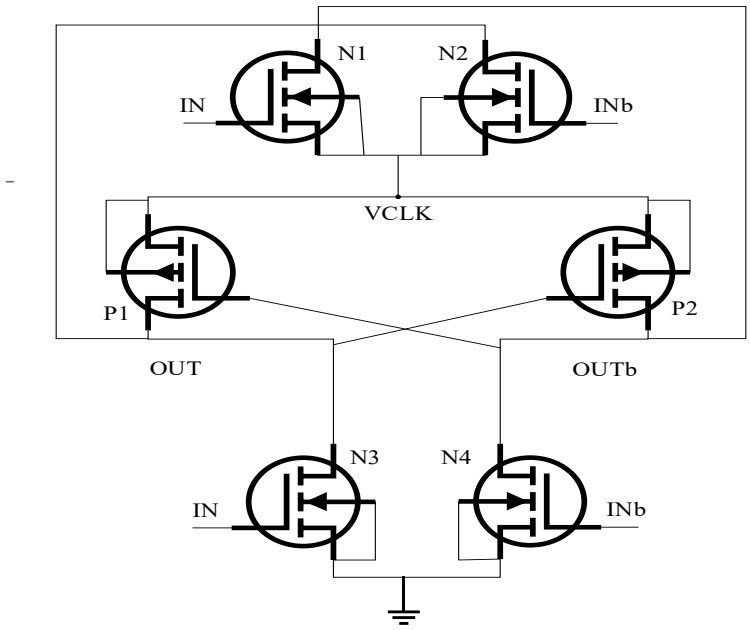

Fig.2.30: EEAL Inverter

By doing so, losses of energy can be effectively mitigated, and the intricacies of clock design, which might be exacerbated by the requirement for signal coordination, can be simplified. As depicted in Fig. 2.30, the EEAL model is a form of dual-rail adiabatic logic composed of two DCVS networks and two interconnected PMOS devices in each stage. To ensure the dependable operation of the Electrical Engineering Analysis Laboratory (EEAL), a solitary sinusoidal power source is employed. This methodology effectively resolves the concern of floating output through the establishment of a parallel pipeline linking the supply and output nodes.

2.3.30. Pre-resolve and Sense Adiabatic Logic (PSAL)

A logic circuit known as the PSAL has been developed to operate within the frequency range of 100 kHz to 500 MHz. A differential sensing logic and a sizable, pre-resolved NMOS structured tree are implemented.

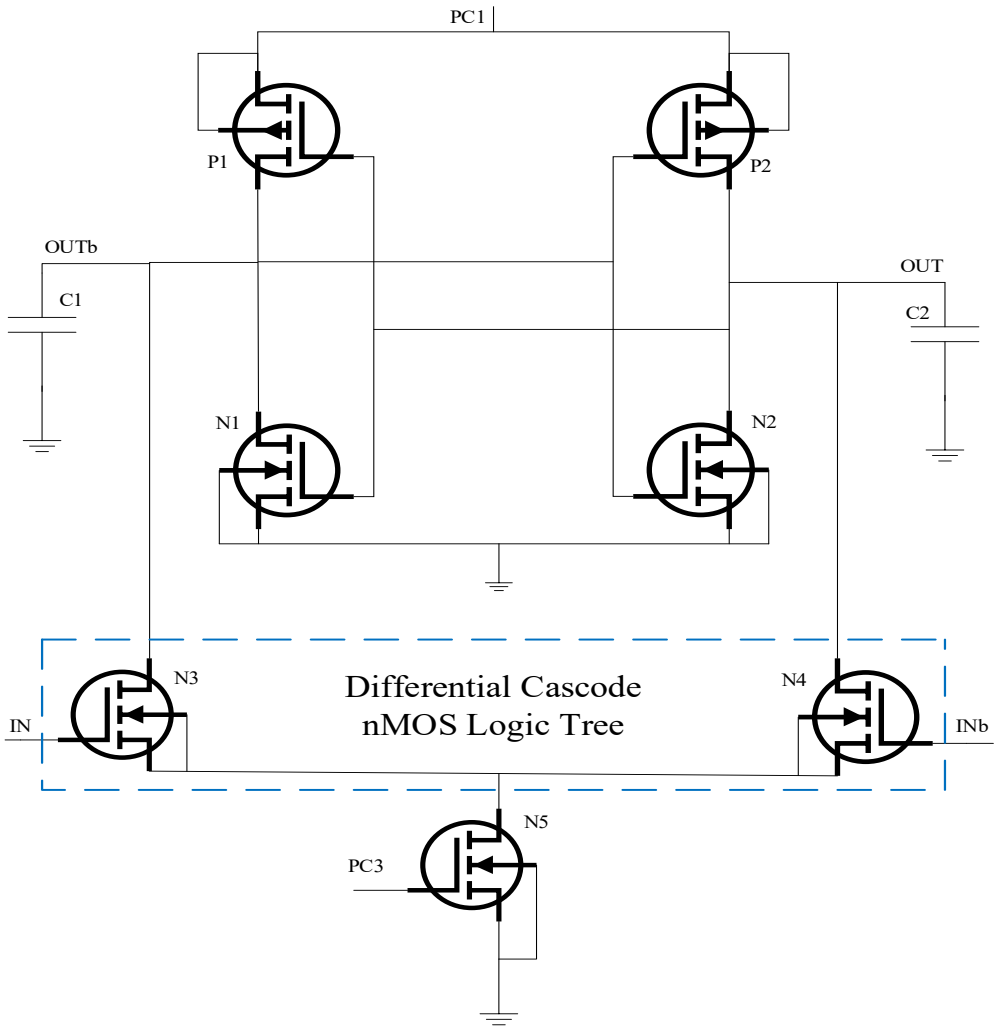

Fig.2.31: PSAL Inverter

PSAL has gained recognition for its exceptional energy efficiency, which is accomplished by minimizing switching transients, reducing silicon area necessities, and maintaining low circuit latency and glitch-free output. By substantially decreasing switching capacitance, it improves both efficiency and performance. By evaluating multiple levels of gates in each phase, PSAL eliminates the requirement for buffers in the adiabatic pipeline. By addressing the circuit latency challenges that are prevalent in four-phase adiabatic logic designs, this method enhances frequency efficacy by improving throughput and decreasing a critical path length. By utilizing differential sensing logic and a NMOS-structured cascode tree, it is possible to circumvent the challenges of inadequate charge retrieval and heating of the output node that are inherent in adiabatic logic architectures. The inverter circuit of PSAL is illustrated in Fig. 2.31, wherein the circuit's precise functions and operation are outlined (Kanchana & Raina, 2012).

2.3.31. Secured Quasi Adiabatic Logic (SQAL)

Secured Quasi Adiabatic Logic (SQAL) was first proposed by Avital et al. (2014). It is constructed upon the foundational principles of efficient charge recovery logic (ECRL). SQAL is designed to mitigate DPA vulnerabilities by integrating both intra-cycle and inter-cycle symmetry, in contrast to ECRL. Its compact, energy-efficient architecture and space efficiency make it a standout. SQAL also ensures unbiased initial conditions during evaluation, reducing the risk of unintentional information leakage through power and current profiles. The SQAL inverter is illustrated in Fig. 2.32

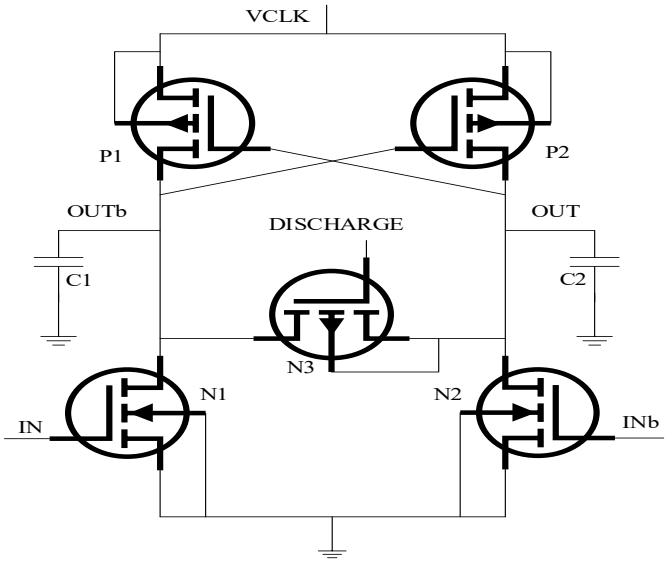

Fig.2.32: SQAL Inverter

2.3.32. Symmetric Pass Gate Adiabatic Logic (SPGAL)

In addressing the obstacles of Differential Power Analysis (DPA) resistance and energy savings, the Secured Quasi-Adiabatic Logic Family (SQAL) is an important breakthrough in mechanical design. The SQAL architecture represents a tremendous advancement over existing adiabatic logic designs that lack the capability to manage differential power analysis (DPA). The improvements are particularly conspicuous in relation to the area needed for operation and the loss of energy. A weakness of SQAL, nevertheless, is its susceptibility to non-adiabatic energy loss throughout the output evaluation procedure. To tackle this difficulty, Kumar et al. (2017) have proposed an innovative design methodology referred to as SPGAL. The buffer circuit utilized in an SPGAL is presented in a clear manner in Fig. 2.33. The utilization of SPGAL-

based gates in the development of circuits tailored for Internet-of-Things (IoT)-based electronic systems and low-power lightweight gadgets exhibits tremendous promise.

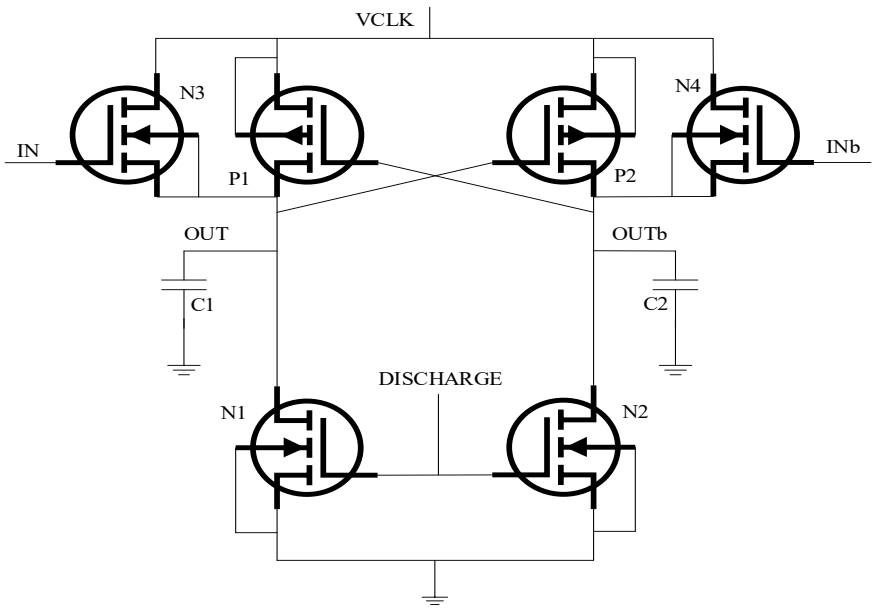

Fig.2.33: SPGAL Inverter

In addition to the aforementioned scholarly works, numerous contemporary and esteemed methodologies for adiabatic logic design have been extensively explored in the preceding sections. These methodologies are referenced as benchmarks for assessing power consumption and circuit delays to the proposed adiabatic logic circuits. In addition, the given adiabatic logic inverter circuits will be illustrated and elucidated through visual depictions within the following chapters.

Quasi-Static Energy Recovery Logic (QSERL):

The QSERL (Li et al., 2007) circuit is designed to include a set of complementary sinusoidal power clocks, each consisting of two unique phases known as the "evaluate" and "hold" phases. The existence of these alternating hold phases gives rise to a significant constraint in the form of floating output. The inclusion of timed feedback keepers in each logic circuit may potentially mitigate the issue of floating output. However, it is crucial to acknowledge that undesired losses may still occur.

***Complementary Energy path Adiabatic Logic* (*CEPAL*):**

The implementation of the CEPAL design offers enhanced robustness and recycle control when compared to the QSERL configuration. The data transfer capacity of the system stays unaltered by fluctuations in the frequency ratio, and it exhibits superior performance compared to the QSERL configuration, with a twofold improvement. Nevertheless, the existence of surplus diodes in the charging and discharging pathways of the structure results in substantial complications. As a consequence, the device attains marginally greater power waste and a comparatively greater physical footprint in comparison to QSERL configurations.

Two-phase clocked adiabatic static CMOS logic (2PASCL):

Since a diode is not included in the 2PASCL (Anuar et al., 2009) charging route, the current can only go to the PMOS transistor throughout the charging phase. The objective of this design decision is to minimize non-adiabatic losses resulting from diode voltage decreases. The 2PASCL circuit differs from previous quasi-adiabatic logic circuits by utilizing two split-level sinusoidal power clocks, as opposed to ramp or sinusoidal power clocks. These timekeeping devices have diminished voltage disparities between their electrodes, which may result in less power dissipation. However, the functionality of this circuit is limited due to the presence of diodes in both the pull-up and pull-down networks (which are attached in series beneath the NMOS and in parallel with the PMOS, respectively). The diodes mentioned above function in the manner of charge recycling that occurs in load capacitances. Nevertheless, it is critical to acknowledge that the incorporation of these components into the circuit could potentially lead to compromises in terms of net velocity and several other facets of accomplishment. The efficacy of this design is contingent upon the particular application and circuit needs, as actual electronic design frequently necessitates the careful consideration of power consumption, speed, and other variables in order to achieve design objectives.

Two Phase drive Adiabatic Dynamic CMOS Logic (2PADCL):

The 2PADCL method, as described by Takahashi et al. (2006), employs a dual sinusoidal power supply clock mechanism that demonstrates characteristics akin to those of static CMOS logic. The consequence is a substantial decrease in the timing delay associated with 2PADCL in comparison to the conventional ADCL circuit, particularly during its second and subsequent

stages. A direct derivation of the design concept of 2PADCL is possible from static CMOS logic circuits. The operational effectiveness of 2PADCL is demonstrated by its reduced switching delay and increased throughput compared to ADCL. The simulation results obtained for 2PADCL circuits demonstrate a significant drop in energy usage, with reductions ranging from a two-fold to a four-fold decrease.

Adiabatic Dynamic CMOS Logic (ADCL):

The operation of ADCL (Takahashi & Mizunuma, 2000) circuits requires the utilization of a voltage source that varies over time, hence inducing either a triangular or sinusoidal waveform. The change in output voltage in ADCL gates is synchronized with the corresponding change in the voltage supply source. Consequently, ADCL circuits have a marginally slower operating speed than static CMOS circuits. In the context of different electronic equipment, the significance of operating velocity may not be of utmost importance, as the emphasis is often placed on minimizing power consumption. In such cases, it is highly recommended to employ the ADCL design technique.

Adiabatic Differential Cascode Voltage Switch Logic (ADCVSL):

The ADCVSL may accomplish its tasks by using a split sinusoidal power clock with two phases rather than the more conventional four-phase trapezoidal power clock. Aiming to reduce power loss, the suggested ADCVSL circuits use charge recovery methods and cap peak current flow. A comprehensive analysis was conducted to examine the characteristics of the inverter, followed by the development of a mathematical framework to represent the power dissipation in the ADCVSL circuit. Furthermore, a comparative analysis was undertaken to assess the effectiveness of ADCVSL inverters in relation to other existing types of differential adiabatic logic.

Diode-Free Adiabatic Logic Circuit (DFAL):

The DFAL (Upadhyay et al., 2013) is distinguished by its intrinsic static property. Additionally, our study has presented a range of logical circuits based on Differential Function Approximation Logic (DFAL). Furthermore, we have performed a comparative evaluation of their operational efficiency compared to newly released adiabatic circuits and traditional CMOS circuits. The

fundamental objective of this method is to enhance overall efficiency without increasing complexity or lowering output magnitudes. It is worth mentioning that DFAL inverter circuits provide a significant advantage in terms of energy efficiency, with a nearly 60% reduction in energy usage compared to CMOS circuits. A noteworthy characteristic of the suggested topology is its lack of diodes in the charging or discharging channels. The DFAL system utilizes split-level sinusoidal power clocks, which are distinguished by a 180-degree phase disparity between them. In contrast to different adiabatic power clocks, the charge and discharge processes for the load capacitance occur at a marginally delayed rate when this split-level clock is in action.

Clocked Differential Cascode Adiabatic Logic (CDCAL):

The effectiveness of the CDCAL, a dynamic logic paradigm that functions at frequencies in the GHz range, is demonstrated. In order for the adiabatic pipeline to function, a two-phase sinusoidal power clock signal is required. By integrating a timed regulator transistor with the differential cascode logic framework, the suggested logic design achieves improved performance abilities and increased power savings. The simulation results authenticate the efficacy of CDCAL logic in high-frequency applications, showcasing its better performance associated to alternative two-phase adiabatic logic circuit approaches.

Two-phase adiabatic dynamic logic (2PADL):

A strategy for two-phase adiabatic dynamic logic known as 2PADL (Sasipriya & Bhaaskaran, 2018) optimizes energy efficiency through the utilization of gate overflow and decreased switching power. The system lacks complementary input signals associated with its parameters and is distinguished by its distinct rail output. Two complimentary clock signals, which serve as the power supply's propelling force, are necessary for the operational structure of 2PADL logic to function. The circuit is analogous to the CMOS design, with the exception of the addition of two transistors that govern the discharge and charging processes at the output node. By virtue of its capacity to regulate the discharge process, the 2PADL substantially diminishes the degree of switching activity. Further, it exhibits the capability of energy recovery at operational frequencies that are comparatively high, specifically reaching 600 MHz. In light of this, high-frequency purposes may successfully utilize the 2PADL logic design.

Clocked CMOS Adiabatic Logic (CCAL):

In order to derive the energy required for the operation of Clocked CMOS Adiabatic Logic (Li et al., 2013), two antiphase sinusoidal supply clocks are utilized. Two distinct components comprise the CCAL system: the clock control element and the CMOS logic aspect. These elements facilitate the connection between the logic segment and the output terminal by collaborating to perform logical assessments. The energy supply is produced through the utilization of an RLC resonant circuit to generate complementary sinusoidal supply cycles. When contrasting CCAL and QSERL, the latter incorporates diodes into its circuit design, impeding the output node's ability to charge and attain a logically high state at higher working frequencies. Consequently, this results in improper operation.

Differential Cascode Pre-resolve Adiabatic Logic (DCPAL):

DCPAL is a low-power design methodology that associations the profits of differential logic and cascode structures for energy-efficient circuit implementation. DCPAL leverages differential signal processing to reduce dynamic power consumption while maintaining high noise immunity. It operates by controlling pre-charge and evaluation phases in cascode-transistor configurations, which significantly reduces energy dissipation. DCPAL's main advantage lies in its ability to minimize short-circuit currents during transitions, making it suitable for high-performance low-power VLSI submissions, particularly in environments where low-energy operation is critical.

Improved Pass-Gate Adiabatic Logic (IPGAL):

IPGAL is an advanced adiabatic logic family designed to enhance energy efficiency in digital circuits. IPGAL modifies the traditional pass-gate logic by incorporating an adiabatic charging mechanism that recycles energy during signal transitions. This technique reduces power dissipation by enabling partial energy recovery, particularly in low-frequency operations. IPGAL circuits operate with reduced voltage swings, making them ideal for ultra-low-power applications such as portable and battery-powered devices. The architecture of IPGAL provides an optimized balance between energy savings and circuit complexity, enabling efficient logic gate implementation with minimal energy loss.

Two-Phase Positive Feedback Adiabatic Logic (2P-PFAL):

2P-PFAL is an energy-efficient design technique that utilizes a positive feedback mechanism for improved energy recovery. This logic family operates in two distinct phases, allowing gradual energy recovery by controlling the charging and discharging of nodes. The use of positive feedback ensures reliable operation while reducing power dissipation. 2P-PFAL circuits are particularly suitable for low-power VLSI applications, offering a noteworthy reduction in dynamic energy consumption associated to conventional CMOS logic. The two-phase approach enables near-zero energy loss in each clock cycle, promoting efficiency in high-frequency digital systems.

2.4. Power Supply in Adiabatic Logic

Adiabatic logic circuits necessitate the employment of non-conventional generators characterized by temporally varying voltage profiles; this is colloquially referred to as the power clock (Akers & Suram, 2002). The preceding term also signifies that the power clock is utilized to acquire the circuit's system clock, thereby obviating the necessity for an independent system clock. When integrating adiabatic logic, it is crucial to account for the substantial design constraints imposed by the supplementary hardware prerequisites of these particular power supply systems. One feasible strategy for achieving an even charging process of current is to estimate it through the use of a sinusoidal power supply.

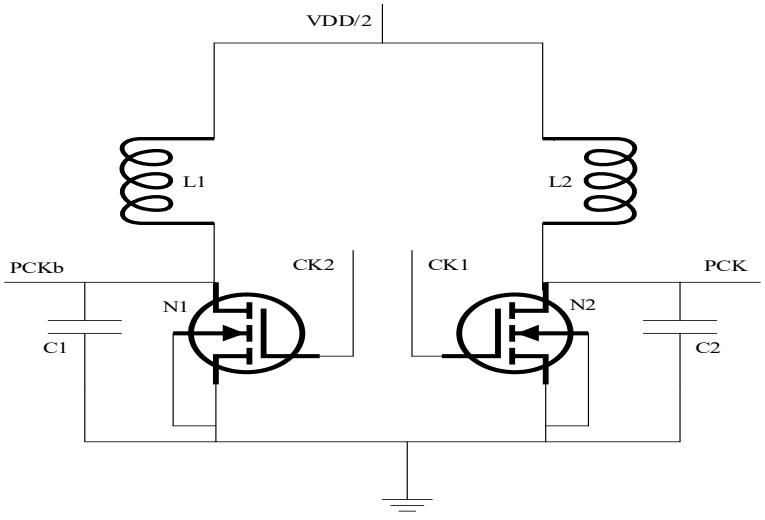

Fig.2. 34: Synchronous two-phase power clock generator (*Mahmoodi-Meimand et al., 2001)*

The generation of sinusoidal power clocks is possible through the utilization of LC resonant circuits, where “C” denotes the capacitance that was linked to the power clock line and its interconnected logic circuits, and “L” signifies an additional inductor. Numerous methodologies have been proposed to achieve resonant energy recovery in a wide range of adiabatic systems. A specific approach, as described by Mahmoodi-Meimand et al. (2001), involves the implementation of a resonant clock driver. This method, depicted in Fig. 2.34, produces the necessary sinusoidal pulse. It is important to acknowledge that the inclusion of an external inductor in this particular scenario is not only economically impractical but also results in cumbersome physical dimensions. Moreover, fluctuations in output load capacitances give rise to instability in clock frequency, and this approach unintentionally contributes unnecessary switching noise. The simplified structure of the LC-resonant-based power supply circuit intended for adiabatic logic, which was first familiarized by Takahashi et al. (2017), is illustrated in Fig. 2.35. Four separate parts comprise the circuit. To begin with, the system integrates a voltage-biasing instrument comprising two discrete voltage levels: Vdd/4 and 3Vdd/4. The second step is to produce two sinusoidal waveforms utilizing an external resonator. Furthermore, a resonant peak controller is integrated into the architecture in order to improve the precision of peak point identification in sinusoidal waveforms. A control function is integrated into the framework in order to regulate the current adequately. This is achieved through the reception of signals from the resonant peak controller, which are then utilized to modulate the current being introduced into the resonant circuit.

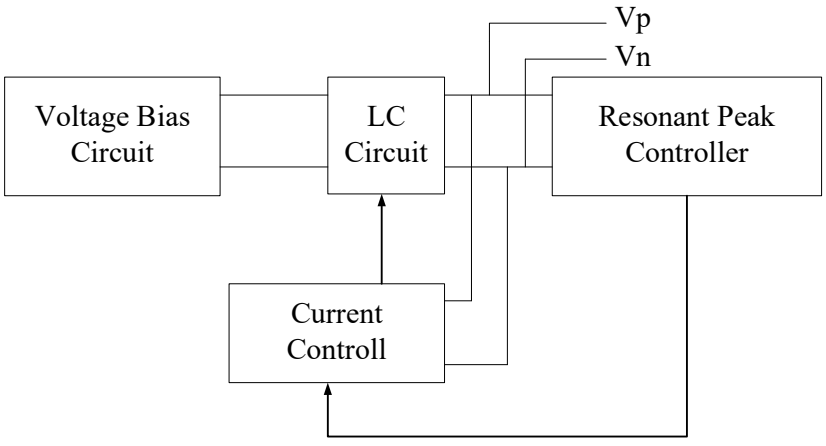

Fig. 2.35: LC resonant built supply circuit for adiabatic logic

2.4.1. Mathematical Design of an Adiabatic Power Supply

In order to accommodate the non-constant characteristics of the charging current, it is possible to implement a constant shape factor denoted as ξ in Eq. (2.8), where $\xi = \frac{\pi^2}{8}$ and the energy loss term is present. By incorporating an external inductor, it is possible to implement a sinusoidal power source. A resonant LC circuit is produced, characterized by a resonance frequency in proximity to $\frac{1}{LC}$. Using this circuit, it is possible to readily oscillate energy between an external inductor and the capacitances that require switching. By employing inductors, the method outlined by Younis, S. G. (1994) permits energy transmission between the load capacitor's electrostatic field and the off-chip inductor's magnetic field. Upon analyzing this particular technique, it is discovered that the energy conservation in the circuit is reduced by a factor of $\frac{\pi^2}{8}$ when a sinusoidal ramp is utilized, as opposed to a pure trapezoidal waveform. Moreover, the aggregate energy consumption, encompassing the power supply, can be delineated as follows:

$$E_{sin\,usoidal} = C_L V_{DD}^2 \left(\pi \sqrt{\frac{\tau_s}{T}} + \frac{\pi^2 \tau_c}{8T}\right) \tag{2.8}$$

Where the variables τ_c and τ_s represent the temporal constants that are inherent to the constituent circuit elements of both the computing segment and the power supply segment of the system, respectively.

Table.2.1: Efficiency of Three Popular Charging Waveforms

Source	Energy Dissipation (E_{diss})	
$V_{step(t)}$	$\int_0^{\infty} \left(Ve^{\frac{-t}{RC}}\right)^2 R.dt$	$\frac{1}{2}CV^2$
$V_{ramp(t)}$ $I_s = \frac{CV}{T}$	$\int_0^{\infty} I_s(t)\, R.dt$	$\frac{RC}{T}CV^2$
$\frac{V}{2}\left[sin\left(\frac{\pi}{T}t - \frac{T}{2}\right) + 1\right]$	$\int_0^{T} \left(\frac{VT^2\pi C\left(T\, sin\left(\frac{\pi t}{T}\right) - RC\pi\, cos\left(\frac{\pi t}{T}\right)\right)}{2T^4 + 2\pi^2 R^2 C^2 T^2}\right)^2 R.dt$	$\frac{\pi^2}{T}\frac{RC}{T}CV^2$

E_{diss}, or energy loss, is caused by three charging waveforms that are frequently observed: a discrete step, a ramping ramp with a linear increase, and a sinusoidal wave. The results mentioned above are succinctly presented in Table 2.1. It is important to highlight that the step input waveform exhibits the distinctive loss associated with $\frac{1}{2}CV^2$. However, it has been determined that the linear voltage gradient, characterized by a steady current profile, represents perhaps the most efficient adiabatic method of energy generation. As the charging duration T approaches infinity, there is a tendency for the loss to be close to zero. As a substitute for the linear ramp, the application of a sine wave tailored to resonate among 0 and V volts over a charging period of T has been proposed (Athas, W.C. et al., 1994). The rationale behind choosing this alternative is its straightforward construction using a resonant inductor and capacitor circuit. Sinusoidal inputs demonstrate superior energy efficiency in comparison to step inputs, provided that the period is suitably prolonged. However, its efficacy is only 28π or 81%, times greater than that of a slope with equivalent rise time. The notion of adiabatic charging entails the utilization of charging waveforms that surpass the conventional paradigm in order to attain enhanced charging efficiency. Enhanced performance can be attained through the implementation of methodologies such as ramp or sinusoidal waveforms.

CHAPTER-3

Improved Diode Free Adiabatic Logic (IDFAL)

3.1. Introduction

In the field of VLSI system design, low-power design has emerged as a major concern since modern electronic systems are increasingly requiring low-power usage. Electronic gadgets, both portable and nonportable, are highly popular nowadays. Several industries and companies have worked to provide devices with higher performance at lower costs since the evolution of VLSI technology (Athas et al., 1994; Chanda et al., 2015; Nayan et al., 2012; Moon & Jeong, 1996; Oklobdzija et al., 1997; Ye & Roy, 1996; Li et al., 2013). It appears that we are all now reliant on portable and hand-held devices. In both high-performance and portable applications, power consumption has become a major issue. Consequently, various design strategies are being developed to reduce power consumption (Han et al., 2019; Yuejun et al., 2018; Khatir et al., 2011). Energy recovery circuits operating on adiabatic principle have emerged as a highly auspicious low-power development strategy (Ye et al., 1997; Denker, 1994; Athas et al., 1994). Product efficiency and performance can be measured in several ways, but the speed of operation and power consumption (battery life) are usually the two most important factors (Moon & Jeong, 1996; Oklobdzija et al., 1997; Ye & Roy, 1996; Li et al., 2013; Han et al., 2019; Yuejun et al., 2018; Khatir et al., 2011; Kumar et al., 2019). When the device's performance is primarily focused on power consumption rather than speed of operation, adiabatically powered logic operation is desirable. The adiabatic design approach is advantageous for devices that can be powered at low frequencies, such as smart cards, Radio Frequency Identification (RFID) systems, and sensors (Kumar et al., 2019; Anuar et al., 2009). The primary goal of adiabatically designed circuits is to minimize energy loss in CMOS circuits while charging and discharging the load capacitor. Furthermore, since an AC power supply is employed instead of a DC power supply, the output transition by charging and discharging is considerably slowed down, resulting in no heat emission inside the adiabatic circuit as described in Dickinson & Denker (1995; Dickinson & Denker, 1994). In addition, the charge stored in the load capacitor is retrieved during a specific adiabatic phase, resulting in less energy loss. (Bhaaskaran & Raina, 2010; Blotti et al., 2010). Several adiabatic circuits have been presented over the years (Oklobdzija et al., 1997; Han et al., 2019; Starosel'skii, 2001; Kudithipudi & John, 2005). Output

floating, pipelining challenges, transmission delays, the requirement for several sophisticated cloaking systems, silicon area usage, and output voltage deterioration have all been reported by some of the adiabatic logic families (Gong et al., 2008; Chanda et al., 2018; Starosel'skii, 2001; Denker, 1994). The output voltage amplitude degradation is mainly because of the voltage drops that occur in the diode while charging and discharging the load capacitor (Dickinson & Denker, 1995; Dickinson & Denker, 1994; Takahashi & Mizunuma, 2000). The study proposed an IDFAL that is realized from conventional static CMOS logic (Ye & Roy, 1996; Anuar et al., 2009; Ye & Roy, 2001; Upadhyay et al., 2013). The logic utilized a two-phase, split-level complementary sinusoidal power clock system. Due to the split-level power supply, the peak current flowing through transistors can be suppressed, minimizing power consumption. In addition, the circuit is provided with control transistors to restrict the leakage power (Ye & Roy, 1996; Li et al., 2013; Sasipriya & Bhaaskaran, 2018; Sasipriya & Bhaaskaran, 2018).

3.1.1. Description of Power Clock

The adiabatic switching process can be implemented with different shapes of power supply waveforms, such as trapezoidal, triangular, and sinusoidal power sources. The sinusoidal power-clock timing events are depicted in Fig. 3.1. It is divided into two phases: *evaluation* and *hold*/*recovery*. During the *evaluation* phase, the energy is supplied to the circuit and, consequently, the output is being evaluated, whereas during the *hold* phase or *recovery* phase, the output is either held or recovered depending on the input conditions. In this phase, the energy stored at the output node can be recovered from the circuit and returned to the power supply. The four-phase trapezoidal power supply is shown in Fig. 3.2. It comprises events such as *evaluation*, *hold*, *recovery*, and *wait*. During the *evaluation* phase, energy is drawn from the power supply and utilized by the circuit to do useful work while the new output is being evaluated. The energy is kept at the output load capacitor during the *hold* phase and given back to the source power supply in the *recovery* period. The circuit is idle and awaits the next input during the *wait* state. In this work, we are using a sinusoidal power clock instead of a trapezoidal power supply since the sinusoidal waveform has more advantages than a trapezoidal power clock (Anuar et al., 2009; Ye & Roy, 2001). Adiabatic switching can be accomplished by keeping the voltage drop across the switching devices as low as possible, which can be achieved by charging the load output capacitor with a non-DC power supply such as a sinusoidal, trapezoidal, or triangular power clock, as demonstrated in Bhaaskaran & Raina (2010), Blotti et al. (2010), and Teichmann (2012).

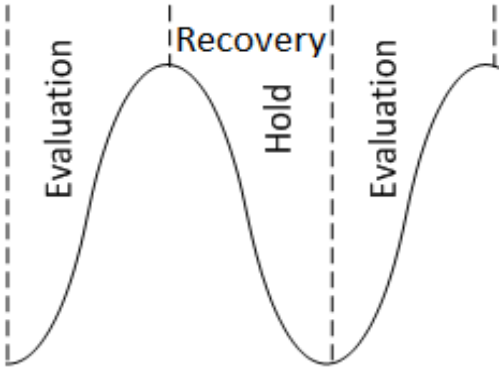

Fig. 3.1: Sinusoidal Power supply

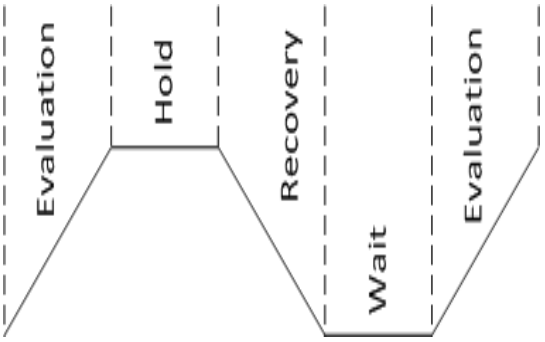

Fig. 3.2: Trapezoidal Power supply

3.2. Adiabatic Logic Families Involved in the Work

The architecture of the fundamental inverter circuits may be seen in Figs. 3.3–3.8. The 2PASCL and other well-known adiabatic reference works were consulted for this purpose (Anuar et al., 2009), 2PADCL (Takahashi et al., 2006), ADCL (Takahashi & Mizunuma, 2000), QSERL (Ye & Roy, 2001), DFAL (Upadhyay et al., 2013; Kumar & Kumar, 2022; Kumar & Kumar, 2020), and CCAL (Li et al., 2013). The proposed design, IDFAL, is compared with conventional CMOS logic and the above reference logic in respect of power consumption and propagation delays. In the energy recovery circuit that employs diodes, the energy benefit would be degraded unless the quotient of $\left(\frac{V_t}{V_{dd}}\right)$ is maintained while scaling a V_{dd} (Ye & Roy, 2001). The estimated energy dissipated by the diode during every logic transition is outlined by Ye and Roy (2001), as shown below,

$$E_{diode} = CV_t(V_{dd} - V_t) \tag{3.1}$$

Both technology scaling and power supply scaling are inseparable, and they are mutually exclusive. However, there is an inevitable problem with continual scaling of the threshold voltage, as it may lead to a significant increase in leakage current (Dadoria et al., 2018). Consequently, maintaining the $\left(\frac{V_t}{V_{dd}}\right)$ ratio while reducing the technology's scale is not possible, and the energy recovery circuits that involve diodes in the structure, such as 2PADCL, 2PASCL, ADCL, and QSERL, have encountered this type of drawback. In addition, QSERL, 2PASCL, and 2PADCL circuits also exhibited output voltage floating at alternate hold phases. A single-clock power supply is utilized in an ADCL circuit to reduce power consumption, but this imposes a substantial amount of gate delay

(Anuar et al., 2009). Another type of design: CCAL, DFAL, and IDFAL use clocked control transistors instead of diodes.

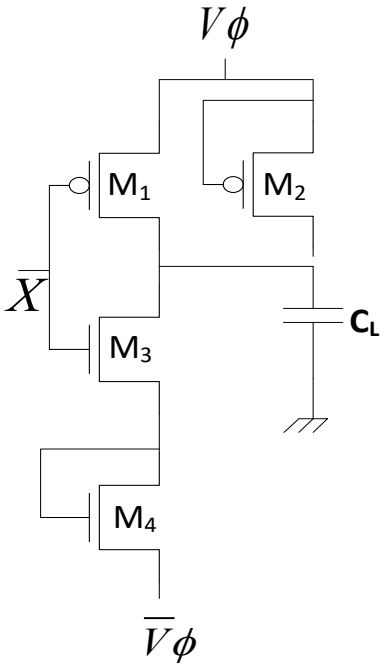

Fig. 3.3: Basic Inverter of 2PASCL

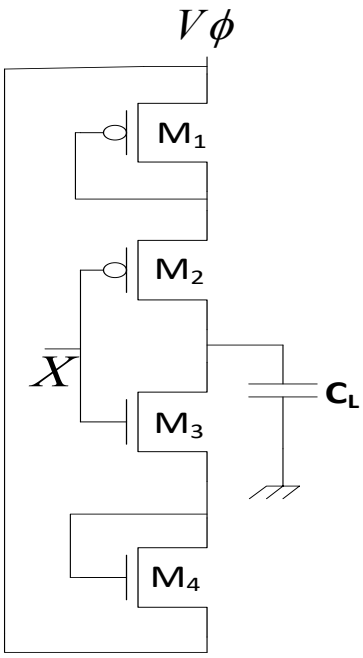

Fig. 3.4: Basic Inverter of ADCL

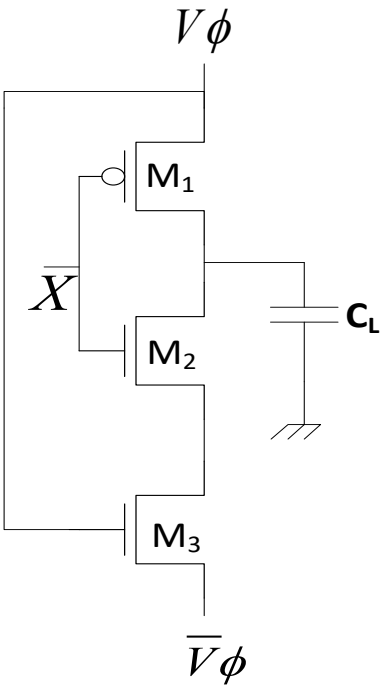

Fig. 3.5: Basic Inverter of DFAL

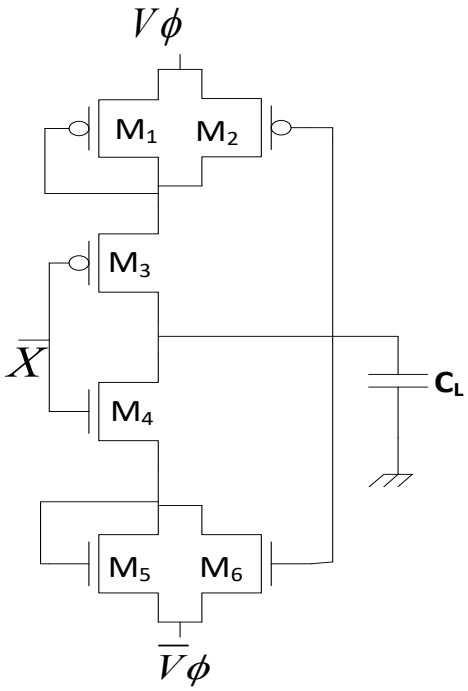

Fig. 3.6: Basic Inverter of QSERL

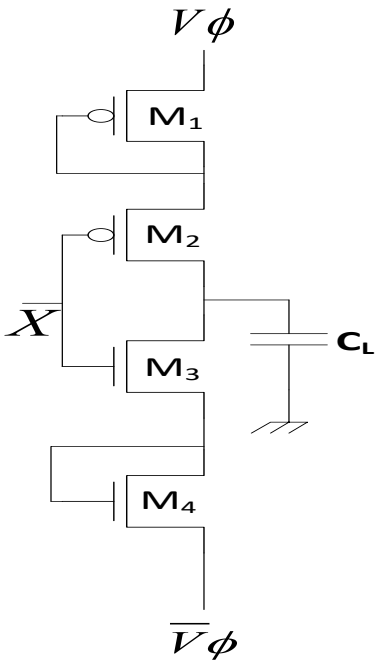

Fig. 3.7: Basic Inverter of 2PADCL

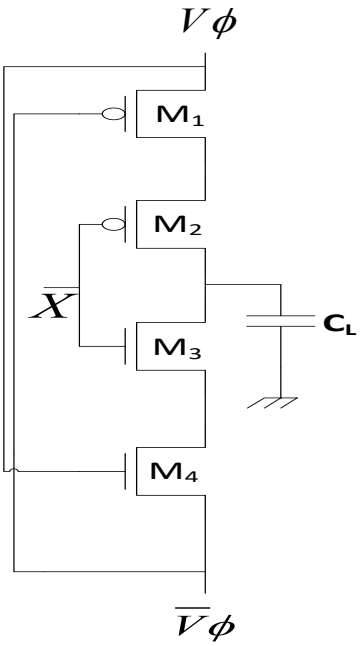

Fig. 3.8: Basic Inverter of CCAL

These control transistors restrict the output wave to following the power supply signal for the whole cycle, thereby reducing node switching activity. These types of circuits with clock control transistors can be operated at high frequencies (Li et al., 2013; Ye & Roy, 2001; Sasipriya & Bhaaskaran, 2018). The IDFAL has two control transistors attached to both the networks, as shown in Fig. 3.9. Moreover, unlike DFAL, the IDFAL circuit has lower discharging resistance due to a parallel transistor M_5 and optimizes power consumption. The control transistors are turned off during the hold phase, and hence the output is disconnected from the sources V_ϕ and $\overline{V_\phi}$. As a consequence, the output stays constant throughout this phase, and for this reason, there is minor output floating merely during half of a clock cycle, making it less susceptible to noise and leakage current.

3.3. Structure of the IDFAL

Figure. 3.9 shows a schematic of the IDFAL inverter, and Fig. 3.10 represents its RC equivalent circuit (Takahashi & Sato, 2015; Jadav & Chandel, 2019). The inverter circuit consists of five transistors in total: two control transistors M_1 and M_4, two functional transistors M_2 and M_3, and a transistor M_5 in the pull-down network for discharging. The control transistors, as their name

implies, control the charging and discharging times of the circuits. That is, the circuit is connected to the power supply and limits the flow of current only when it is deemed necessary, which eliminates redundant switching at the output node and, in turn, minimizes unwanted power dissipation. By replacing the transistors M_2 and M_3, any logic function can be implemented. In addition, the circuit employs complementary split-level sinusoidal power clocks, V_ϕ and $\overline{V_\phi}$, that replace V_{dd} and V_{ss}, respectively (Anuar et al., 2009). The two power clocks are 180 degrees out of phase. An LC resonant oscillator can be used to build and implement these types of power clocks effectively (Anuar et al., 2009; Takahashi & Sato, 2015; Jadav & Chandel, 2019). Each power clock's peak-to-peak voltage is set to half of that, implying that the magnitude of both V_ϕ and $\overline{V_\phi}$ peak-to-peak voltages is $\frac{V_{dd}}{2}$.

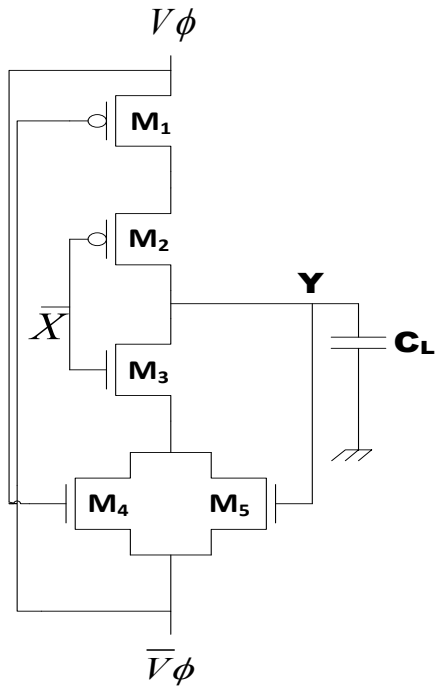

Fig. 3.9: Basic IDFAL Circuit

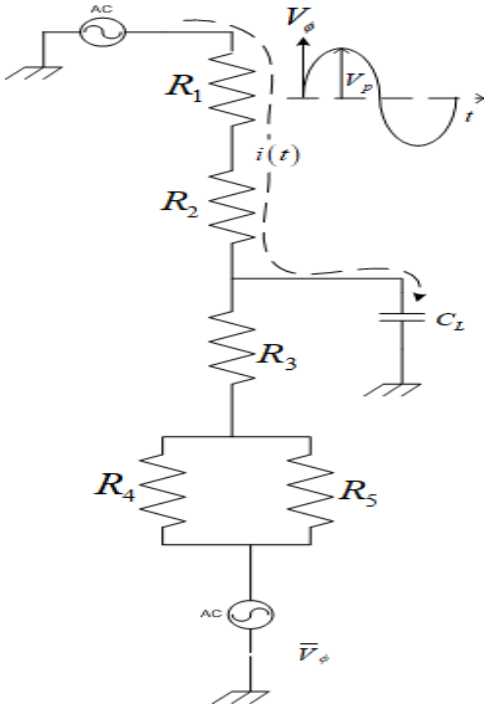

Fig. 3.10: Equivalent RC model of IDFAL

Therefore, by a factor of $\frac{V_{dd}}{2}$, the voltage level of V_ϕ is higher than that of $\overline{V_\phi}$. By utilizing these two power clocks in the circuit, the voltage between the current-carrying electrodes could be minimized, resulting in reduced power consumption, as mentioned in Starosel'skii (2001). That being stated, M_1 and M_4 are the control transistors that can be used to limit the flow of current in the

circuit and reduce dynamic and leakage power, while M_2 and M_3 are the functional transistors that influence logic operations. From Figs. 3.9 and 3.10, the output voltage across the load capacitor C_L swings at (Sasipriya & Bhaaskaran, 2018).

$$\left(\frac{V_{\phi p-p}-V_{ctl}}{2}\right) \tag{3.2}$$

Where $V_{\phi p-p}$ is the peak-to-peak voltage of the power supply V_ϕ, and V_{ctl} is the voltage drop across the control transistor M_1, which is close to the transistor's drain-to-source voltage V_{DS} and its threshold voltage V_t (Ye & Roy, 1996; Sasipriya & Bhaaskaran, 2018).

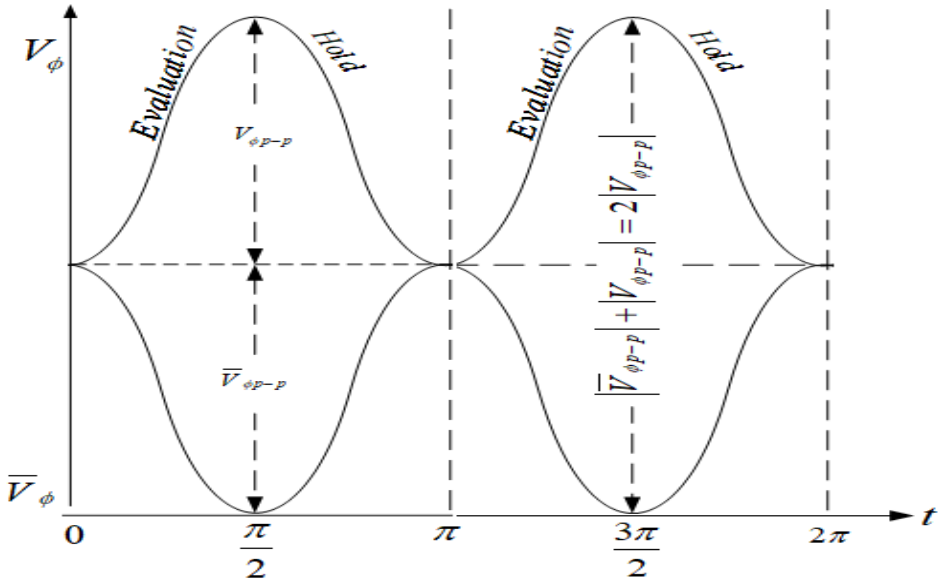

Fig. 3.11: A timing diagram of IDFAL

3.3.1. Working of the Circuit

The circuit operations can be described by referring to Figs. 3.9–3.11. Depending on the nature of power clocks, the circuit actions are split into two phases: *evaluation* and *hold,* as depicted in Fig. 3.11. During the evaluation interval, V_ϕ goes up and $\overline{V_\phi}$ goes down, whereas in the hold interval, the opposite happens: V_ϕ swings down and $\overline{V_\phi}$ swings up. From the schematic shown in Fig. 3.9, IDFAL is analogous to static CMOS logic. It is a normal static CMOS logic with two additional control transistors, one at the pull-up network and the other at the pull-down network, and

one more extra transistor in parallel to the NMOS tree for reducing the discharging resistance of the circuit. The function of the inverter circuit based on the IDFAL design is described below.

- *Evaluation Phase:*

1. In this phase, V_ϕ swings up and $\overline{V_\phi}$ swings down, and by the time they reach their corresponding threshold voltages, both the transistors M_1 and M_2 are turned on.
2. When output node Y is in logic 0, or the LOW state, and the PMOS tree is ON, the output load capacitor C_L is charged to logic 1 through the PMOS transistors M_1 and M_2, and hence the output is maintained in a HIGH state.
3. No transition happens when NMOS transistors in the pull-down network are ON but node Y logic level is in a LOW state.

When the output node is in a HIGH state and the NMOS transistors in the pull-down network are turned ON, the load capacitor C_L is discharged to $\overline{V_\phi}$ and recycled via the transistors M_3 and M_4, resulting in zero output logic.

- *Hold Phase:*

1. In this phase, V_ϕ swings down and $\overline{V_\phi}$ swings up, and, by the time they reach their corresponding threshold voltages, both the transistors M_1 and M_2 are turned off.
2. If the initial condition of the output node Y is high and only PMOS transistors in the pull-up network are switched on, no transition occurs.

Since the IDFAL is static in nature, unlike dynamic logic circuits in which each gate requires continual charging and discharging every clock cycle, the circuit nodes do not have to charge and discharge every clock cycle, which dramatically minimizes node switching activity. The hold phase significantly suppresses dynamic switching activities, resulting in lower power dissipation.

3.3.2. Dynamic Energy Consumption

Assuming all the initial conditions of the circuit are zero. During the charging process, the amount of charge ejected from the power supply is provided below, with reference to the works of Anuar et al. (2009) and Takahashi & Mizunuma (2000).

$$Q = C_L\left(\frac{V_{\phi_{p-p}} - V_{ctl}}{2}\right) \tag{3.3}$$

The energy requires to transport the charge Q through the control transistor M_1 (Dickinson & Denker, 1995).

$$E_{ctl} = QV_{ctl} \tag{3.4}$$

From Eqs. (3.2) & (3.3), we get

$$E_{ctl} = C_L\left(\frac{V_{\phi_{p-p}} - V_{ctl}}{2}\right)V_{ctl} \tag{3.5}$$

Also, the energy dissipated in the ON-resistance R_2 of the charging path is given as,

$$E_{R_{2(chrg)}} = i^2R_2T = \left(\frac{Q}{T}\right)^2 R_2T \tag{3.6}$$

$$= \left(\frac{R_2C_L}{T}\right)C_L\left(\frac{V_{\phi p-p} - V_{ctl}}{2}\right)^2$$

$$= \left(\frac{R_2C_L}{4T}\right)C_L\left(V_{\phi p-p} - V_{ctl}\right)^2 \tag{3.7}$$

Therefore, from (3.4) and (3.6), total energy lost on charging is given as (Takahashi & Mizunuma, 2000),

$$E_{T(chrg)} = E_{ctl} + E_{R_{2(chrg)}} \tag{3.8}$$

$$E_{T(chrg)} = C_L\left(\frac{V_{\phi_{p-p}} - V_{ctl}}{2}\right)V_{ctl} + \left(\frac{R_2C_L}{4T}\right)C_L\left(V_{\phi p-p} - V_{ctl}\right)^2 \tag{3.9}$$

The energy lost owing to threshold voltage of the transistor M_2 when it starts to be conductive is estimated as (Moon & Jeong, 1996; Ye & Roy, 1996; Takahashi & Mizunuma, 2000).

$$E_{tp} = \frac{1}{2}C_L\left|V_{tp}\right|^2 \tag{3.10}$$

Whereas, during discharging, the energy consumed by the NMOS transistor M_3 due to the threshold voltage has the same expression as:

$$E_{tn} = \frac{1}{2}C_L|V_{tn}|^2 \tag{3.11}$$

E_{tp} and E_{tn} are the non-adiabatic energy losses that are inevitable (Moon & Jeong, 1996). On discharge, the energy accumulated across the output load capacitor C_L is dissipated across the discharging path transistors. From Eq. 3.2, the output voltage swing is:

$$V_{out} = \left(\frac{V_{\phi p-p} - V_{ctl}}{2}\right) \quad (3.12)$$

By applying Kirchhoff's voltage law (KVL) to the discharging route when $\overline{V}_{\phi}$ is swinging down as shown in (Sasipriya & Bhaaskaran, 2018).

$$V_{out} = V_R + V_{PDT} \quad (3.13)$$

Where V_R denotes the voltage drop across transistor M_3, and V_{PDT} denotes the voltage across parallel transistors M_4 and M_5. Since the output voltage is identical to the load capacitor voltage, the total energy consumption on discharging will be formulated as:

$$E_{T(dischrg)} = E_{R_{3(dischrg)}} + E_{PDT(dischrg)} \quad (3.14)$$

The energy dissipated in the parallel transistors is the product of the voltage drop across the transistors and the charge drawn from the output capacitor on discharging.

$$E_{PDT(dischrg)} = QV_{PDT} \quad (3.15)$$

From Eqs. (3.3) and (3.15), we get

$$E_{PDT(dischrg)} = C_L \left(\frac{V_{\phi p-p} - V_{ctl}}{2}\right) V_{PDT} \quad (3.16)$$

The energy lost while discharging on the ON resistance R_3 is the same as it is in Eq. 3.7, as mentioned in Takahashi & Mizunuma (2000).

$$E_{R_3(dischrg)} = \left(\frac{R_3 C_L}{4T}\right) C_L \left(V_{\phi p-p} - V_{ctl}\right)^2 \quad (3.17)$$

From Eqs. (3.14), (3.16), and (3.17), the total energy lost while discharging is:

$$E_{T(dischrg)} = \left(\frac{R_3 C_L}{4T}\right) C_L \left(V_{\phi p-p} - V_{ctl}\right)^2 + C_L \left(\frac{V_{\phi p-p} - V_{ctl}}{2}\right) V_{PDT} \quad (3.18)$$

The total energy loss, on the other hand, is the sum of dynamic and static energy dissipations (Hu et al., 2010).

$$E_{Total} = E_{dynamic} + E_{static} \quad (3.19)$$

The total energy consumption of the IDFAL inverter is given as,

$$E_{IDFAL} = (E_{adb} + E_{non-AL})_{dynamic} + (E_{leak})_{static} \quad (3.20)$$

$$E_{adb} = E_{T(chrg)} + E_{T(dischrg)}$$

From (3.19) and (3.18)

$$E_{adb} = C_L\left(\frac{V_{\phi_{p-p}} - V_{ctl}}{2}\right)V_{ctl} + \left(\frac{R_2 C_L}{4T}\right)C_L\left(V_{\phi p-p} - V_{ctl}\right)^2$$

$$+\left(\frac{R_3 C_L}{4T}\right)C_L\left(V_{\phi p-p} - V_{ctl}\right)^2 + C_L\left(\frac{V_{\phi p-p} - V_{ctl}}{2}\right)V_{PDT} \quad (3.21)$$

The non-adiabatic loss is the energy lost due to the threshold voltage or drain-source potential difference when a MOS transistor begins to be conductive. Assuming the NMOS and PMOS are symmetrical (Takahashi & Mizunuma, 2000; Ye & Roy, 1995). Hence, from (3.10) and (3.11),

$$E_{non-AL} = E_{tp} + E_{tn} = \frac{1}{2}C_L\left|V_{tp}\right|^2 + \frac{1}{2}C_L|V_{tn}|^2$$

$$\frac{1}{2}C_L\left|V_{tp}\right|^2 = \frac{1}{2}C_L|V_{tn}|^2 = \frac{1}{2}C_L {V_{th}}^2$$

$$E_{non-AL} = C_L {V_{th}}^2 \quad (3.22)$$

Assuming R_2 and R_3 are the same and denoted as R, the total energy consumption of an IDFAL circuit is given as,

$$E_{IDFAL} = \left(\frac{RC_L}{2T}\right)C_L\left(V_{\phi p-p} - V_{ctl}\right)^2$$

$$+C_L\left(\frac{V_{\phi p-p} - V_{ctl}}{2}\right)(V_{ctl} + V_{PDT}) + C_L {V_{th}}^2 + E_{leak} \quad (3.23)$$

3.3.3. Leakage Energy Consumption

The general equation of leakage current is given as (Gong et al., 2008; Teichmann, 2012),

$$I_{leak} = I_0 e^{\frac{V_{GS} - V_{th}}{nV_T}}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \quad (3.24)$$

$$V_T = \frac{kT}{q}$$

Here, V_T is the thermal voltage, $k$is Boltzmann's constant, T is the temperature in kelvin, and $q$is the number of charges in coulombs. A general formula for energy consumption is given below (Takahashi et al., 2006; Anuar et al., 2009),

$$E_{diss} = \int_0^{T_S}\left(\sum_{i=1}^{n} V_{pi} \times I_{pi}\right)dt \quad (3.25)$$

The power clock and power clock bar expressions are given in Eq. (3.24) (Anuar et al., 2009; Nayan et al., 2012; Upadhyay et al., 2013).

$$V_\phi = \frac{V_{DD}}{4} sin(wt + \theta) + \frac{3}{4} V_{DD}$$
$$\overline{V_\phi} = -\frac{V_{DD}}{4} sin(wt + \theta) + \frac{1}{4} V_{DD} \quad (3.26)$$

According to Hu et al. (2010), the leakage energy is given as,

$$E_{leak} = \int_0^T P_{leak}(t)dt$$
$$\approx \int_0^{\pi} I_{leak} \cdot V_\phi(t)dt + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \left(I_{leak} \cdot \overline{V}_\phi(t)\right) dt \quad (3.27)$$

Referring to Fig. 3.11, the integration intervals are obtained.

$$= \int_0^{\pi} I_{leak} \cdot \left(\frac{V_{DD}}{4} sin(wt + \theta) + \frac{3}{4} V_{DD}\right) dt$$
$$+ \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} I_{leak} \cdot \left(-\frac{V_{DD}}{4} sin(wt + \theta) + \frac{1}{4} V_{DD}\right) dt$$
$$= I_1 + I_2$$
$$I_1 = \int_0^{\pi} I_{leak} \left(\frac{V_{DD}}{4} sin(wt + \theta) + \frac{3}{4} V_{DD}\right) dt \quad (3.28)$$
$$= I_{leak} \frac{V_{DD}\, cos(\theta) - V_{DD}\, cos(\theta + \pi w) + 3\pi V_{DD} w}{4w}$$
$$I_2 = \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} I_{leak} \left(-\frac{V_{DD}}{4} sin(wt + \theta) + \frac{1}{4} V_{DD}\right) dt \quad (3.29)$$

Therefore, the leakage energy may be approximated as:

$$E_{leak} = I_{leak} \frac{V_{DD} \cos\left(\frac{2\theta + 3\pi w}{2}\right) - V_{DD} \cos\left(\frac{2\theta + \pi w}{2}\right) + \pi V_{DD} w}{4w} \quad (3.30)$$

3.4. Circuit Using IDFAL

Adiabatic logic is a subfield of digital circuit design that provides a number of benefits when building sequential and combinational circuits. Adiabatic reasoning is predicated on the tenet that less energy is used when possible. While there are many benefits to using adiabatic logic, there are

also some drawbacks to be aware of. These encompass, in comparison to conventional CMOS logic, a higher degree of circuit complexity, additional design concerns, and the possibility of slower operating rates. When designing digital circuits, adiabatic logic may provide compelling solutions that meet the requirements of reducing heat, conserving energy, and power. Here we take a look at several digital combinational and sequential circuits using the IDFAL circuit technique.

3.4.1. Basic Inverter Circuit

The circuit simulations are conducted using the cadence virtuoso's spectre simulator in an analog development environment. Fig. 3.12 shows the basic inverter circuit of IDFAL using 45nm_HP_PTM technology with parameters $C_L = 10pf$ and $V_{in} = 1V$.

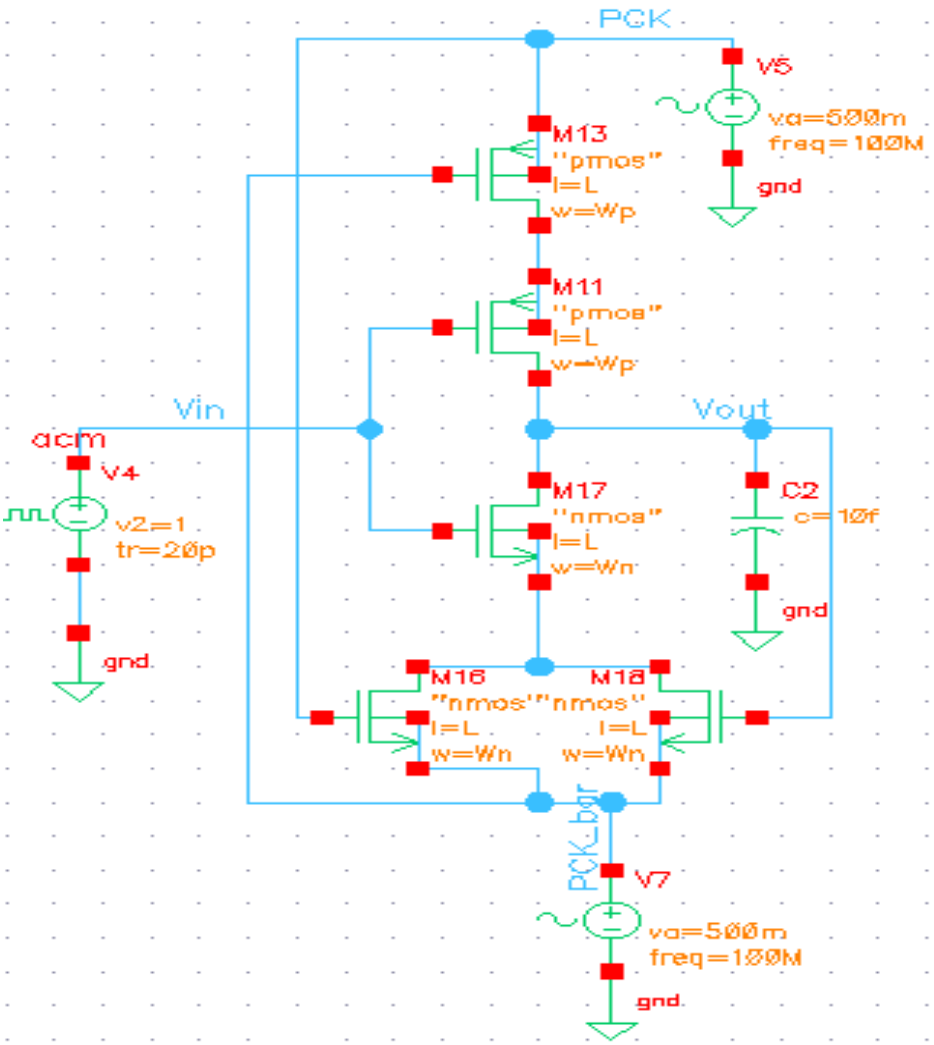

Fig. 3.12: Basic Inverter Circuit.

Both the power clock PCK and PCK_bar are represented by the time-varying voltages V_ϕ and $\overline{V_\phi}$, and the magnitude of each peak voltage is set to $0.5V$. The operating frequency is set at $100MHz$, and the duration of each simulation is fixed at 50 ns. Unlike other recovery circuits, both complementary power supply frequencies do not need to be double or larger than the input signal frequency but can be operated at the same frequency. That is to say, the input frequency and the supply frequency are kept at the same value. In the case of 2PASCL, IDFAL, etc., power clock frequencies can be double, triple, or multiples of input frequencies, and that may cause more delay time in logic transitions.

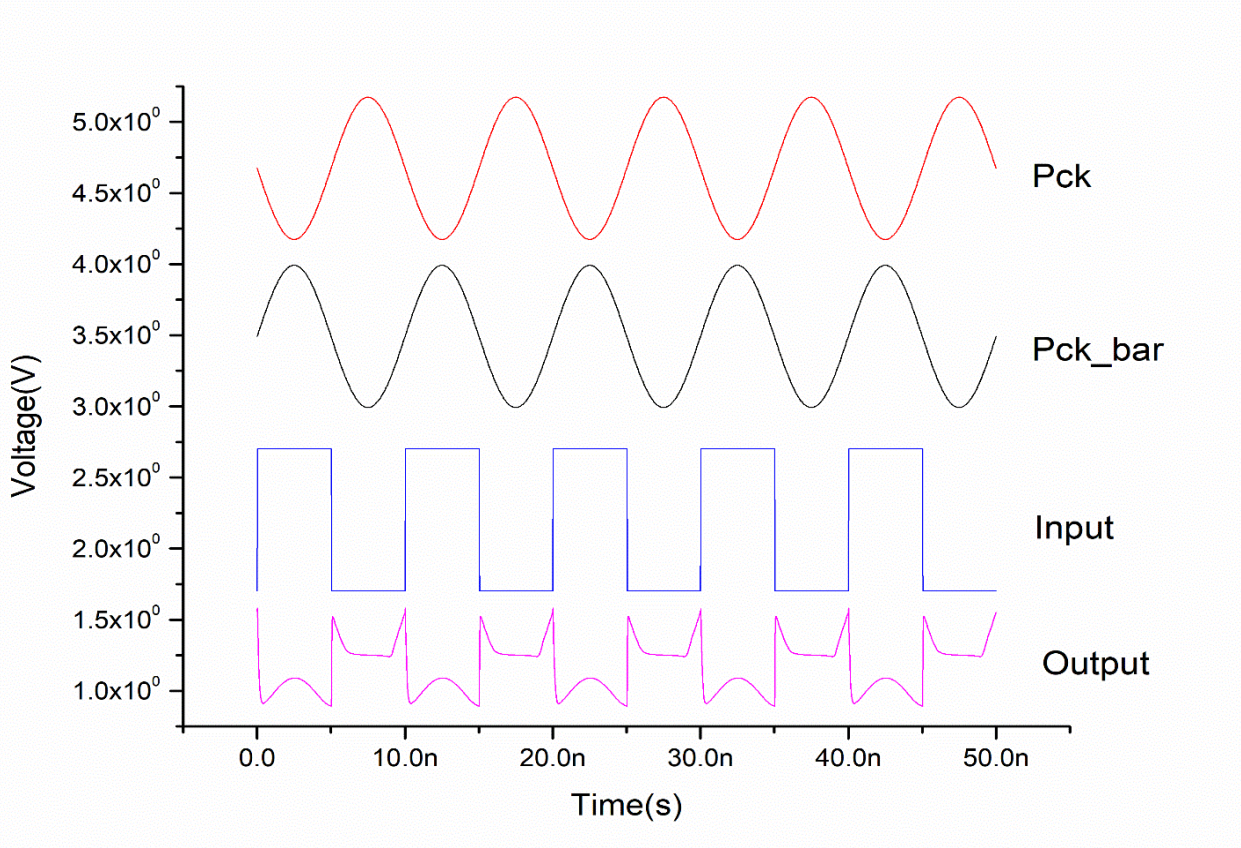

Fig. 3.13: Waveform of the IDFAL Inverter Circuit.

Fig. 3.13 depicts the waveform of the IDFAL inverter, and by utilizing the graph tool, the circuit delay was directly measured and evaluated. It's worth noting that we do not apply a DC offset voltage to the complementary power clocks in any simulations when analysing the power consumption and the propagation delay of each circuit.

3.4.2. NAND Gate Using IDFAL

Maintaining all the circuit parameters and power supply under the same conditions as the previous IDFAL inverter circuit, a NAND gate circuit is designed based on IDFAL and simulated to ensure the feasibility of the IDFAL design technique. The circuit and waveform are shown in Fig. 3.14 and Fig. 3.15, respectively.

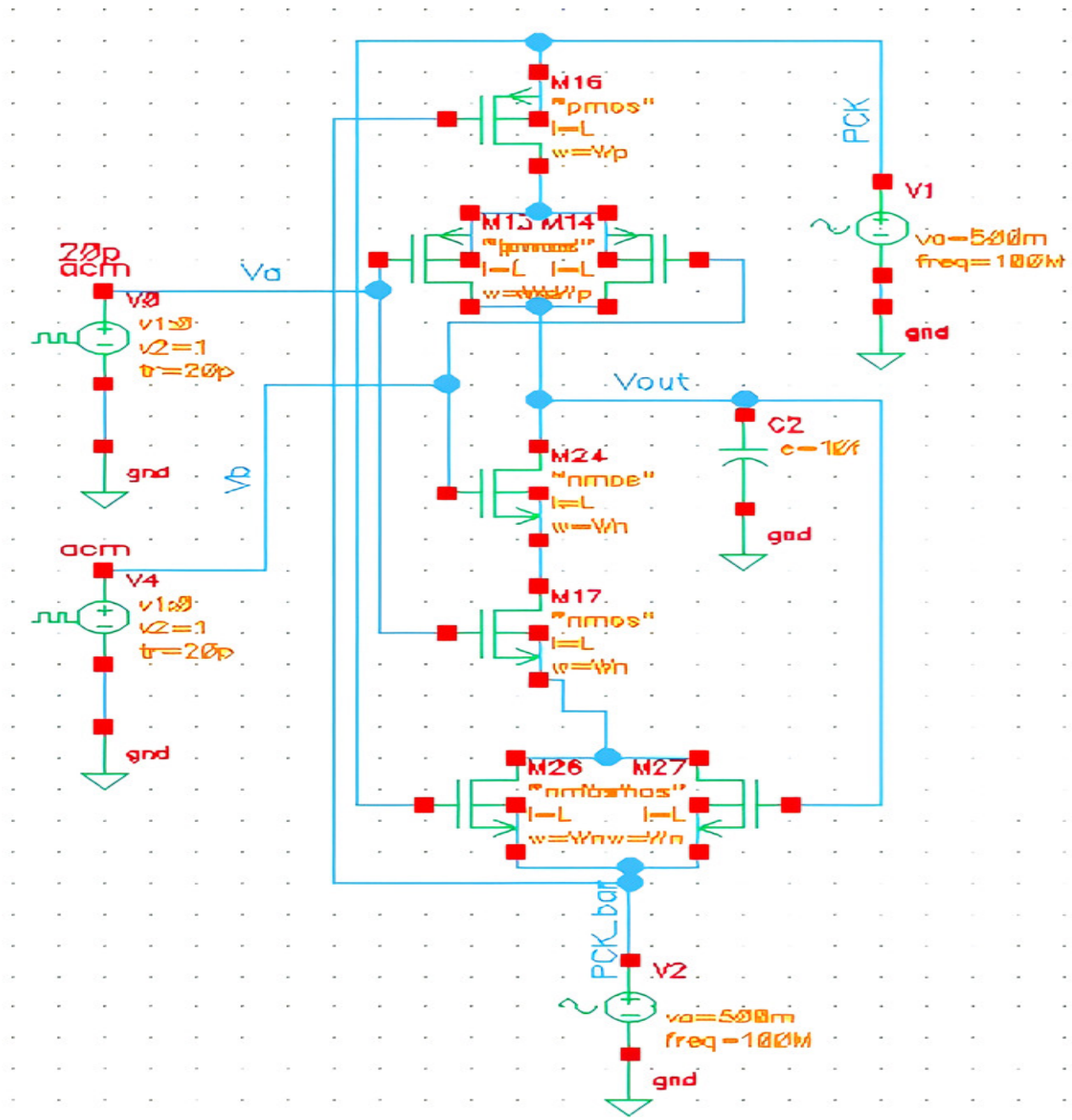

Fig. 3.14: IDFAL NAND gate.

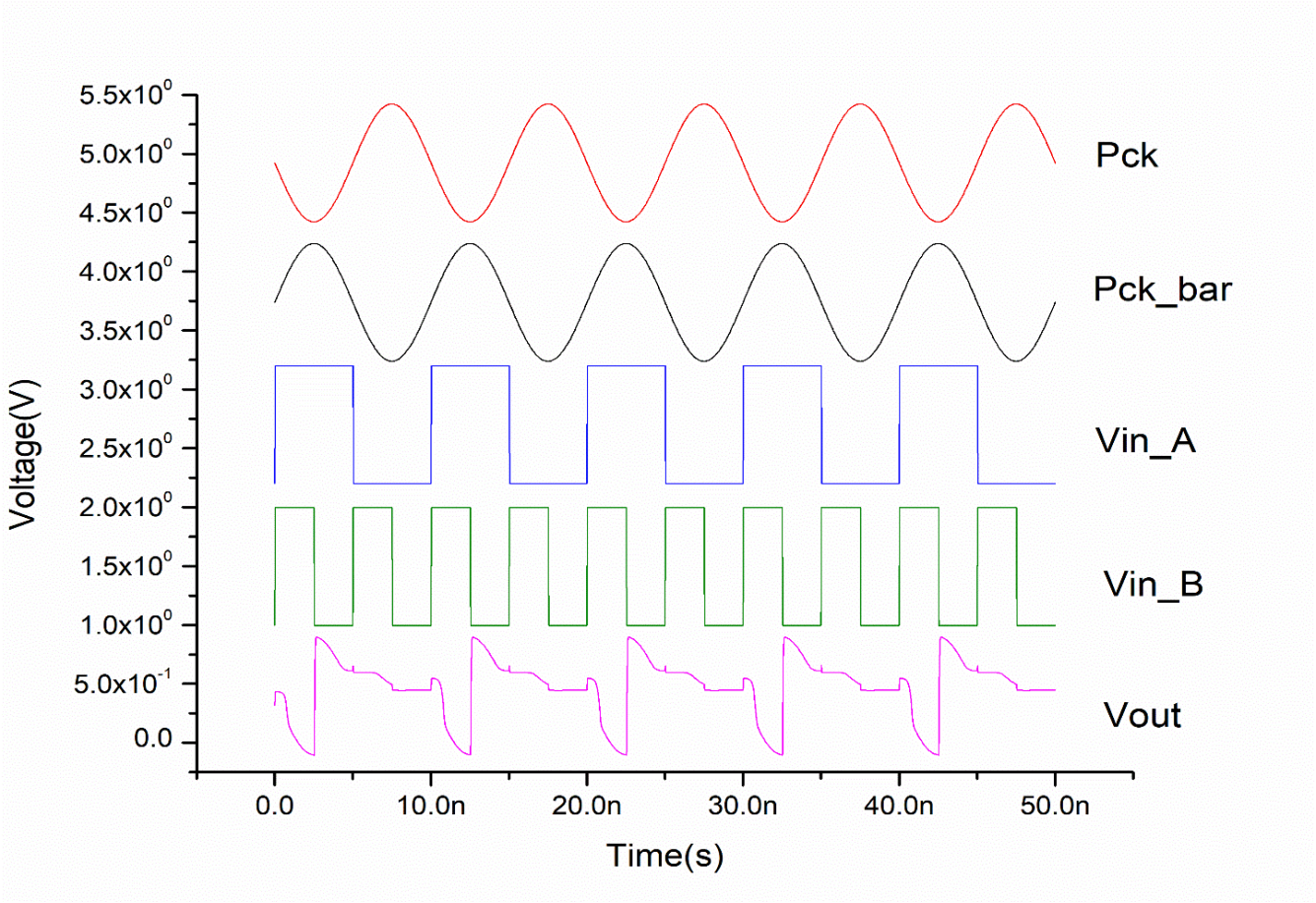

Fig. 3.15: Waveform of IDFAL NAND gate

3.4.3. IDFAL Inverter Chain

Figure 3.16 depicts the four inverter chains of an IDFAL circuit, each with a load capacitance of $0.01pf$. The power supply is connected in such a way that every alternate inverter has a different phase of power source than the previous inverter and vice versa (Ye & Roy, 2001). During the evaluation phase, the output of the first and third inverters follows the power clock, whereas there is an antiphase with the second and fourth inverters. During the hold period, the opposite happens. The alternate power supply is useful for successful pipelining and cascading and to minimize the floating of the output nodes. Fig. 3.17 shows the waveform of the IDFAL four-inverter chain, indicating each output stage and the output logic are not degraded. The phases of cascaded inverters are reversed; when the second inverter is evaluated, the first inverter is in the hold phase.

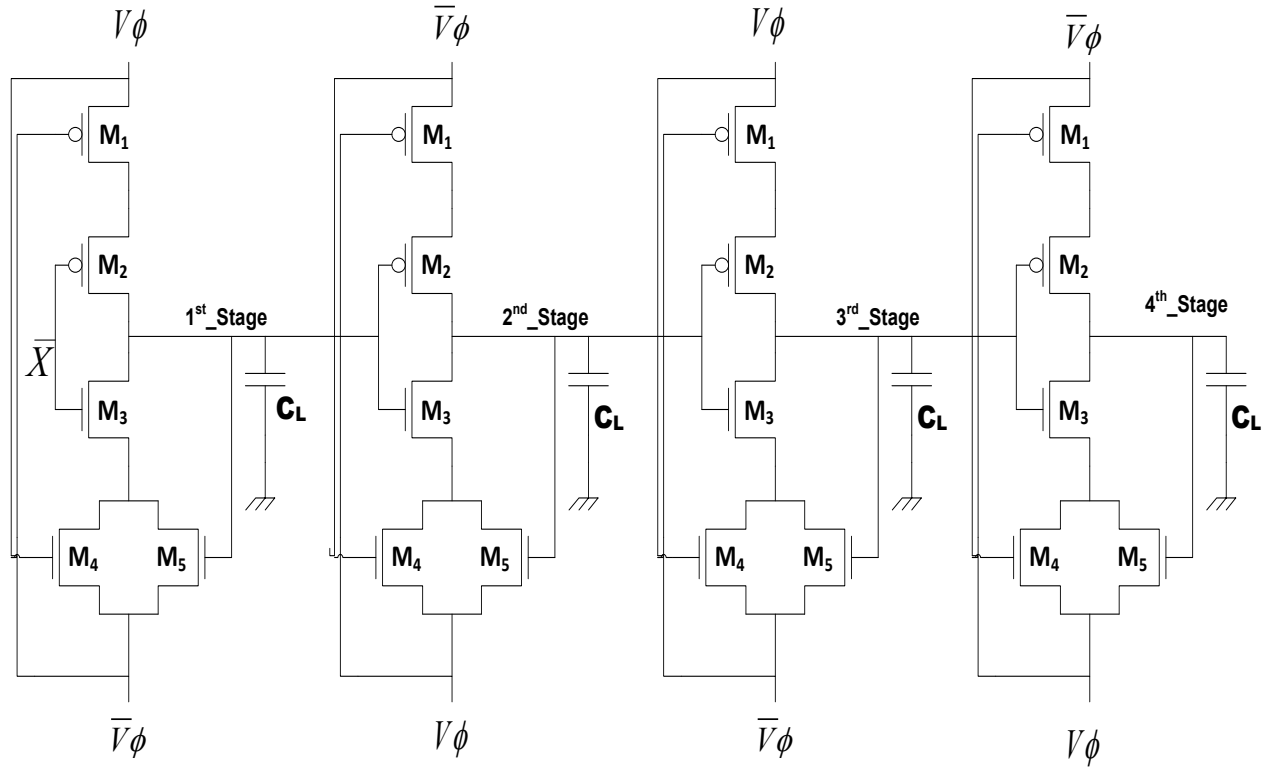

Fig. 3.16. Pipelining of IDFAL Inverter

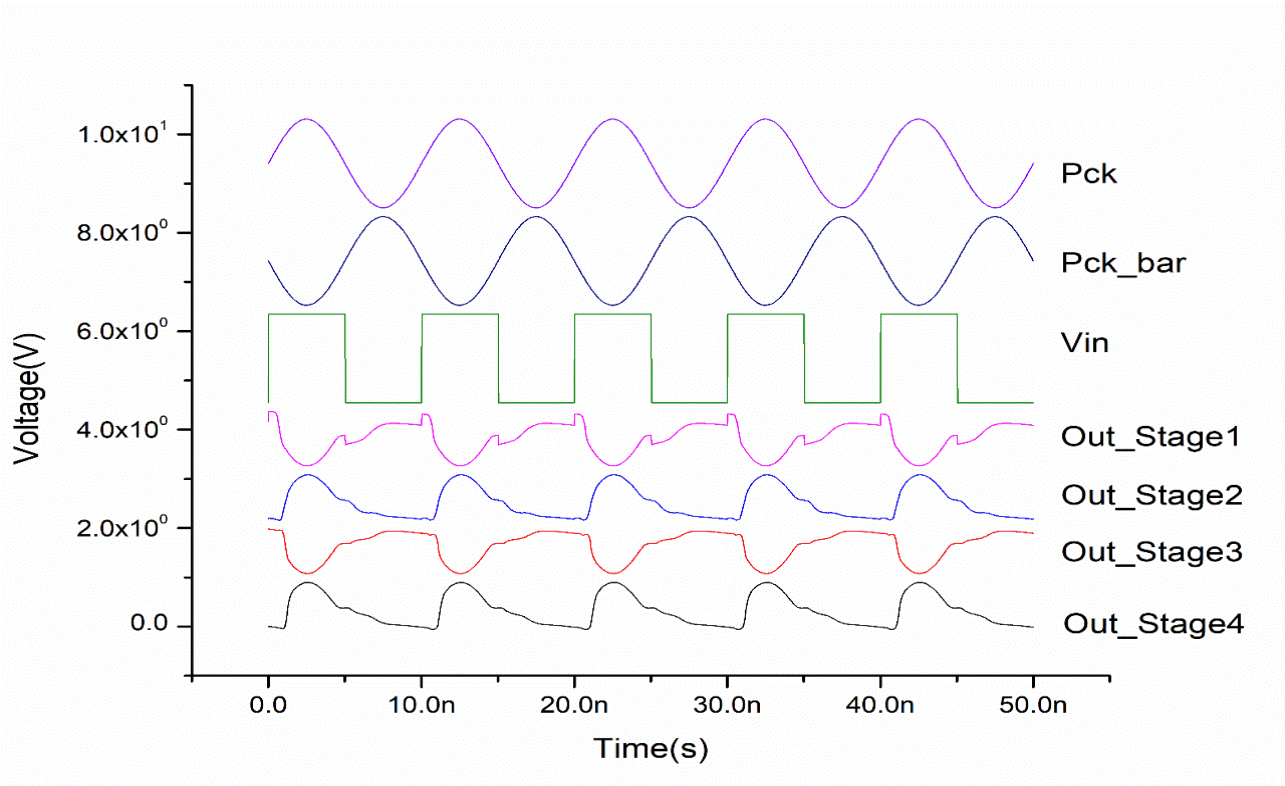

Fig. 3.17: Waveform of IDFAL Inverter Chain

3.4.4. SR Flip Flop Using IDFAL

The SR flip flop can be constructed with either two-input NOR or NAND gates since they are more adaptable compared to other gates, and the NAND is the most commonly used.

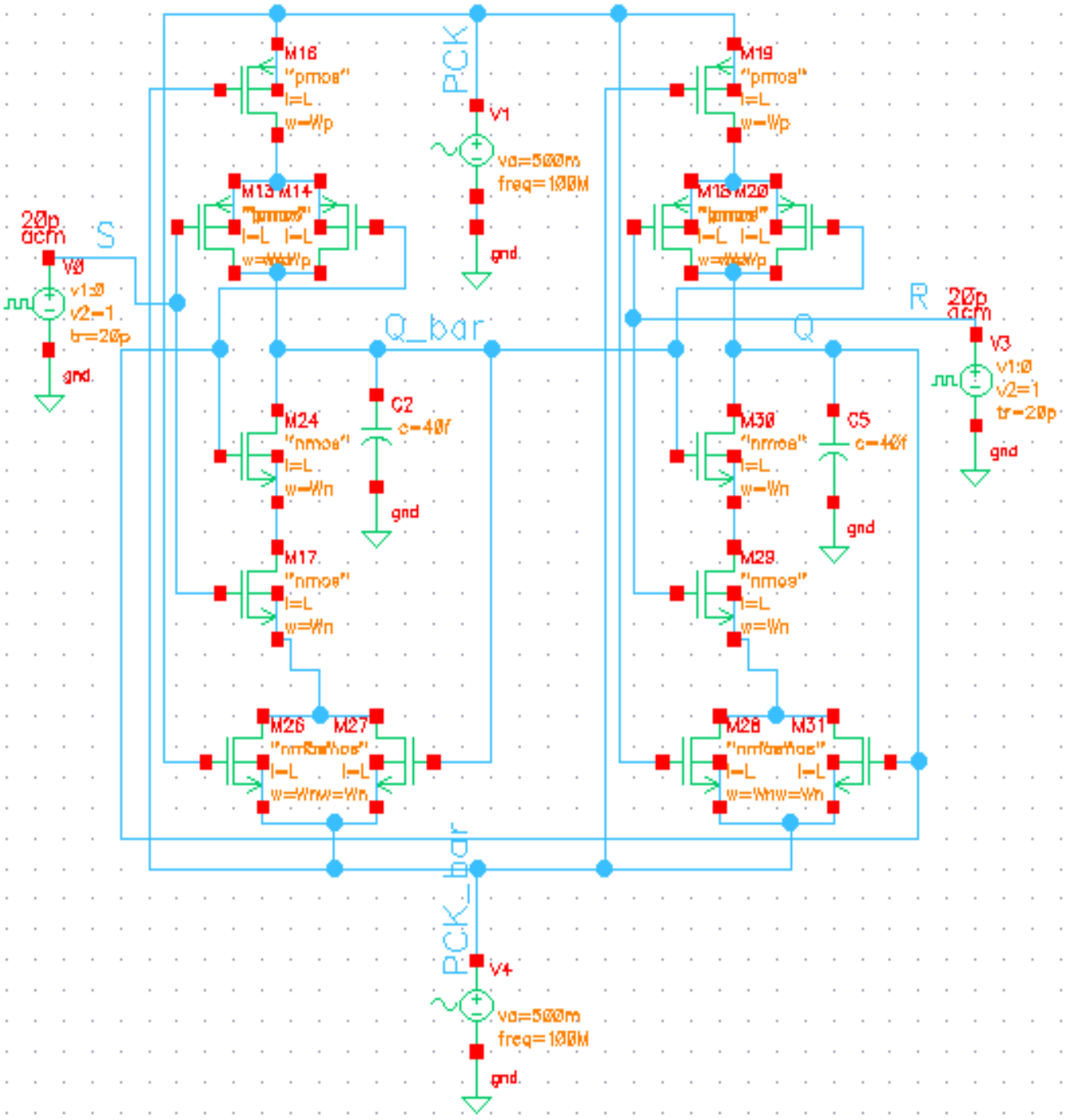

Fig. 3.18: IDFAL SR Flip-Flop.

This is owing to fact that, in addition to being universal, i.e., capable of mimicking any of the other conventional logic functions, it is also less expensive to build. The SR is composed of the components Set and Reset, denoted S and R, respectively. The device is comprised of four terminals, with R and S designated as inputs and Q and Q_bar as outputs. The diagram of an IDFAL SR flip-flop is illustrated in Fig. 3.18. This flip-flop features cross-coupled NAND gates, where output of one gate is allied with input of opposite gate, and vice versa. The waveform of output is illustrated in Fig. 3.19 (Sasipriya & Bhaaskaran, 2018; Ng & Lau, 2000).

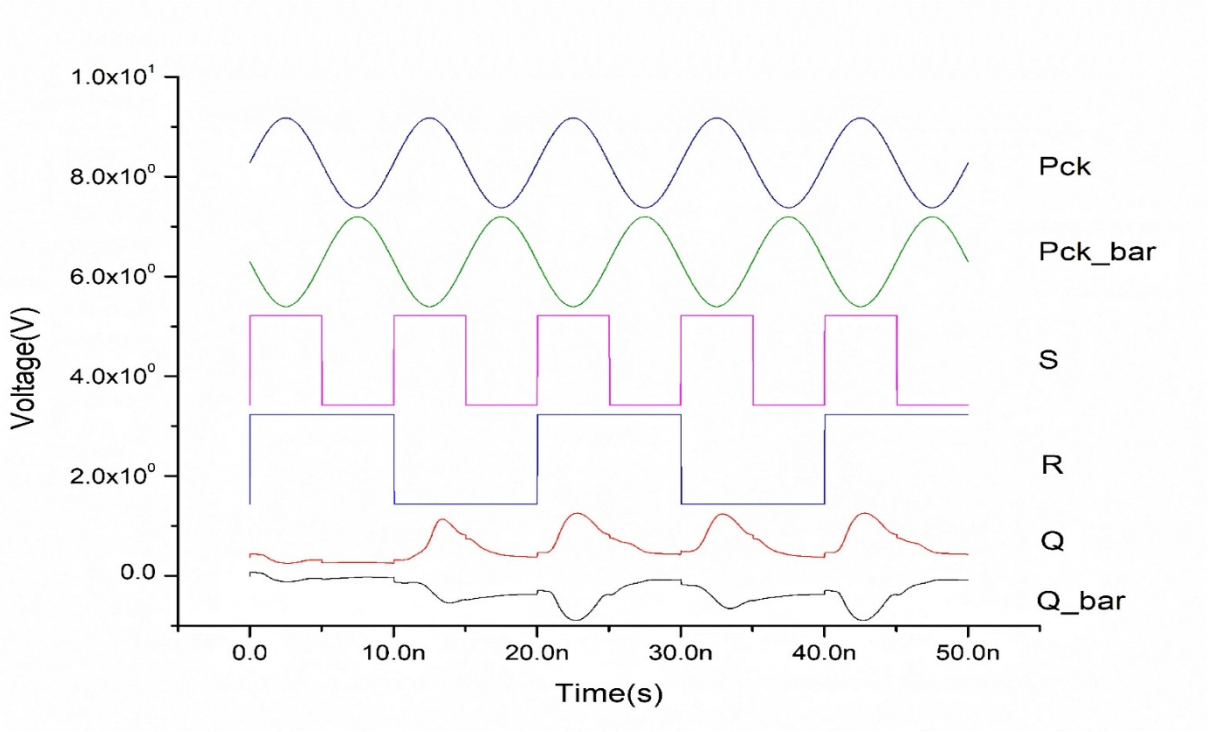

Fig. 3.19: Waveform of IDFAL SR Flip-Flop.

3.5. RESULTS AND DISCUSSIONS

The power consumption of each circuit is evaluated using the Cadence Virtuoso analog design environment, as shown in Fig. 3.20. Several CMOS technology nodes, their respective power supplies $V_{DD}(V)$, the channel length $L(nm)$, the channel width for PMOS $W_p(nm)$, the channel width for NMOS $W_n(nm)$, and aspect ratios are illustrated in Table 3.1 as presented in (Bhushan & Ketchen, 2014).

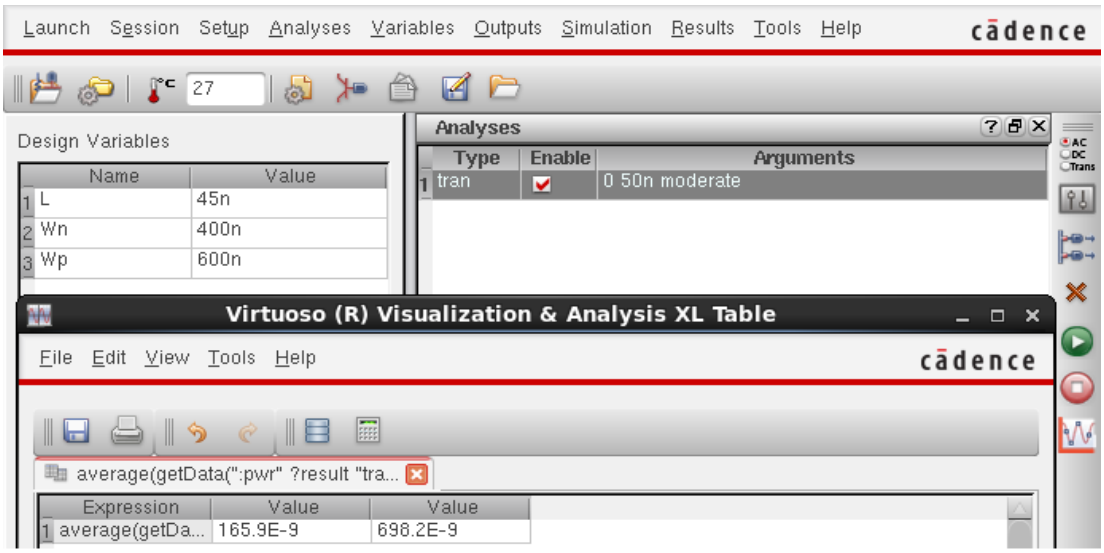

Fig. 3.20: Analog design environment showing simulation parameters and the result of average power consumption in the analysis XL table.

In all analyses, the load capacitor is fixed at $C_L = 0.01pf$. TSMC stands for Taiwan Semiconductor Manufacturing Company Limited, and HP_PTM. The evaluation of the inverter circuit's average power consumption at various switching frequencies, from 20 MHz up to 800 MHz, is depicted in Table 3.2.

Table 3.1: Different CMOS Technology Nodes, Their Respective Power Supplies, Parameters,and Aspect (Bhushan & Ketchen, 2015)

CMOS Technology Nodes	$V_{DD}(V)$	$L(nm)$	$W_p(nm)$	$W_n(nm)$	$\frac{W_p}{L}$	$\frac{W_n}{L}$
180nm_TSMC	1.8	180	800	400	4.444	2.222
45nm_HP_PTM	1	45	600	400	13.333	8.888
32nm_HP_PTM	0.9	32	420	280	13.125	8.75
22nm_HP_PTM	0.8	22	300	200	13.636	9.090
16nm_HP_PTM	0.7	16	225	150	14.062	9.375

The CMOS technology employed 180n TSMC. From Table 3.2, it can be seen that the IDFAL circuit consumed the least average power at several operating frequencies when compared to CMOS and other adiabatic logic circuits. Table 3.3 represents the leakage current and leakage power associated with CMOS and adiabatic circuits at 100 MHz using 180 nm TSMC technology.

Simulation results show that ADCL has the best leakage power savings. However, it has the slowest logic transitions, as mentioned earlier in Section 3.2. The IDFAL comes in second place in leakage power saving. Each analysis was done within four cycles of the operating frequency.

Table 3.2: Comparison of 180 nm TSMC Inverter Power Consumption at Various Operating Frequency Within Four Clock Periods or Cycle Times of Their Respective Inputs

180nm_TSMC: Average Power Consumption in (µW)							
Logics/ Freq.	**20 MHz**	**50 MHz**	**100 MHz**	**200 MHz**	**400 MHz**	**500 MHz**	**800 MHz**
CMOS	0.8279	2.111	4.254	8.556	17.14	21.42	34.34
2PASCL	0.5298	1.222	2.422	4.494	5.640	5.888	6.370
DFAL	0.02421	0.0676	5.505	5.883	6.708	7.195	8.653
CCAL	0.02765	0.07434	0.1697	0.4043	1.054	1.422	2.740
ADCL	0.1277	0.2035	0.3393	0.6406	1.297	1.634	2.608
2PADCL	0.2404	0.3175	0.4407	0.7067	1.314	1.645	2.702
ADCL	0.5663	0.7546	0.9722	1.409	2.368	2.885	4.541
IDFAL	0.02673	0.07054	0.1595	0.3836	0.9765	1.328	2.599

Table 3.3: Leakage Current and Leakage Power Measurements Within 40 nm Simulation Time, at a Frequency of 100 MHz

Basic Inverter using 180nm_TSMC_Model		
Circuit Design	**Total Leakage Current (A)**	**Leakage Power (W)**
CMOS	23.7838E-12	4.28E-11
2PASCL	24.6459653E-27	2.22E-26
DFAL	12.65461E-27	1.14E-26
IDFAL	8.261607E-27	7.44E-27
CCAL	13.8382E-27	1.25E-26
2PADCL	14.16858 E-27	1.28E-26
ADCL	1.63267E^37	1.47E-37
QSERL	17.5636E-27	1.58E-26

Table 3.4: Comparison of 45nm_HP_PTM Inverter Circuits' Power Consumptions at Several Operating Frequencies Within Four Clock Periods or Cycle Times of Their Respective Inputs

45nm_HP_PTM: Average Power Consumption in (nW)							
Logics/Freq.	**20 MHz**	**50 MHz**	**100 MHz**	**200 MHz**	**400 MHz**	**500 MHz**	**800 MHz**
CMOS	239.3	530	1175u	2344	4671	5835	9353
2PASCL	117	160	220.9	305	401.5	436	509.7
DFAL	38.41	59.91	95.30	169.7	329.4	420.1	712.9
CCAL	37.41	58.42	91.71	161	313.2	398.2	677.5
2PADCL	44.58	91.6	144.9	205.4	266.4	290.6	350.9
QSERL	53.64	115.4	196.7	302.5	420.5	455.2	539.2
IDFAL	35.72	54.51	84.13	145.2	284.8	362.3	619.5

Tables 3.4 and 3.5 present the average power consumption of inverter circuits designed with conventional CMOS and several adiabatic logic techniques at various frequencies using 45 nm HP_PTM and 32 nm HP_PTM technology, respectively, and the load capacitor is kept at $C_L = 0.01pf$ for each analysis. From these two tables, it can be noted that at every operating frequency, the proposed circuit, IDFAL, consumes the least power when compared with CMOS and other design methods. 2PADCL and QSERL, unlike other adiabatic logic styles, use full-scale V_{DD} and consume significant power. To maintain fair comparisons, their V_{DD} amplitudes are scaled down to half of each corresponding input logic.

Table 3.5: Comparison of 32nm_HP_PTM Inverter Circuits' Power Consumptions at Various Operating Frequency Within Four Clock Periods or Cycle Times of Their Respective Inputs

32nm_HP_PTM: Average Power Consumption in (nW)							
Logics/Freq.	**20 MHz**	**50 MHz**	**100 MHz**	**200 MHz**	**400 MHz**	**500 MHz**	**800 MHz**
CMOS	191.4	463.6	917.2	1825	3639	4545	7265
2PASCL	51.03	69.04	86.82	106.2	135	148.6	193.6
DFAL	10.78	23.16	43.75	88.29	186.8	245.3	431
CCAL	10.49	22.57	42.31	84.53	180.4	236	417.7
2PADCL	27.62	46.24	60.28	76.08	102.6	116.5	161
QSERL	33.63	62.98	88.72	114.3	146.4	160.9	209.3
IDFAL	10.07	21.24	39.89	79.98	172.8	223.5	403.7

Table 3.6: 16nm_HP_PTM: Performance Comparison of Basic Gates Designed Using Conventional CMOS and Various Adiabatic Logic Techniques Within 40nm Simulation Time at 100 MHz operating frequency

16nm_HP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (µW)**	**Delays (ns)**	**PDP (fJ)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	NOT	0.5931	0.025375	0.01505	23.724	0.601997
	AND	0.7391	0.03055	0.02258	29.564	0.90318
	NAND	0.6314	0.03391	0.021411	25.256	0.856431
	OR	0.6905	0.031405	0.021685	27.62	0.867406
	NOR	0.5871	0.05938	0.034862	23.484	1.39448
	XOR	0.599	0.057495	0.03444	23.96	1.37758
	XNOR	0.7721	0.0353	0.027255	30.884	1.090205
2PASCL	NOT	0.03084	0.248425	0.007661	1.2336	0.306457
	AND	0.1496	0.65926	0.098625	5.984	3.945012
	NAND	0.03668	0.4913	0.018021	1.4672	0.720835
	OR	0.1515	0.41896	0.063472	6.06	2.538898
	NOR	0.05149	0.305885	0.01575	2.0596	0.630001
	XOR	0.07571	0.740575	0.056069	3.0284	2.242757
	XNOR	0.2058	0.689325	0.141863	8.232	5.674523
DFAL	NOT	0.01987	0.184635	0.003669	0.7948	0.146748
	AND	0.1019	0.26804	0.027313	4.076	1.092531
	NAND	0.0218	0.49841	0.010865	0.872	0.434614
	OR	0.08856	0.274625	0.024321	3.5424	0.972832
	NOR	0.02601	0.49899	0.012979	1.0404	0.519149
	XOR	0.04735	0.513905	0.024333	1.894	0.973336
	XNOR	0.1229	0.52634	0.064687	4.916	2.587487
CCAL	NOT	0.0198	0.1851	0.003665	0.792	0.146599
	AND	0.05627	0.550115	0.030955	2.2508	1.238199
	NAND	0.0218	0.496755	0.010829	0.872	0.43317
	OR	0.06011	0.558125	0.033549	2.4044	1.341956
	NOR	0.02644	0.49896	0.013193	1.0576	0.5277
	XOR	0.04441	0.50829	0.022573	1.7764	0.902926
	XNOR	0.08673	0.574785	0.049851	3.4692	1.994044
ADCL	NOT	0.6438	1.596875	1.028068	25.752	41.12273
	AND	0.3664	1.78331	0.653405	14.656	26.13619
	NAND	0.5888	1.62494	0.956765	23.552	38.27059
	OR	0.3661	1.20688	0.441839	14.644	17.67355
	NOR	0.6500	1.576235	1.024553	26	40.98211
	XOR	0.5858	1.539065	0.901584	23.432	36.06337
	XNOR	0.4545	1.81871	0.826604	18.18	33.06415
IDFAL	NOT	0.02032	0.098214	0.001995	0.8128	0.014804
	AND	0.05102	0.55361	0.028245	2.0408	1.129807
	NAND	0.0216	0.497765	0.010752	0.864	0.430069
	OR	0.05006	0.622652	0.03117	2.0024	1.246798
	NOR	0.02717	0.500635	0.013602	1.0868	0.54409
	XOR	0.04403	0.91763	0.040403	1.7612	1.61613
	XNOR	0.08024	0.768695	0.06168	3.2096	2.467203

Table 3.7: 22nm_HP_PTM: Performance Comparison of Basic Gates Designed Using Conventional CMOS and Various Adiabatic Logic Techniques Within 40nm Simulation Time at 100 MHz operating frequency

22nm_HP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (µW)**	**Delays (ns)**	**PDP (fJ)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	NOT	0.7203	0.02196	0.015818	28.812	0.632712
	AND	0.8454	0.027515	0.023261	33.816	0.930447
	NAND	0.7602	0.028345	0.021548	30.408	0.861915
	OR	0.8319	0.02923	0.024316	33.276	0.972657
	NOR	0.7430	0.032065	0.023824	29.72	0.952972
	XOR	1.528	0.04772	0.072916	61.12	2.916646
	XNOR	1.748	0.031705	0.05542	69.92	2.216814
2PASCL	NOT	0.04018	0.250305	0.010057	1.6072	0.40229
	AND	0.2092	0.95675	0.200152	8.368	8.006084
	NAND	0.03648	0.652725	0.023811	1.4592	0.952456
	OR	0.2006	0.45423	0.091119	8.024	3.644742
	NOR	0.05448	0.317415	0.017293	2.1792	0.691711
	XOR	0.08992	0.693325	0.062344	3.5968	2.493751
	XNOR	0.2687	0.57786	0.155271	10.748	6.210839
DFAL	NOT	0.02812	0.136815	0.003847	1.1248	0.15389
	AND	0.1295	0.213595	0.027661	5.18	1.106422
	NAND	0.03065	0.210245	0.006444	1.226	0.25776
	OR	0.1088	0.210245	0.022875	4.352	0.914986
	NOR	0.04106	0.486115	0.01996	1.6424	0.798395
	XOR	0.08055	0.498055	0.040118	3.222	1.604733
	XNOR	0.1703	0.20248	0.034482	6.812	1.379294
CCAL	NOT	0.0277	0.124238	0.003441	1.108	0.137656
	AND	0.0967	0.556875	0.05385	3.868	2.153993
	NAND	0.03030	0.480715	0.014566	1.212	0.582627
	OR	0.09424	0.54746	0.051593	3.7696	2.063705
	NOR	0.04182	0.48544	0.020301	1.6728	0.812044
	XOR	0.07501	0.49861	0.037401	3.0004	1.496029
	XNOR	0.1513	0.56643	0.085701	6.052	3.428034
ADCL	NOT	0.8630	1.05551	0.910905	34.52	36.43621
	AND	0.4892	1.63573	0.800199	19.568	32.00796
	NAND	0.8243	1.489945	1.228162	32.972	49.12647
	OR	0.4846	1.63807	0.793809	19.384	31.75235
	NOR	0.8711	1.48886	1.296946	34.844	51.87784
	XOR	0.8298	1.54444	1.281576	33.192	51.26305
	XNOR	0.8488	2.14977	1.824725	33.952	72.98899
IDFAL	NOT	0.02727	0.121255	0.003307	1.0908	0.132265
	AND	0.08781	0.556735	0.048887	3.5124	1.955476
	NAND	0.02942	0.482085	0.014183	1.1768	0.567318
	OR	0.07977	0.54513	0.043485	3.1908	1.739401
	NOR	0.04079	0.48572	0.019813	1.6316	0.792501
	XOR	0.07345	0.498005	0.036578	2.938	1.463139
	XNOR	0.1369	0.56737	0.077673	5.476	3.106918

Table 3.8: 32nm_HP_PTM: Performance Comparison of Basic Gates Designed Using Conventional CMOS and Various Adiabatic Logic Techniques Within 40nm Simulation Time at 100 MHz operating frequency

32nm_HP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (µW)**	**Delays (ns)**	**PDP (fJ)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	NOT	0.9173	0.018435	0.01691	36.692	0.676417
	AND	1.107	0.024255	0.02685	44.28	1.074011
	NAND	0.9727	0.02249	0.021876	38.908	0.875041
	OR	1.101	0.02465	0.02714	44.04	1.085586
	NOR	0.9676	0.02535	0.024529	38.704	0.981146
	XOR	2.06	0.03327	0.068536	82.4	2.741448
	XNOR	2.419	0.028765	0.069583	96.76	2.783301
2PASCL	NOT	0.08971	0.182035	0.01633	3.5884	0.0586
	AND	0.2946	0.41308	0.121693	11.784	1.434035
	NAND	0.08974	0.33411	0.029983	3.5896	0.107627
	OR	0.2792	0.40878	0.114131	11.168	1.274619
	NOR	0.1284	0.38277	0.049148	5.136	0.252422
	XOR	0.09225	0.66875	0.061692	3.69	0.227644
	XNOR	0.3051	0.52788	0.161056	12.204	1.96553
DFAL	NOT	0.04548	0.058405	0.002656	1.8192	0.004832
	AND	0.1770	0.16109	0.028513	7.08	0.201872
	NAND	0.05458	0.4592	0.025063	2.1832	0.054718
	OR	0.1559	0.159075	0.0248	6.236	0.154652
	NOR	0.07206	0.459175	0.033088	2.8824	0.095373
	XOR	0.1548	0.460115	0.071226	6.192	0.44103
	XNOR	0.2612	0.158025	0.041276	10.448	0.431253
CCAL	NOT	0.04395	0.05475	0.002406	1.758	0.00423
	AND	0.1756	0.4116	0.072277	7.024	0.507673
	NAND	0.05307	0.45824	0.024319	2.1228	0.051624
	OR	0.1414	0.351055	0.049639	5.656	0.280759
	NOR	0.0728	0.461825	0.033621	2.912	0.097904
	XOR	0.1478	0.459605	0.06793	5.912	0.4016
	XNOR	0.2675	0.426695	0.114141	10.7	1.221308
ADCL	NOT	1.095	0.77826	0.852195	43.8	34.08779
	AND	0.6844	1.48207	1.014329	27.376	40.57315
	NAND	1.112	1.151985	1.281007	44.48	51.24029
	OR	0.6808	1.44728	0.985308	27.232	39.41233
	NOR	1.098	1.089485	1.196255	43.92	47.85018
	XOR	1.253	1.377665	1.726214	50.12	69.04857
	XNOR	0.6932	1.476595	1.023576	27.728	40.94303
IDFAL	NOT	0.04118	0.026435	0.001089	1.6472	0.043544
	AND	0.1641	0.55094	0.090409	6.564	3.61637
	NAND	0.04954	0.45983	0.02278	1.9816	0.911199
	OR	0.1233	0.527955	0.065097	4.932	2.603874
	NOR	0.06873	0.459355	0.031571	2.7492	1.262859
	XOR	0.1412	0.459165	0.064834	5.648	2.593364
	XNOR	0.1745	0.552825	0.096468	6.98	3.858719

Table 3.9: 45nm_HP_PTM: Performance Comparison of Basic Gates Designed Using Conventional CMOS and Various Adiabatic Logic Techniques Within 40nm Simulation Time at 100 MHz operating frequency

45nm_HP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (µW)**	**Delays (ns)**	**PDP (fJ)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	NOT	1.175	0.01547	0.018177	47	0.72709
	AND	1.911	0.033095	0.063245	76.44	2.529782
	NAND	1.585	0.024655	0.039078	63.4	1.563127
	OR	2.272	0.0293	0.06657	90.88	2.662784
	NOR	1.881	0.0229	0.043075	75.24	1.722996
	XOR	3.311	0.02785	0.092211	132.44	3.688454
	XNOR	3.865	0.044745	0.172939	154.6	6.917577
2PASCL	NOT	0.2243	0.122625	0.027505	8.972	1.100192
	AND	0.4265	0.32725	0.139572	17.06	5.582885
	NAND	0.2423	0.280	0.067844	9.692	2.71376
	OR	0.3938	0.32015	0.126075	15.752	5.043003
	NOR	0.3068	0.36121	0.110819	12.272	4.432769
	XOR	0.2395	0.477755	0.114422	9.58	4.576893
	XNOR	0.4435	0.39865	0.176801	17.74	7.072051
				0	0	0
DFAL	NOT	0.09727	0.016934	0.001647	3.8908	0.065887
	AND	0.2946	0.07738	0.022796	11.784	0.911846
	NAND	0.1475	0.435245	0.064199	5.9	2.567946
	OR	0.260	0.075955	0.019748	10.4	0.789932
	NOR	0.138	0.430915	0.059466	5.52	2.378651
	XOR	0.1407	0.43634	0.061393	5.628	2.455722
	XNOR	0.291	0.53899	0.156846	11.64	6.273844
				0	0	0
CCAL	NOT	0.09347	0.011255	0.001052	3.7388	0.04208
	AND	0.306	0.149335	0.045697	12.24	1.82786
	NAND	0.1439	0.43466	0.062548	5.756	2.501903
	OR	0.2301	0.13778	0.031703	9.204	1.268127
	NOR	0.1483	0.429615	0.063712	5.932	2.548476
	XOR	0.1422	0.436765	0.062108	5.688	2.484319
	XNOR	0.2978	0.17288	0.051484	11.912	2.059347
ADCL	NOT	1.289	1.133005	1.460443	51.56	58.41774
	AND	0.9435	1.326875	1.251907	37.74	50.07626
	NAND	1.327	1.088025	1.443809	53.08	57.75237
	OR	0.9325	1.3277	1.23808	37.3	49.52321
	NOR	1.282	0.979645	1.255905	51.28	50.2362
	XOR	1.593	1.115345	1.776745	63.72	71.06978
	XNOR	1.214	1.377435	1.672206	48.56	66.88824
IDFAL	NOT	0.08636	0.0241	0.002081	3.4544	0.083251
	AND	0.3033	0.17625	0.053457	12.132	2.138265
	NAND	0.1348	0.435755	0.05874	5.392	2.349591
	OR	0.2451	0.1778	0.043579	9.804	1.743151
	NOR	0.1380	0.430915	0.059466	5.52	2.378651

	XOR	0.7018	0.43689	0.306609	28.072	12.26438
	XNOR	0.2835	0.1766	0.050066	11.34	2.002644
2PADCL	NOT	0.1482	0.21792	0.032296	5.928	1.29183
	AND	0.2446	0.5668	0.138639	9.784	5.545571
	NAND	0.1842	0.398625	0.073427	7.368	2.937069
	OR	0.2097	0.9725	0.203933	8.388	8.15733
	NOR	0.2142	0.63476	0.135966	8.568	5.438624
	XOR	0.2594	0.81845	0.212306	10.376	8.492237
	XNOR	0.1884	0.545265	0.102728	7.536	4.109117
QSERL	NOT	0.200	0.557685	0.111537	8	4.46148
	AND	0.2902	0.84652	0.24566	11.608	9.826404
	NAND	0.2369	0.9684	0.229414	9.476	9.176558
	OR	0.2416	0.76274	0.184278	9.664	7.371119
	NOR	0.3812	0.501355	0.191117	15.248	7.644661
	XOR	0.2444	0.814785	0.199133	9.776	7.965338
	XNOR	0.249	0.6600015	0.16434	9.96	6.573615

Table 3.10: Comparative Analysis of the Average Power Usage of Fundamental Logic Gates, Constructed with the IDFAL Methodology at Different Technology Nodes.

Dynamic Power Dissipation of the proposed technique IDFAL (µW)				
Circuits	**45nm_HP_PTM**	**32nm_HP_PTM**	**22nm_HP_PTM**	**16nm_HP_PTM**
NOT gate	0.08636	0.04118	0.02727	0.02032
AND gate	0.3033	0.1641	0.08781	0.05102
NAND gate	0.1348	0.04954	0.02942	0.0216
OR gate	0.2451	0.1233	0.07977	0.05006
NOR gate	0.1380	0.06873	0.04079	0.02717
XOR gate	0.7018	0.1412	0.07345	0.04403
XNOR gate	0.2835	0.1745	0.1369	0.08024

Tables 3.6, 3.7, 3.8, and 3.9 show the average power consumption, circuit delay, PDP, energy consumption, and EDP (Dadoria & Khare, 2019) of basic logic gates NOT, AND, NAND, OR, NOR, and XNOR using different CMOS technology nodes, namely 16 nm HP_PTM, 22 nm HP_PTM, 32 nm HP_PTM, and 45 nm HP_PTM. Simulations are performed within four clock cycles at 100 MHz. It should be noted that all power supply voltages except for CMOS and ADCL are scaled to half of their corresponding input voltages, and the load capacitor is fixed at $0.01pf$ for all simulations. According to observation tables 3.6, 3.7, 3.8, and 3.9, the average power consumption, PDP, energy consumption, and EDP of the proposed IDFAL circuit at 16 nm

HP_PTM, 22 nm HP_PTM, 32 nm HP_PTM, and 45 nm HP_PTM outperformed their counterpart traditional CMOS and adiabatic logic design styles used in the work. Table 3.10 also presents the average power consumption of basic logic gates designed using IDFAL. Figure 3.21 depicts the average power savings of numerous adiabatic logic circuits as compared to standard CMOS. The comparative evaluations are carried out on inverter circuits at various CMOS technology nodes. The bar graph shows that the power savings of 2PASCL, CCAL, DFAL, and IDFAL over CMOS at 45 nm HP_PTM are 80.9%, 92%, 91.7%, and 92.6%, respectively. whereas the power savings in 32nm HP_PTM are 90.02 %, 95.2 %, 95 %, and 95 %. In the same way, in 22nm HP_PTM, the power savings are 94.4%, 96.1%, 96.2%, and 96.2%, respectively. Similarly, the power savings of the aforementioned adiabatic logic circuits over traditional CMOS at 16 nm HP_PTM are 94.8%, 96.6%, and 96.5%. IDFAL provides better power savings and optimization in all scenarios.

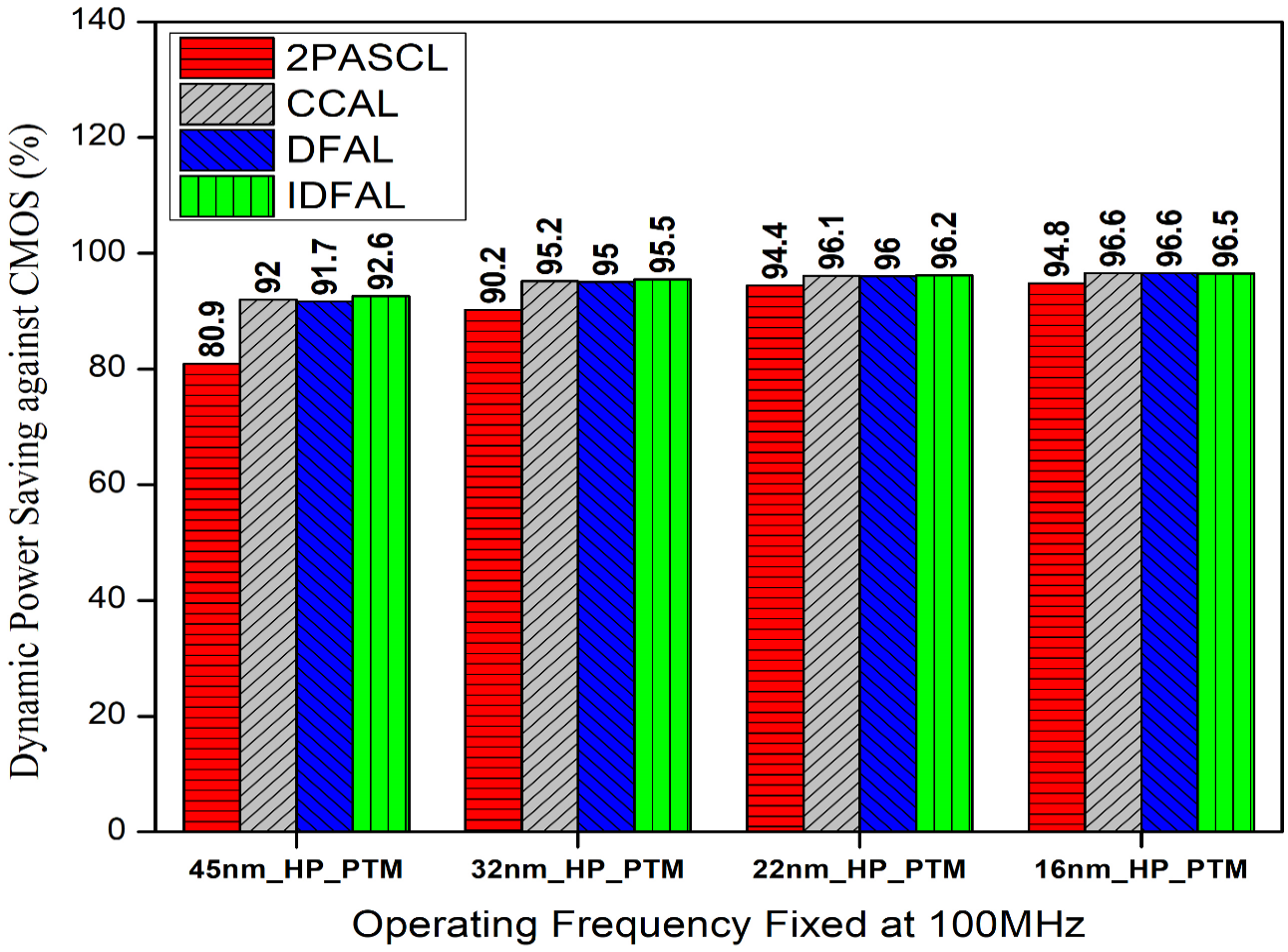

Fig. 3.21: Dynamic power saving of adiabatic inverter circuits against conventional CMOS at a fixed frequency of 100 MHz

3.6. SUMMARY

In this chapter, an IDFAL is presented. IDFAL utilized two control transistors, resulting in the minimization of output node floating. The control transistors and complementary split-level power clocks reduce the leakage current and leakage power. A parallel additional transistor across the pull-down network reduced the discharging resistance and hence lessened the dynamic power consumption. To validate the feasibility of the circuit, an extensive analysis was carried out at various technology nodes, such as 180 nm TSMC, 45 nm, 32 nm, 22 nm, and 16 nm HP_PTM. Besides circuit delay, average, and leakage power consumption, assessments were performed with other aspects such as PDP and EDP on basic gates like NOT, AND, OR, NAND, NOR, XOR, XNOR, and XOR circuits. Furthermore, the IDFAL circuit diagrams and simulation waveforms of a combinational circuit (a NAND gate) and a sequential circuit (an SR flip-flop) are shown to represent the feasibility and versatility of the IDFAL circuit. Fig. 3.28 shows that IDFAL saves an average power of 92.6%, 95.5%, 96.2%, and 96.5% against CMOS at 45nm, 32nm, 22nm, and 16nm HP_PTM nodes. Observation tables, graphs, analysis results, and comparative performance evaluations exhibit its superiority over CMOS and the reported literature. IDFAL has better power savings and optimization than CMOS and the mentioned adiabatic logic families. Hence, the IDFAL is considered advantageous for future trends in low-power VLSI circuit implementations.

CHAPTER-4

Sequential and Combinational Circuits With Improved Diode Free Adiabatic Logic (IDFAL)

4.1. Introduction

Low-power design has been a prominent topic in VLSI system design community due to the increasing need for energy efficiency in modern electronic systems. This requirement may be attributed to the fact that electronic systems are becoming more complex. Electronic devices, both portable and immovable, can be found just about everywhere in today's society. Since the introduction of VLSI technology, numerous industries and companies have endeavoured to develop devices that are both high-performing and inexpensive (Ye & Roy, 1996; Athas et al., 1994; Li et al., 2013; Oklobdzija et al., 1997; Nayan et al., 2012). At first glance, it can appear as though our modern culture is wholly dependent on portable technological gadgets. It is becoming more and more obvious that a significant problem for both high-performance and portable applications is the amount of power that they consume. Several studies are being done on a variety of different design approaches with the goal of cutting down on power consumption (Yuejun et al., 2018; Han et al., 2019). Adiabatic switching-based energy recovery circuits have shown great potential as a very effective method for designing low-power devices (Ye & Roy, 1996; Gong et al., 2008; Upadhyay et al., 2013; Brzozowski, 1971; Bakopoulos et al., 2012; Abdul et al., 2022; Askarian & Akbarizadeh, 2022; Roa & Jung, 2013). Although there are several ways to measure a product's effectiveness and efficiency, the two most common are its operational speed and power consumption (battery life) (Khatir et al., 2011; Li et al., 2013; Kumar et al., 2019). An adiabatic logic design technique should be adopted and advised when power consumption, rather than processing speed, is the key issue in our circuit design. The appeal of the adiabatic design approach is increased as a result of the possibility of low-frequency powering of smart cards, RFIDs, and sensors (Kumar et al., 2019; Anuar et al., 2010). It has been shown that an adiabatic circuit may be kept running using an AC power source rather than a DC one, since the longer transition of the AC power supply's output during charging and discharging stops heat from escaping the circuit. As the system enters an adiabatic phase, energy is also conserved since the charge held in the load capacitor is released (Blotti et al., 2010; Bhaaskaran & Raina, 2010). Over time, several different adiabatic circuits have

been developed (Ye & Roy, 1996; Athas et al., 1994; Oklobdzija et al., 1997; Khatir et al., 2011). Output voltage deterioration, silicon area utilization, and floating outputs are only some of the issues that have bothered adiabatic logic families (Chanda et al., 2018; Gong et al., 2008; Starosel'skii, 2001). Other issues include pipelining problems, transmission delays, the requirement for several sophisticated cloaking systems, and floating outputs. Degradation of the output voltage amplitude is caused by voltage drops in the diode during charging and discharging of the load capacitor (Dickinson & Denker, 1995; Dickinson & Denker, 1994; Takahashi & Mizunuma, 2000). Based on existing static CMOS logic, an IDFAL is designed structurally (Ye & Roy, 1996; Anuar et al., 2010; Ye & Roy, 2001). A complementary sinusoidal power clock was utilized in the logic. By lowering the peak current across the transistors, the split-level power supply helps conserve energy. Further, control transistors are included in the circuit to cut down on leakage power (Ye & Roy, 1996; Li et al., 2013; Sasipriya & Bhaaskaran, 2018; Sasipriya & Bhaaskaran, 2018).

4.2. Work Involving Adiabatic Logic Families

The CCAL (Li et al., 2013), 2PASCL (Nayan et al., 2012; Anuar et al., 2010), DFAL (Upadhyay et al., 2013; Kumar & Kumar, 2020; Kumar & Kumar, 2022), 2PADCL (Takahashi et al., 2006), QSERL (Ye & Roy, 2001), and ADCL (Takahashi & Mizunuma, 2000) are examples of well-known adiabatic logic families employed as references in this work. The IDFAL inverter schematic and inverter circuit diagrams for the reference adiabatic logic circuits used in this chapter are shown in Figs. 4.1–4.7. The power consumption and signal propagation times of the proposed design, IDFAL, are compared to those of conventional CMOS logic and the aforementioned reference logics. The energy optimization of the diode-based circuit for energy recovery would decrease if the quotient of $\left(\frac{V_{th}}{V_{dd}}\right)$ were not maintained during the scaling of V_{dd} (Ye & Roy, 2001). The energy that the diode dissipates at each logic transition is approximated (Ye & Roy, 2001), as shown below,

$$E_D = CV_{th}(V_{dd} - V_{th}) \tag{4.1}$$

MOS technology scaling and power supply scaling for reduction of power consumption have huge drawbacks and limitations since there is an issue with this approach since it may cause a considerable increase in leakage current (Kumar et al., 2011). Consequently, on scaling down the technology, conservation of the relation $\left(\frac{V_{th}}{V_{dd}}\right)$is not practicable and diode-based energy recovery

circuits such as QSERL, ADCL, 2PASCL, and 2PADCL have run into this problem. In addition, the output voltage would float during different hold phases in 2PADCL, QSERL, and 2PASCL circuits. While using a single clock power source in an ADCL circuit saves energy, it also causes a significant degree of gate delay (Anuar et al., 2010). In contrast to diode-base logics, time-control transistors are used in IDFAL, DFAL, and CCAL designs. These control transistors, or regulating transistors, limit node switching by ensuring that the output wave tracks the supply signal throughout its whole cycle. Clock control transistor-based circuits like these have been shown to function at very high frequencies (Li et al., 2013; Ye & Roy, 2001; Sasipriya et al., 2018).

Two control transistors, as shown in Fig. 4.1, are included in the IDFAL and are linked to both the networks. In addition, the IDFAL circuit reduces power utilization compared to DFAL because of the parallel transistor M_5, which also leads to a decreased resistance to capacitor discharge. Throughout the hold phase, control transistors are deactivated, isolating the output from V_{clk} and $\overline{V_{clk}}$. Therefore, production remains unchanged during this phase. As a result, there is less output floating for half of a clock cycle, making it more robust against noise and leakage current.

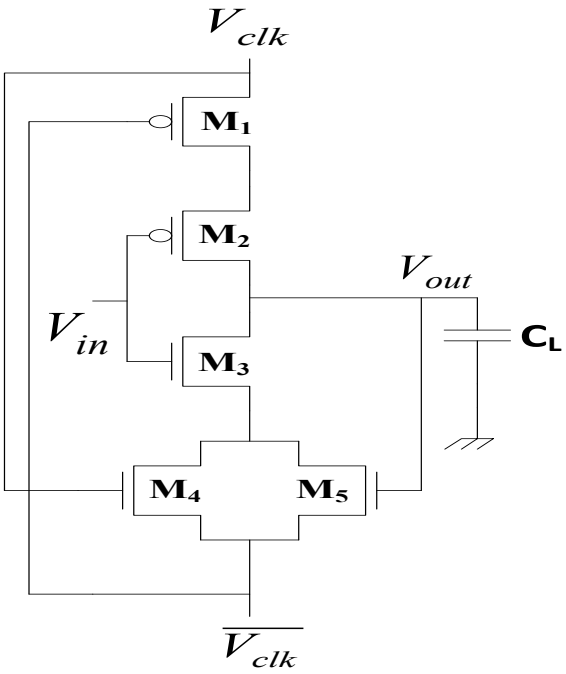

Fig.4.1: Basic Inverter of IDFAL

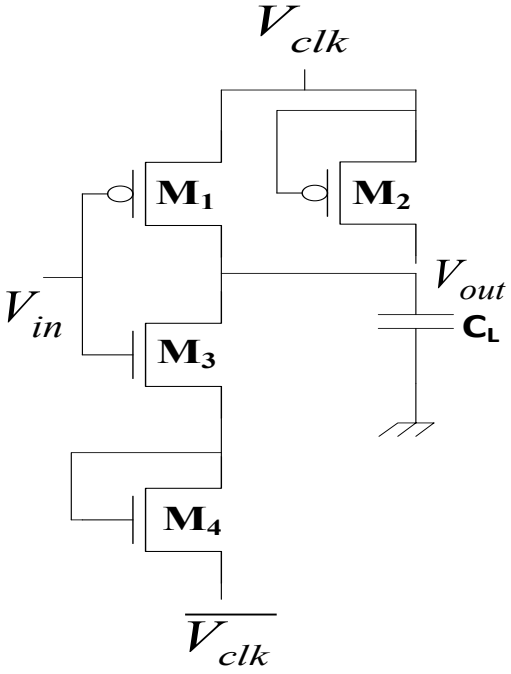

Fig.4.2: Basic Inverter of 2PASCL

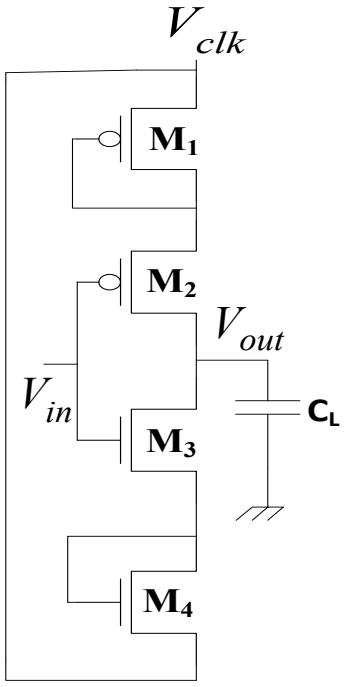

Fig.4.3: Basic Inverter of ADCL

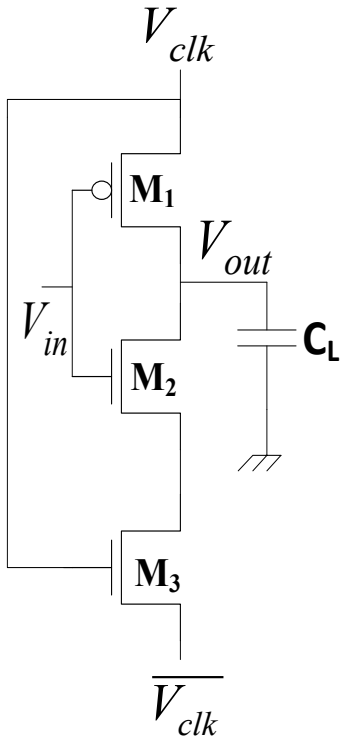

Fig.4.4: Basic Inverter of DFAL

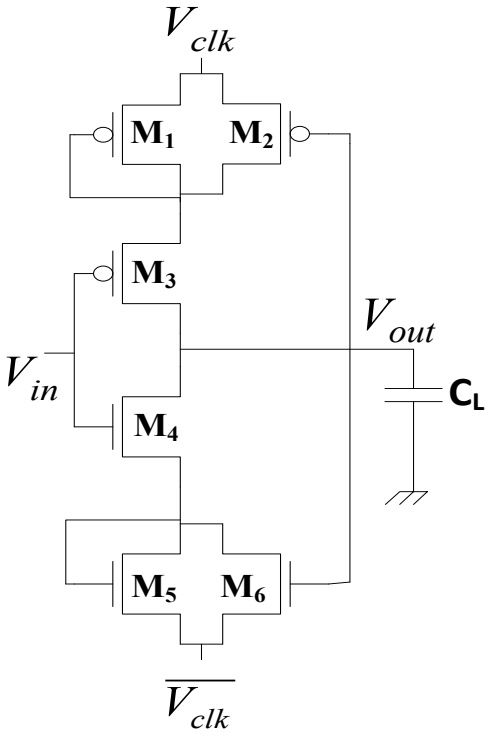

Fig.4.5: Basic Inverter of QSERL

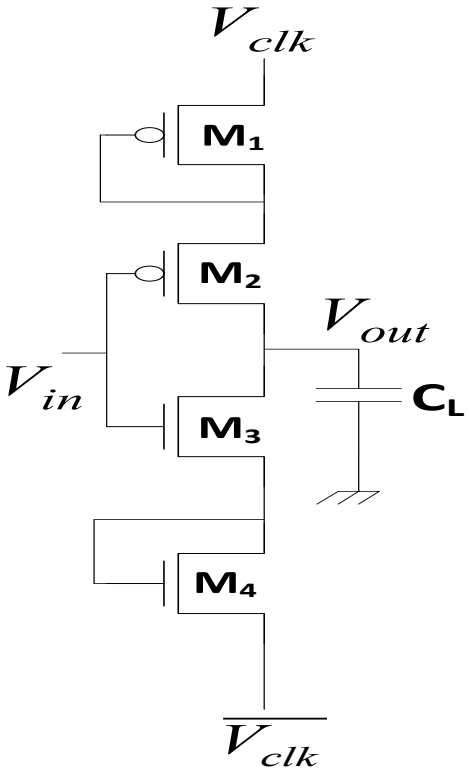

Fig.4.6: Basic Inverter of 2PADCL

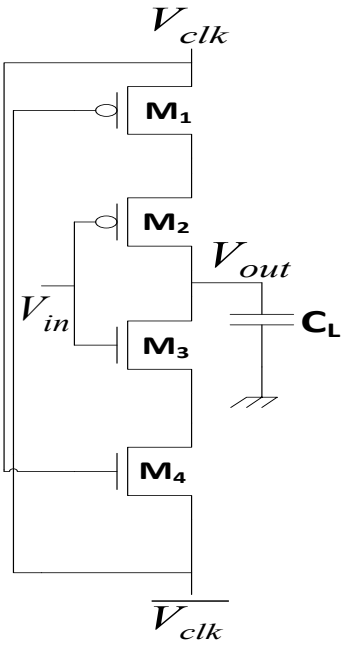

Fig.4.7: Basic Inverter of CCAL

4.3. Analyzing the IDFAL Circuit

Referring section 3.3.2, and considering all starting conditions of the circuit are zero and all ON-resistances of charging and discharging transistors are identical and indicated by R, then the total amount of energy consumed by an IDFAL circuit is given as,

$$E_{IDFAL} = \left(\frac{RC_L}{2T}\right) C_L \left(V_{clk_{p-p}} - V_{ctl}\right)^2$$
$$+C_L \left(\frac{V_{clk_{p-p}} - V_{ctl}}{2}\right) (V_{ctl} + V_{PDT}) + C_L {V_{th}}^2 + E_{leak} \quad (4.2)$$

The leakage energy is also approximated as (Hu, Ye, & Su, 2010):

$$E_{leak} = I_{leak} \frac{V_{DD} \cos\left(\frac{2\theta + 3\pi w}{2}\right) - V_{DD} \cos\left(\frac{2\theta + \pi w}{2}\right) + \pi V_{DD} w}{4w} \quad (4.3)$$

By utilizing the Kirchhoff voltage law (KVL) along the charging path of the RC equivalent of the IDFAL circuit illustrated in Fig.3.10, the transfer function can be calculated as follows:

$$V_{clk} = V_{ctl} + i.R + \frac{1}{C_L} \int i.dt$$

$$V_{clk}(s) = V_{ctl}(s) + R.I(s) + \frac{1}{C_L s} I(s)$$

$$\Rightarrow I(s)\left\{R+\frac{1}{C_L s}\right\}=V_{clk}(s)-V_{ctl}(s)$$

$$\Rightarrow I(s)=\frac{V_{clk}(s)-V_{ctl}(s)}{\left\{R+\frac{1}{C_L s}\right\}}$$

(4.4)

$$V_o(s)=\frac{1}{C_L s}I(s)$$

$$I(s)=\frac{V_o(s)}{\frac{1}{C_L s}}$$

$$\frac{\mathrm{V_o(s)}}{\frac{1}{\mathrm{C_L s}}}=\frac{\mathrm{V_{clk}(s)-V_{ctl}(s)}}{\mathrm{R+\frac{1}{C_L s}}} \tag{4.5}$$

$$\mathrm{LetZ(s)}=\frac{\mathrm{V_{ctl}(s)}}{\mathrm{V_{clk}(s)}}$$

$$AndH(s)=\frac{V_o(s)}{V_{clk}(s)}$$

$$H(s)=\left(\frac{\frac{1}{C_L s}}{R+\frac{1}{C_L s}}\right).\left(1-Z(s)\right) \tag{4.6}$$

4.3.1. Simulation of Basic IDFAL Inverter Circuit

An analog design environment in Cadence Virtuoso is used to determine how much power each circuit consumes and how long it takes for signals to propagate across it. The fundamental IDAFL inverter circuit with parameters $C_L = 10pf$ and $V_{in} = 1V$ at 45nm LP_PTM is shown in Fig. 4.8. In this arrangement, the representations PCK (power clock) and $PCKb$ (power clock bar) are used in place of V_{clk} and $\overline{V_{clk}}$, and the peak voltage for each power supply is set to 0.5V since it employs the split-level power supply. The simulation time is set to 40 ns at a frequency of 400 kHz. The input voltage and power supply frequency must be twice or more than doubled for traditional adiabatic energy recovery logic circuits, the IDFAL circuit could run and function properly under the same frequency of both the input and complementary power supplies V_{clk} and $\overline{V_{clk}}$.

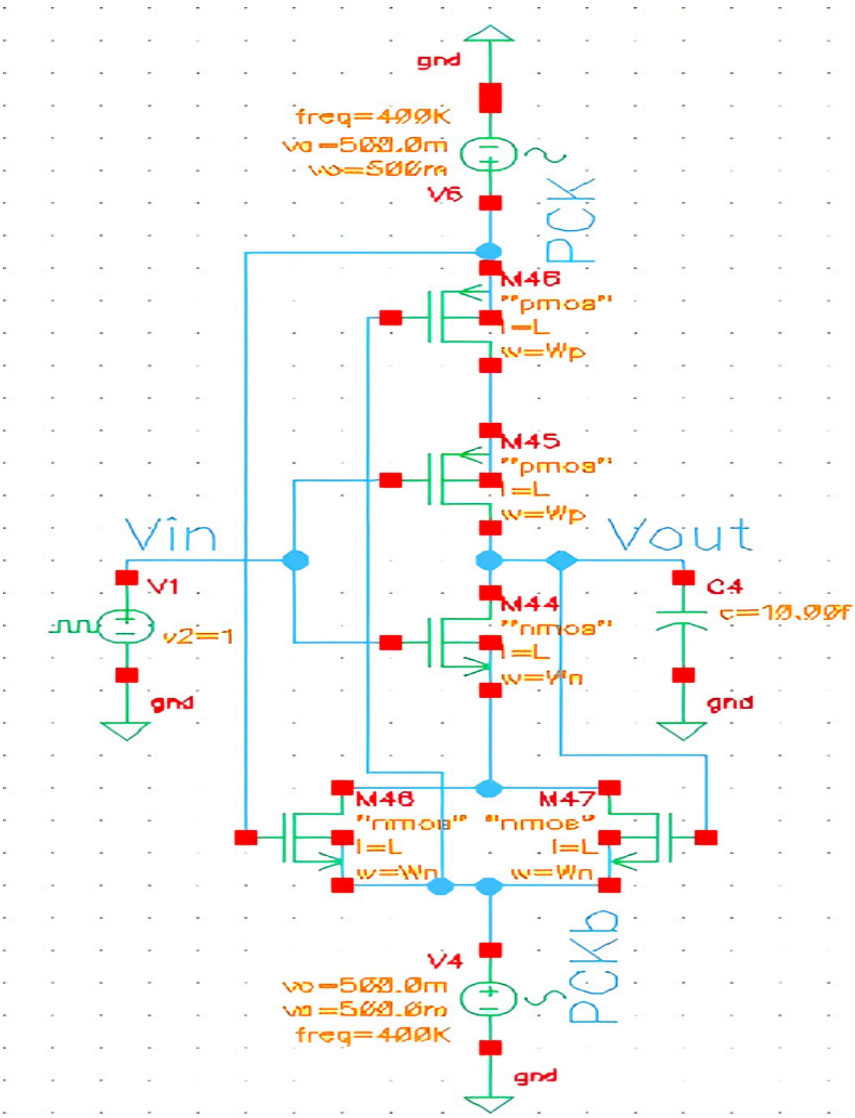

Fig.4.8: Basic Inverter Circuit.

Thus, in the case of IDFAL, the input frequency and complementary power supply frequencies are preserved at the same value. When using certain static adiabatic logic techniques, some power clock frequencies need to be twice as fast as input frequency in order to get the anticipated output voltage swing and undistorted amplitude. This lowers the energy consumption raises the dynamic power consumption. The input and output waveforms of the IDFAL inverter are depicted in Fig. 4.9. The propagation delays of a circuit can be easily evaluated using the tools provided by the software. While examining the power consumption and the propagation delay of each circuit, we do not provide a DC offset voltage to the complementary power clocks in any simulations.

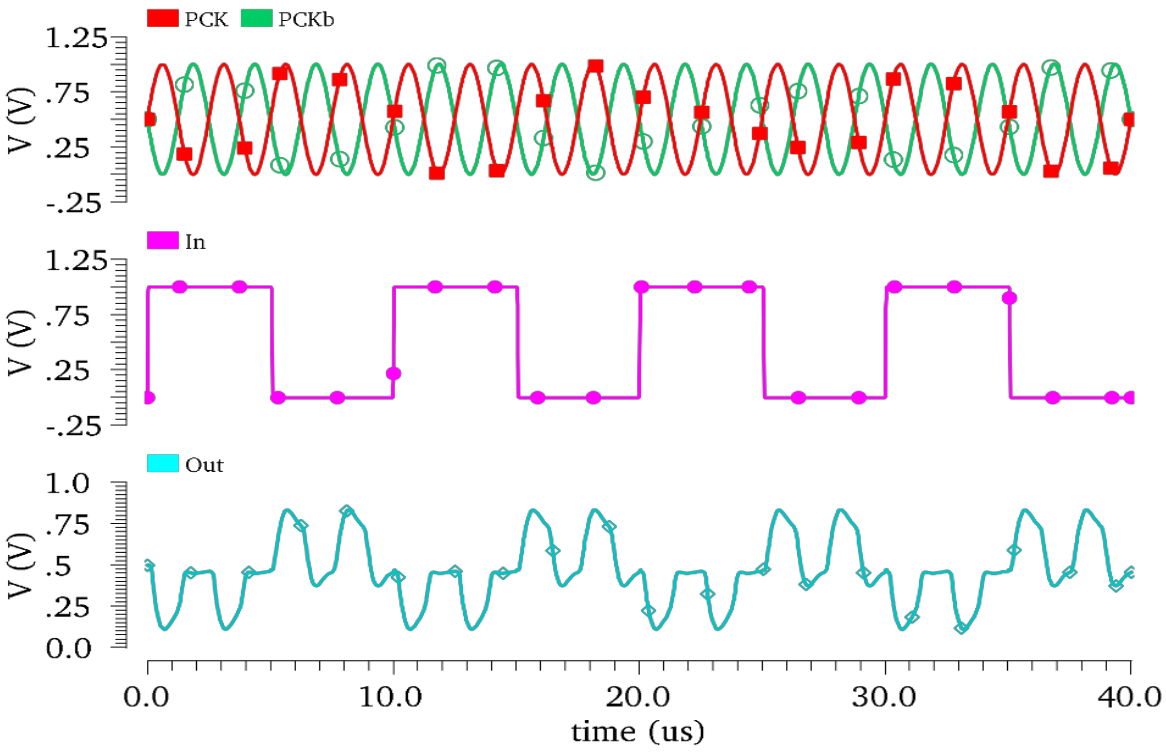

Fig.4.9: Waveform of the IDFAL Inverter Circuit.

4.4. The IDFAL Sequential Circuits.

The term "sequential" describes the sequence in which things happen; in a sequential circuit, a clock signal from outside the system controls timing of these occurrences. The input state determines the output of a flip-flop, making it a memory element in sequential circuits. Unlike combinational logic circuits, which change states depending on the current signals sent into them, sequential logic circuits include an internal "memory" that lets them hold onto a prior state. This means that sequential circuits are able to consider both the current and previous input states; this is known as a "before and after" influence. Another way of putting it is that the current, previous, and/or future states of the inputs and/or outputs of a sequential logic circuit determine its output. Until a fresh clock signal deviations, the circuits may remember the current situation and stay in that state (Challa et al., 2019; Brzozowski, 1971). Computer memory is based on the flip-flop, often known as a bi-stable circuit. A single bit may be stored in this volatile memory so long as the power supply is active.

4.4.1. SR Flip-flop Using IDFAL

One of the simplest sequential circuits, the SR flip-flop, may be built using two-input NOR gates or NAND gates; the latter is more popular due to its adaptability. This is due to the fact that, in addition to being universal, i.e., capable of mimicking any of the other conventional logic functions, it is also less expensive to build. The letters S and R in the SR represent set and reset, respectively. The four-terminal device accepts inputs from R and S and outputs from Q and Q_Bar. Fig. 4.10 depicts the logic design of an SR flip-flop employing a NAND latch, and Table 4.1 illustrates the truth table of the same. The IDFAL SR flip-flop, seen in Fig. 4.11, is designed using two NAND gates that are cross-coupled.

Table 4.1: Truth Table of an SR Flipflop

CLK	S	R	Q	Q_Bar
1	0	0	Q	Qb
1	0	1	0	1
1	1	0	1	0
1	1	1	x	X
0	x	x	x	X

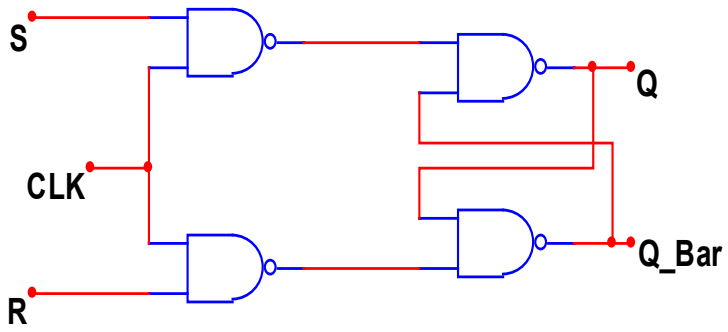

Fig.4.10: SR Flip-Flop Logic Diagram.

In Fig. 4.12, we can see the output waveform. Equation (4.7) below shows the characteristic equation of an SR flip-flop. According to Challa et al. (2019), Brzozowski (1971), and Kacprzak (1988).

Characteristic equation:

$$Q^+ = S + \overline{R}Q \tag{4.7}$$

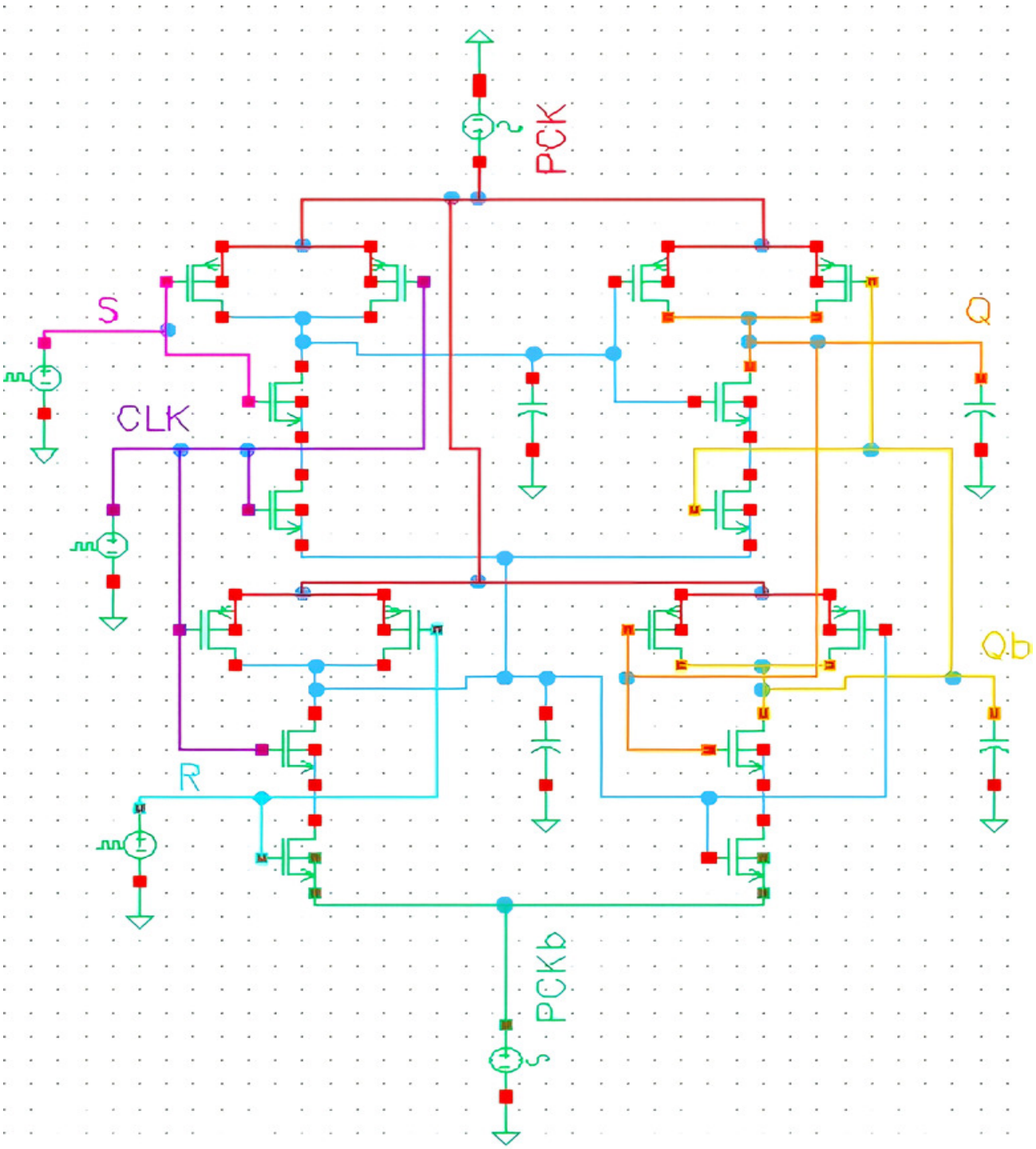

Fig.4.11: IDFAL SR Flip-Flop

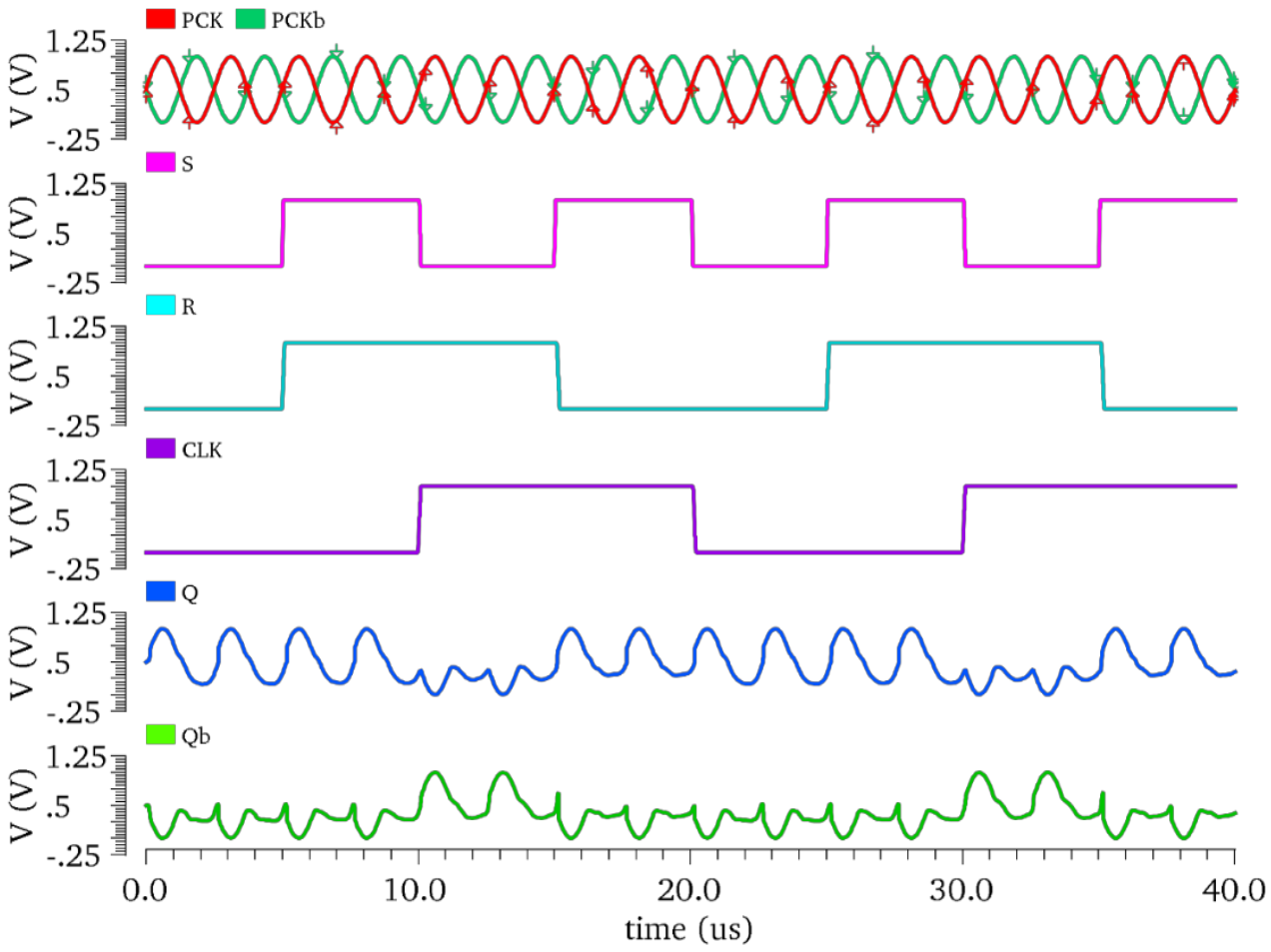

Fig.4.12: Waveform of IDFAL SR Flip-Flop

4.4.2. D Flip-flop Using IDFAL

In order to create D flip-flop, an inverter circuit, or NOT gate, is inserted across the S and R ends. This ensures that any logic input to the R terminal match up to the antithesis of the logic input to the S terminal. A clock (CLK) and data (D) are the two inputs that the D flip-flop accepts. The oscillator, which is a timed pulse produced by the circuit, is utilized for function control. Data is recorded and maintained for a predetermined period of time using the D flip-flop. Thus, prior to transmitting the input data, a latency of up to one clock pulse is introduced. A countdown timer can be generated by connecting D flip-flops in a chain and employing external combinational logic gates appropriately. The exclusive structural element comprising a shift register is a D flip-flop. The effective structure of a shift register that facilitates data transmission in two distinct directions—

from right to left or left to right—is possible by cascading a number of D-flip-flops. Both serial and parallel inputs and outputs are supported. Table 4.2 presents the truth table of a D flip flop, whereas Figs. 4.13, 4.14, and 4.15 illustrate the logic diagram and simulated waveforms of a D flip flop, which were implemented using the IDFAL approach. The characteristic equation of the D flip-flop is given in Eq. (4.8) (Chandrasekaran et al., 2005; Saw et al., 2017).

Table 4.2: Truth Table of a D Flipflop

CLK	D	Q	Q_Bar
1	0	0	1
1	1	1	0
0	x	x	X

Characteristic equation:

$$Q^+ = D \tag{4.8}$$

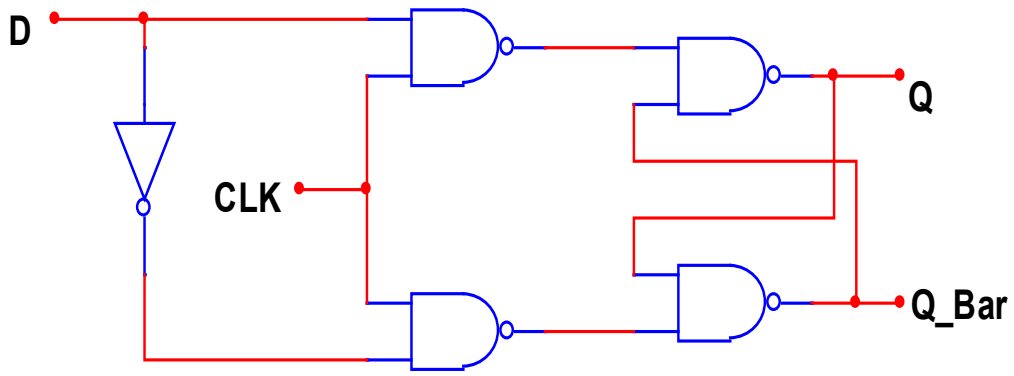

Fig.4.13: D Flip-Flop Logic Diagram

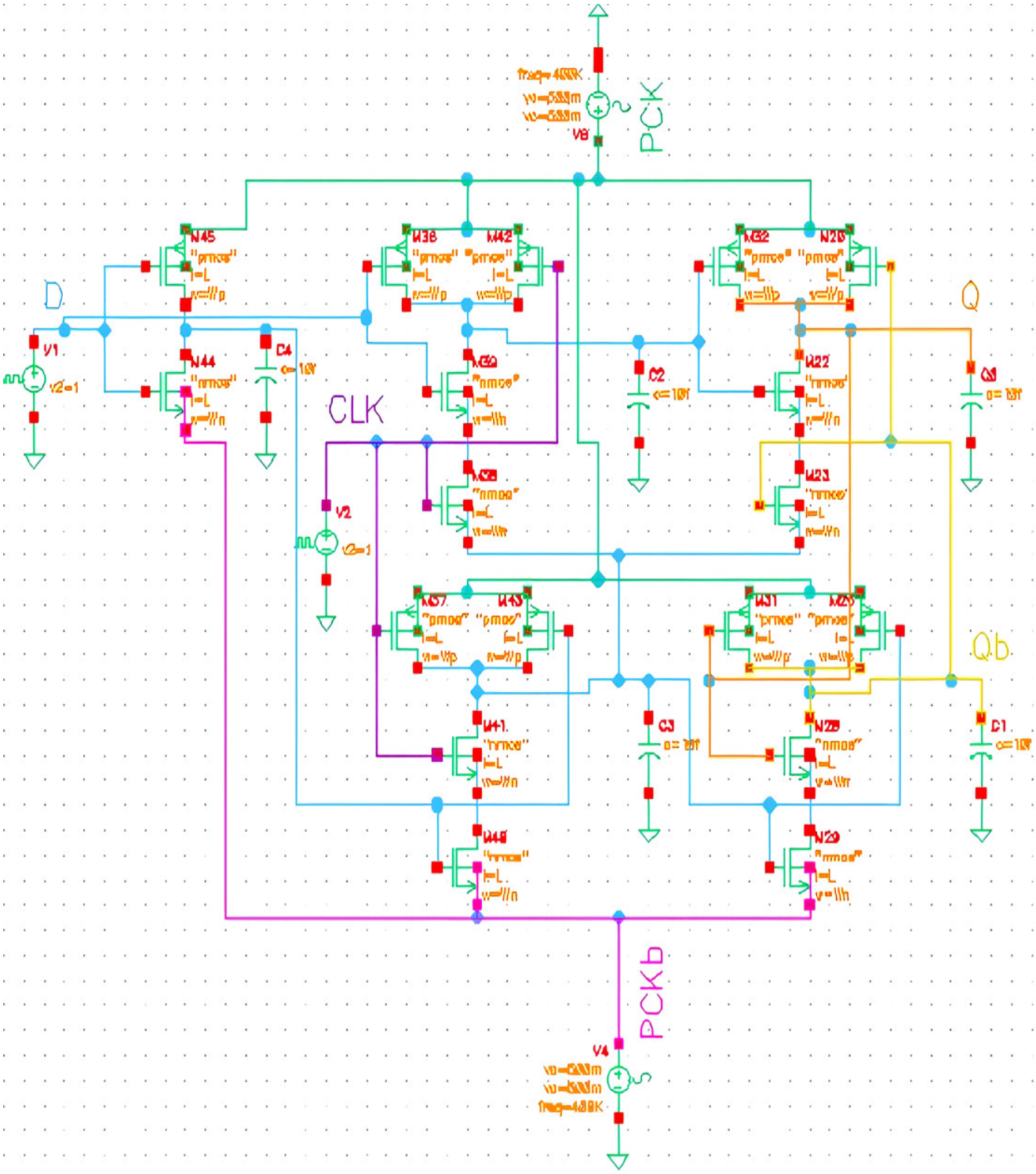

Fig.4.14: IDFAL D Flip-Flop

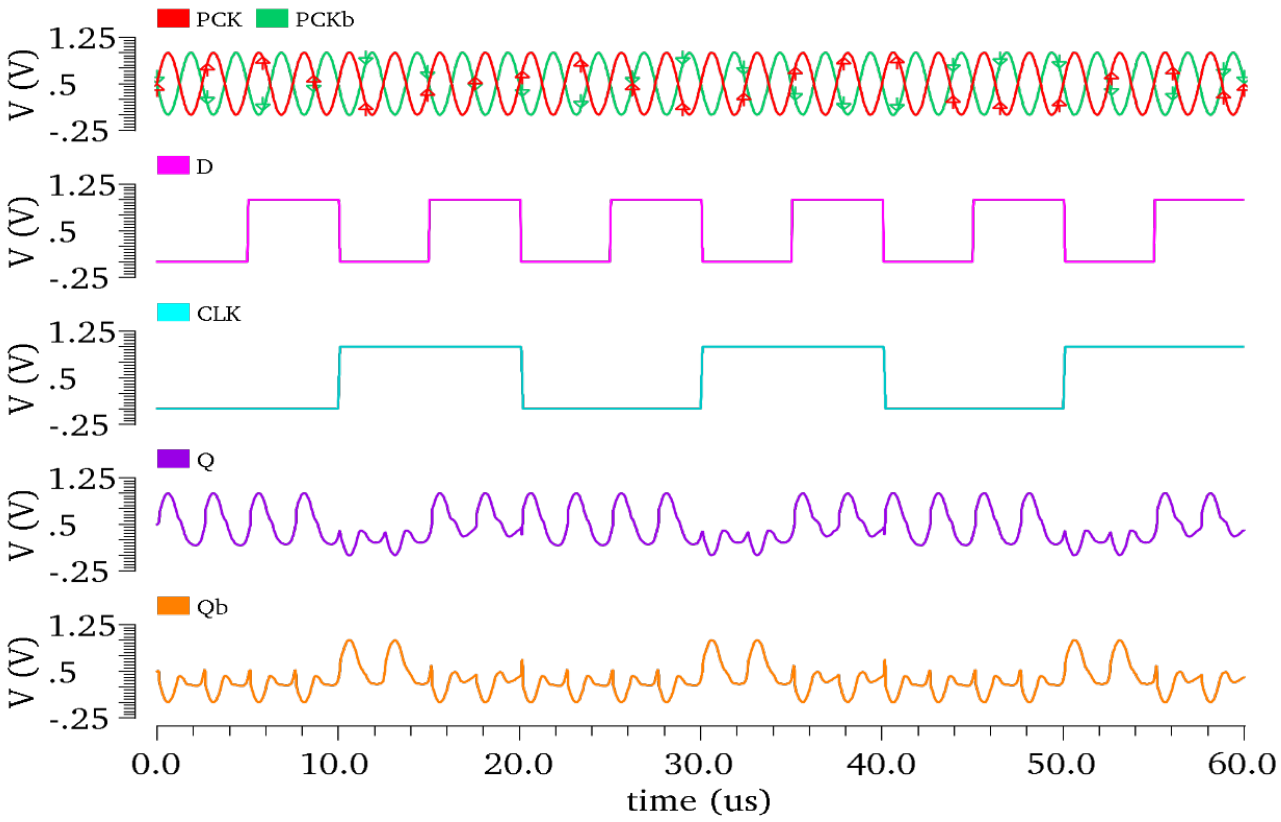

Fig.4.15: Waveform of IDFAL D Flip-Flop

4.4.3. T Flip-flop Using IDFAL

T-flip-flop is one of the essential types of flip-flops. Data storage is the main function of Flip Flop. By connecting the J and K terminals of a JK flip flop to one another, we may create a T-flip flop. This kind of flip-flop has one input, T, and one clock input, CLK. Toggling refers to the process by which an output transitions from one state to another in response to an appropriate clock input.

Table 4.3: Truth Table of a T Flipflop

CLK	T	Q (prev)	Qb (Prev)	Q (Next)	Qb (Next)
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	0	1

The subsequent expression illustrates the fundamental equation that defines a T flip-flop.

$$Q^{+} = \overline{T}Q + T\overline{Q} = T \oplus Q \qquad (4.9)$$

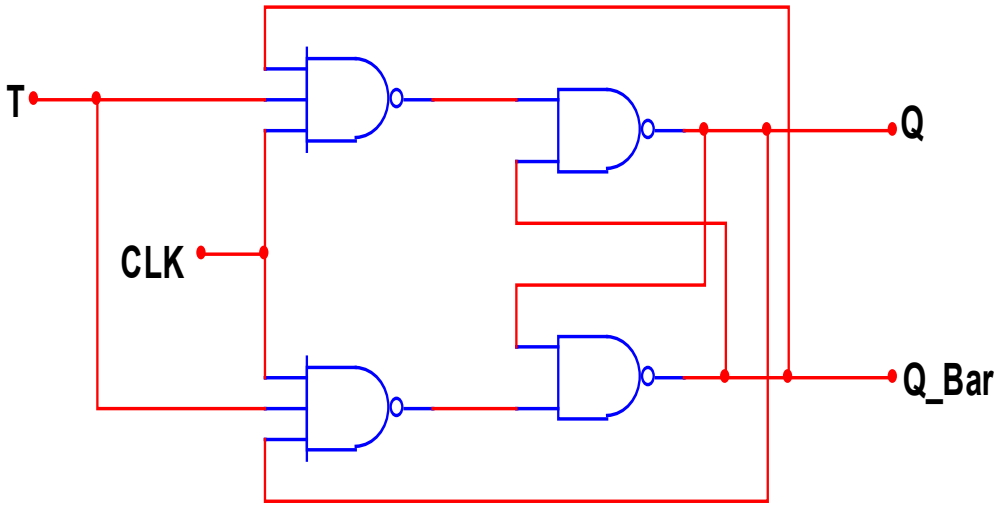

Fig.4.16: T Flip-Flop Logic Diagram

Whenever CLK is logic HIGH, the circuits operate. In a T-flip flop, the middle letter "T" represents the toggle. Since this is the case, the T-flip flop may be thought of as a switch. An example of a toggle is entering a reverse state. In this case, the frequency of the output is half that of the signal at the T input. Since it splits the input frequency in half, resulting in an output frequency that is half of the input frequency, the T-Flip Flop essentially serves as a frequency divider. On the plus side, it modifies the current output state whenever the clock input is activated. Due to their small size, they find use in Minecraft pistons. In addition, this flip-flop works well for counters. In contrast, knowing the prior state of the flip-flop is necessary in order to determine its current state. They can only be created from SR or JK flip flops since integrated circuits containing them do not exist. The truth table of a T flip flop is shown in Table 4.3, while the logic diagram, realization of a T flip flop using the IDFAL approach, and simulated waveforms of an IDFAL-based T flip flop (Figs. 4.16, 4.17, and 4.18) (Chen et al., 1999; Bakopoulos et al., 2012).

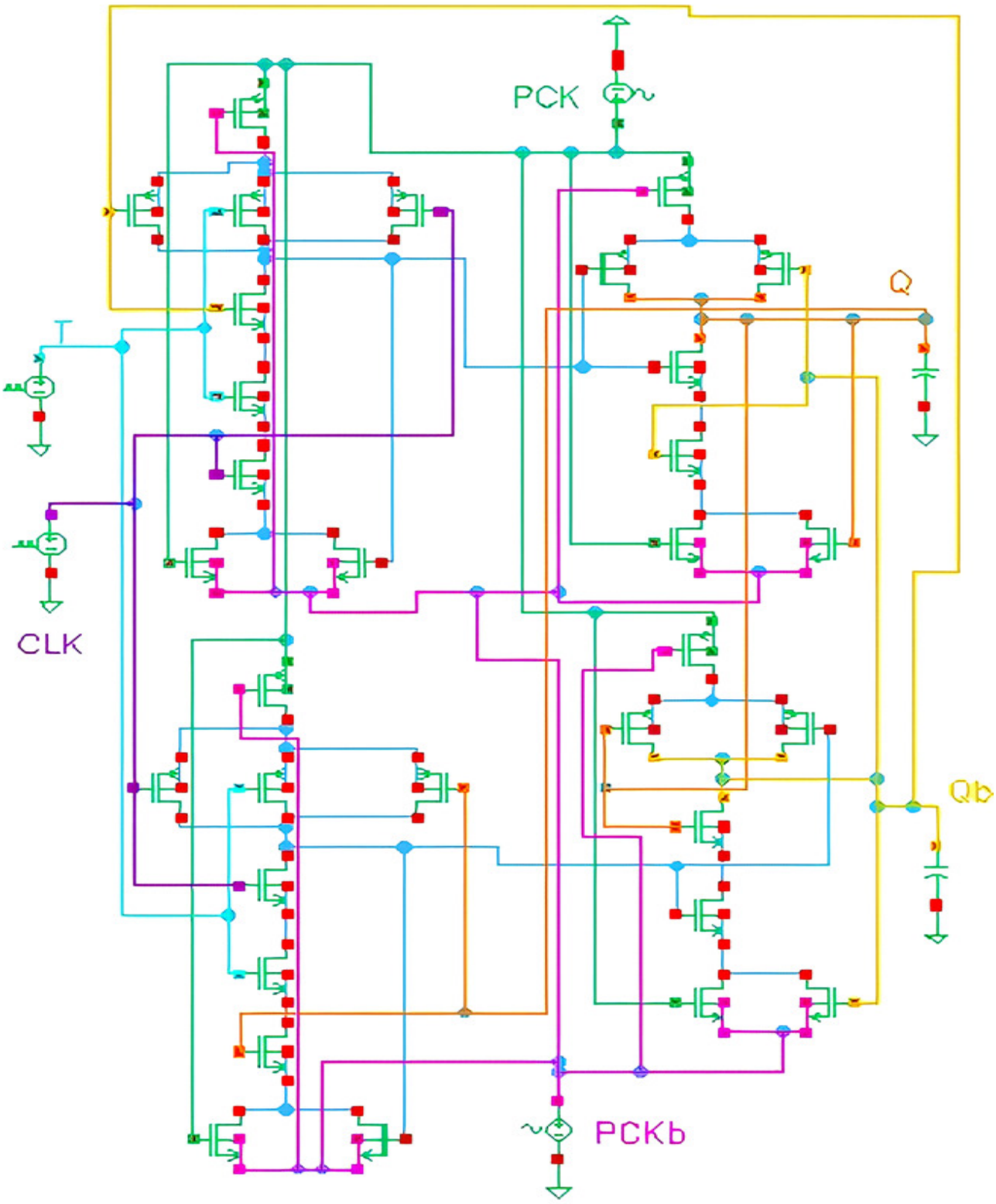

Fig.4.17: IDFAL T Flip-Flop

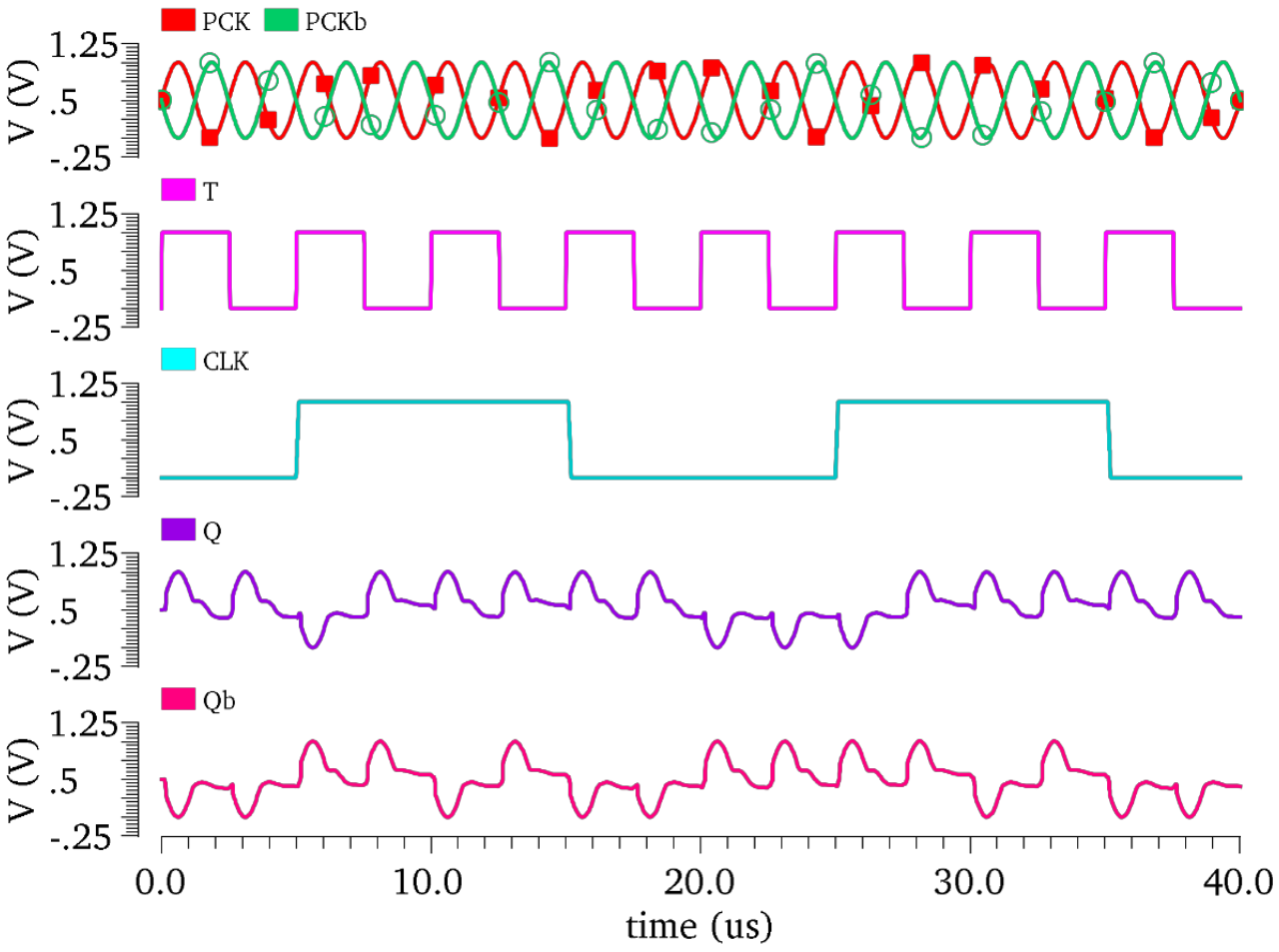

Fig.4.18: Waveform of IDFAL T Flip-Flop

4.5. The IDFAL Combinational Circuits.

For digital circuits, a combinational circuit is one whose output is sensitive to both the present input and the history of that input. Therefore, it is possible to think of the output of a combinational circuit as being a function of all the inputs, both closely and distantly preceding it. An alternate circuit design is a sequential circuit. Not only does the current input influence the output of a sequential circuit, but so does the state of the circuit, which are related to prior operations. Since the output of a logic gate is only a function of the input values and the outcome can be anticipated using the accompanying truth table, logic gates are the simplest combinational circuits. Data processing in digital electronics—including computers, cellphones, tablets, game consoles, and more—is accomplished by the use of combinational circuits.

4.5.1. Utilizing IDFAL for a Full Adder

The term "full-adder" denotes a specific type of combinational logic circuit that exerts addition operations on two binary numerals (bits) and a carry bit. Once the addition operation is finished, both the sum bit and the carry bit are output. When a combinational circuit generates two outputs and is capable of adding three binary digits, it is occasionally denoted as a "full adder." A complete adder circuit performs the addition of three binary digits. The first two digits represent inputs, whereas the last is the carry forward from the prior addition. The elementary arithmetic operation of addition can be executed by computing apparatus, calculators, and other electronic instruments.

Table 4.4: Truth Table of a Full Adder

Inputs			Outputs	
A	**B**	**C_{in}**	**Sum**	**Carry**
0	**0**	**0**	0	0
0	**0**	**1**	1	0
0	**1**	**0**	1	0
0	**1**	**1**	0	1
1	**0**	**0**	1	0
1	**0**	**1**	0	1
1	**1**	**0**	0	1
1	**1**	**1**	1	1

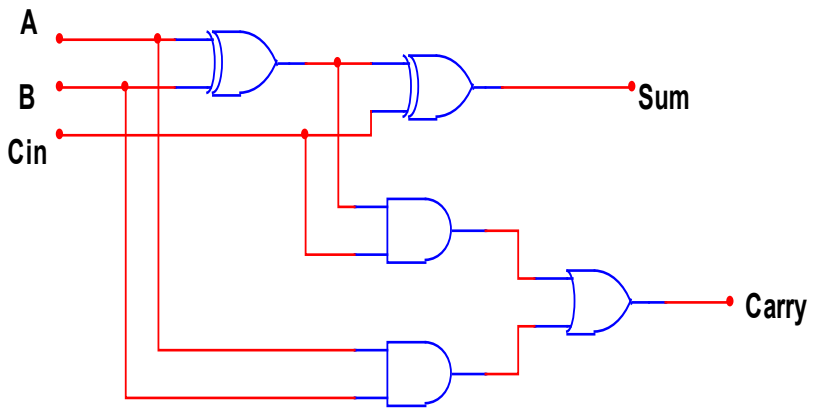

Fig.4.19: Full Adder Logic Diagram

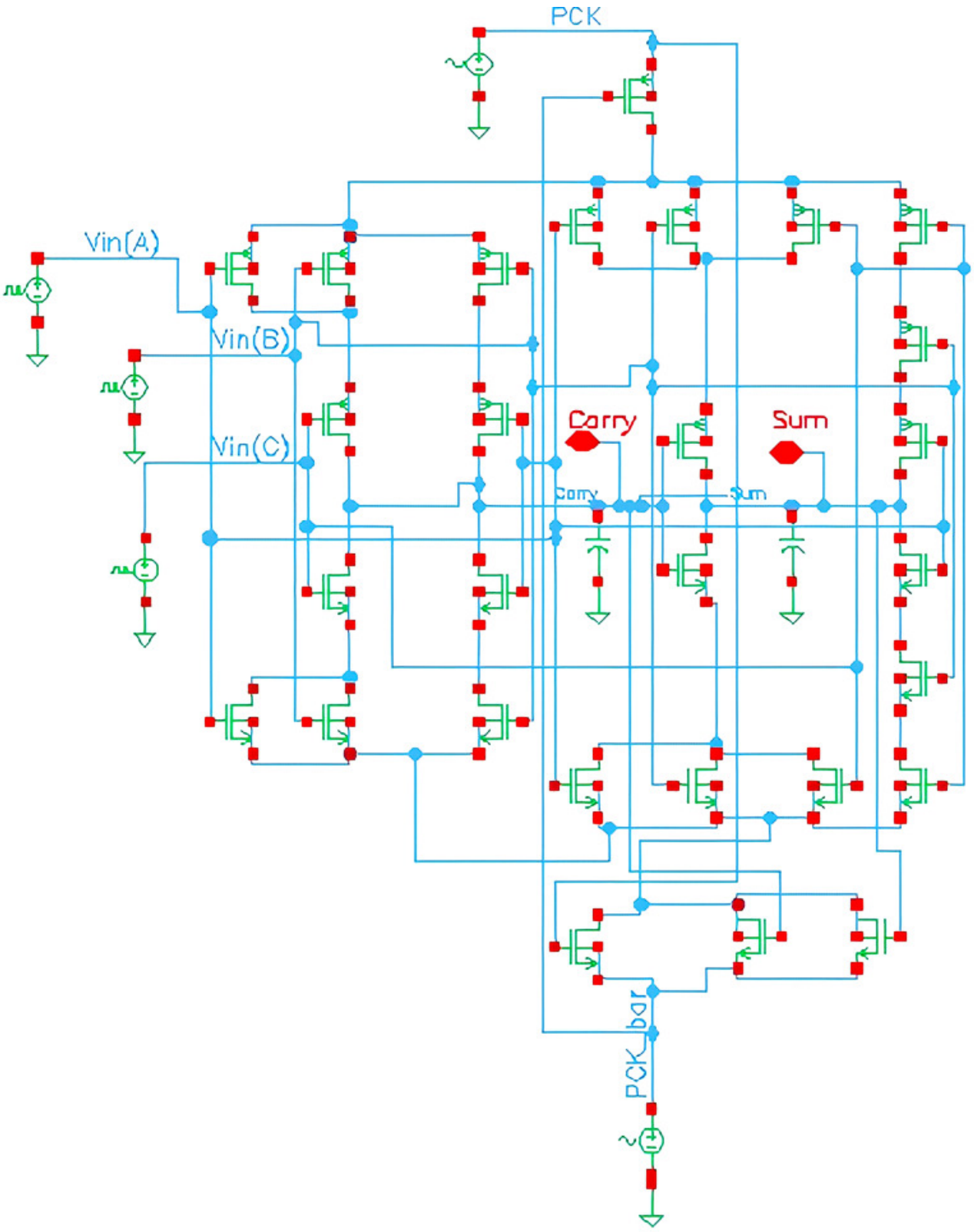

Fig.4.20: An IDFAL-Based Full Adder Circuit

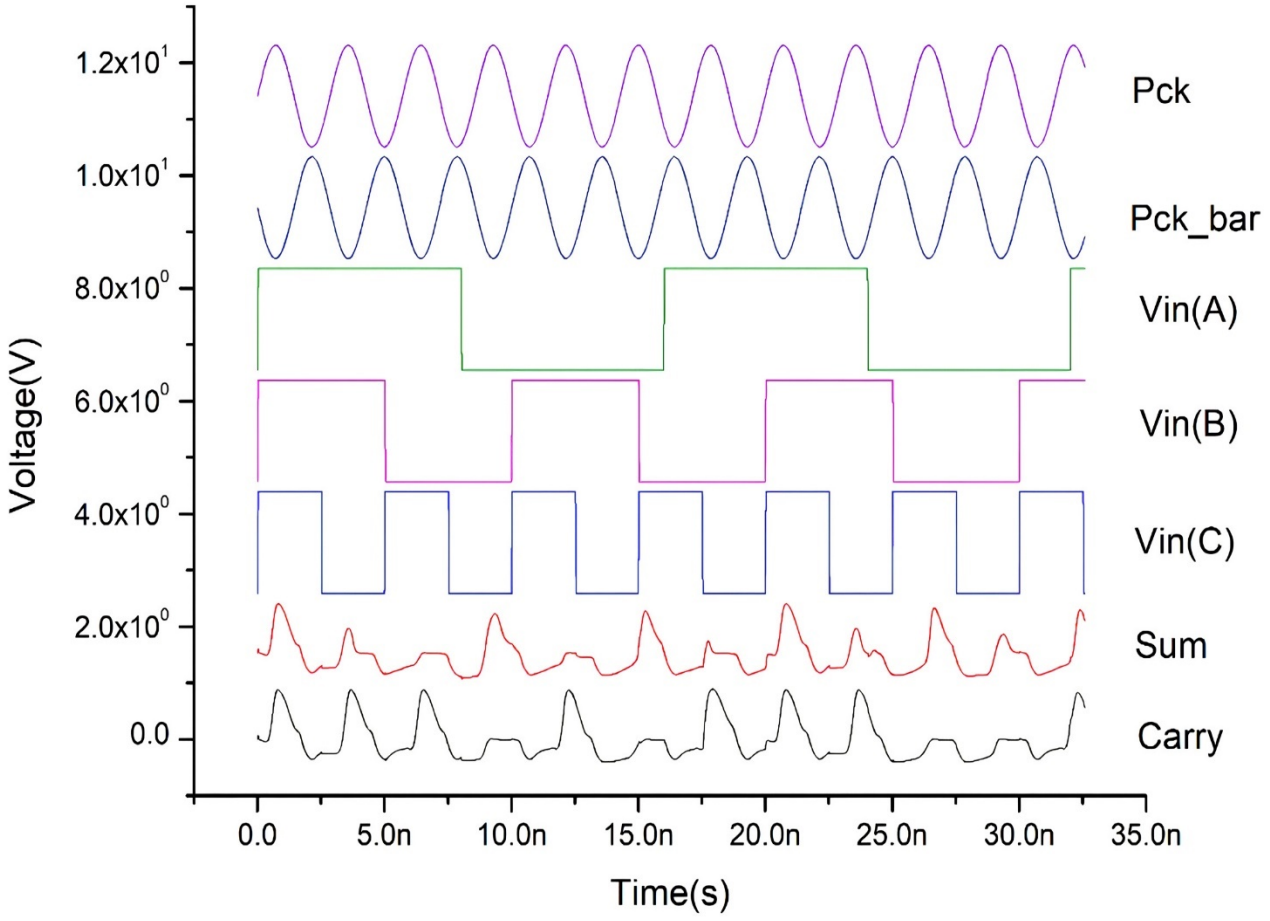

Fig.4.21: Waveform of IDFAL Full Adder

Boolean expressions for the sum and carry of full adder, as previously presented in Eqs. (4.10) and (4.11) (Zhuang & Wu, 1992; Abdul et al., 2022; Hasan et al., 2021; Kumar et al., 2011; Rajagopal & Chakrapani, 2021).

$$Sum = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$
$$= C_{in} \oplus (A \oplus B) \quad (4.10)$$

$$Carry = AB + AC_{in} + BC_{in}$$
$$= AB + C_{in}(A \oplus B) \quad (4.11)$$

An integral part of many digital electronic devices, the full adder allows for the realization of several other critical digital circuits. Digital circuits that can accept three inputs and execute addition operations are known as full-adders. This circuit typically has two XOR gates, one OR gate, and two AND gates, as seen in the logic design in Fig. 4.19. The three variables $V_{in}(A)$, $V_{in}(B)$ and $V_{in}(C)$ stand for the inputs, while the two variables Sum and $Carry$ stand for the outputs, as shown in Fig. 4.20 (Chen et al., 1999; Hasan et al., 2021). In Fig. 4.21, we can see the output waveform.

4.5.2. Single Bit Comparator Using IDFAL

The digital comparator is an extra-practical combinational logic circuit for finding the contrast between two binary values. A binary difference of two numbers is what it claims to do. Digital magnitude comparators are essential for determining whether two binary values are greater than, equal to, or less than one another.

Table 4.5: Truth Table of a 1-Bit Comparator

Inputs		Outputs		
A	**B**	**A<B**	**A=B**	**A>B**
0	**0**	0	1	0
0	**1**	1	0	0
1	**0**	0	0	1
1	**1**	0	1	0

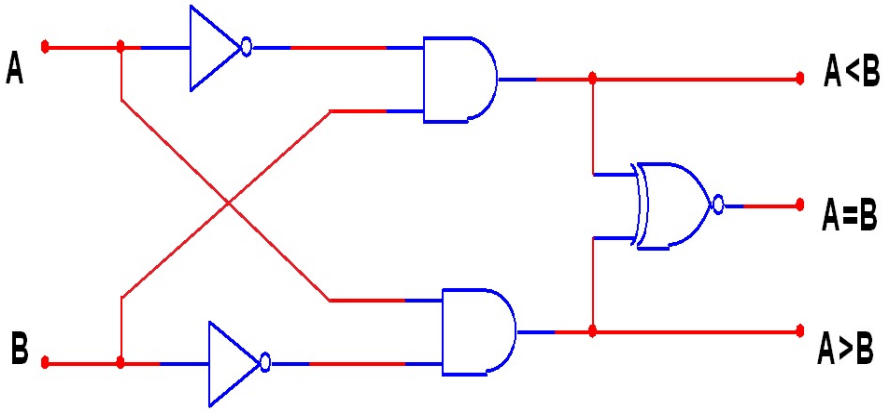

Fig.4.22: Logic Diagram of a 1-Bit Comparator

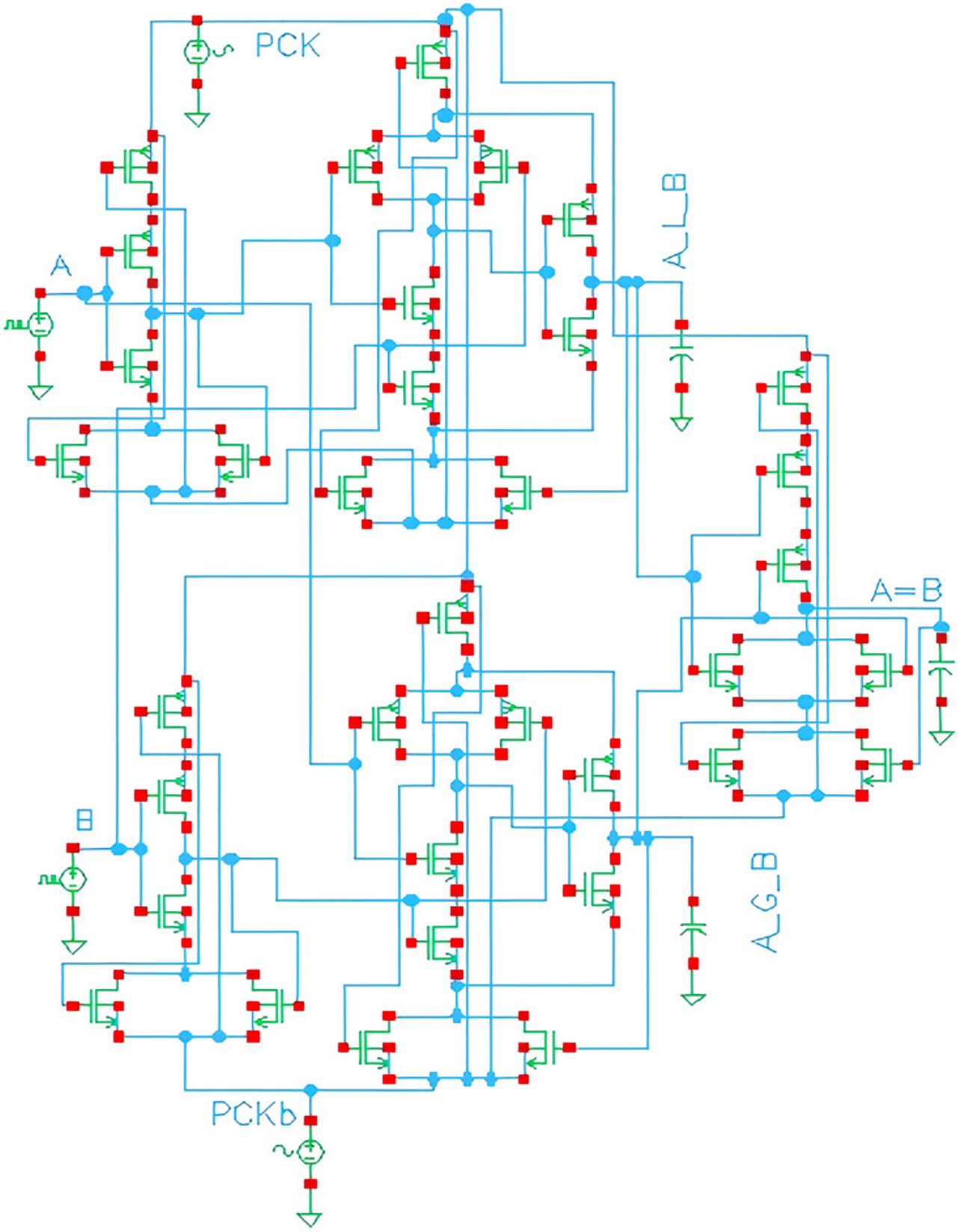

Fig.4.23: 1-Bit Comparator Circuit Using IDFAL

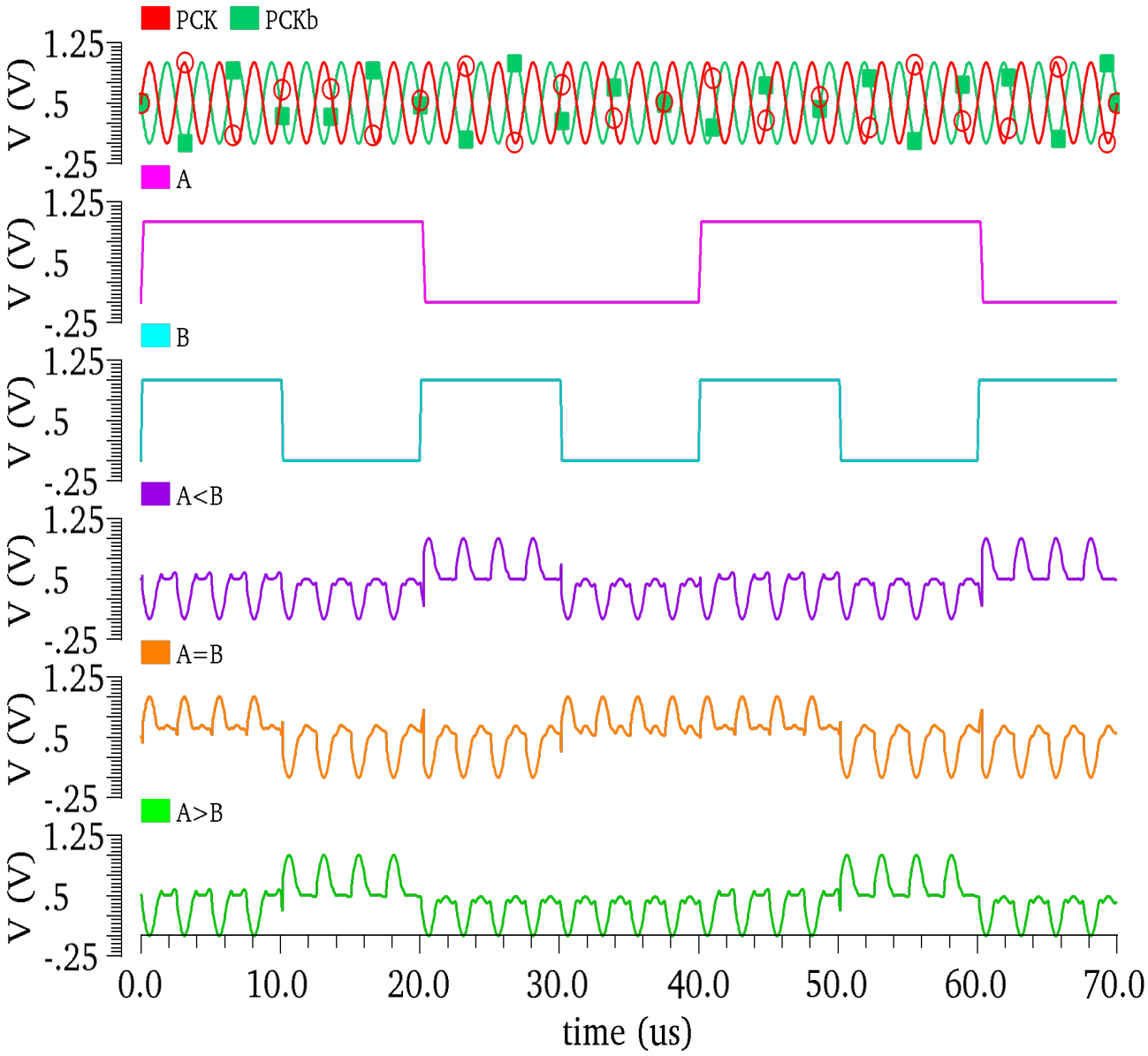

Fig.4.24: Waveform of IDFAL 1-Bit Comparator

$$(A < B) = \overline{A}B$$

$$(A = B) = \overline{\overline{A}B + A\overline{B}}$$

$$(A > B) = A\overline{B} \qquad (4.12)$$

A logic circuit is built utilising two inputs, A and B, and three outputs: one for when A>B, one for when A=B, and one for if A>B. With the help of exclusive-NOR gates, digital comparators can do bit-by-bit comparisons. In order to compare two binary or BCD values or variables, one uses a "magnitude comparator," as the name implies. This tool compares the "magnitude" of both values, which corresponds to the number of bits that each value has, which may range from 0 to 1. In Table 4.5 and Fig. 4.22, we can see the truth table and logic diagram of a 1-bit comparator, respectively. In Eq. 4.12, the Boolean expression is also referenced. The IDFAL-based structure of a 1-bit comparator circuit is shown in Fig. 4.23, and the waveforms that go with it are shown in Fig. 4.24 (Ahmed et al., 2020; Tailor et al., 2019; Rakshit, 2017).

4.5.3. 2x4 Decoder Using IDFAL

A circuit that receives a sequence of digital signals and transforms them into a decimal code is a digital decoder, since the term "decoder" denotes the operation of transforming encoded data into its unencoded state. With a limit of $m = 2^n$ distinct lines, this combinational circuit converts binary data from n input lines to output. An n-digit binary code has the capacity to contain a total of $2n$ distinct combinations of encoded data. Decoding accomplishes this purpose. In order to generate $2n$ lines of output, a decoder converts an n-bit code. Typically, binary codes are employed in digital electronics for expressing discrete quantities of data. N-bit binary codes are necessary to represent a maximum of $2n$ distinct elements of information. In the realm of digital electronics, binary codes are employed to encode only two-digit integers. In binary code representation, an n-bit code can accommodate no more than $2n$distinct data points. All other inputs are "idle" (HIGH) at any given time, while one is "active" (LOW) on a binary decoder. Which output will be active at any particular time is determined by the active low input. A variety of binary decoders exist, some of which employ priority decoding to prioritize particular outputs over others, while others scan the binary code for errors and output an error message if one is detected. As depicted in Fig. 4.25, the 2-to-4-line binary decoder comprises a 4-gate AND array. Taking two binary inputs (S0 and S1) and outputting one of four potential results is the reason this is referred to as a 2-to-4 binary decoder. A single output, any one from (Y0–Y3), can be active (HIGH) at any given time, and this is controlled by the binary inputs S0 and S1. The other outputs are conserved at level LOW, or OFF, at all other times.

Table 4.6: Truth Table of a 2x4 Decoder

Enable	Inputs		Outputs			
E	**S1**	**S0**	**Y3**	**Y2**	**Y1**	**Y0**
0	**X**	**X**	0	0	0	0
1	**0**	**0**	0	0	0	1
1	**0**	**1**	0	0	1	0
1	**1**	**0**	0	1	0	0
1	**1**	**1**	1	0	0	0

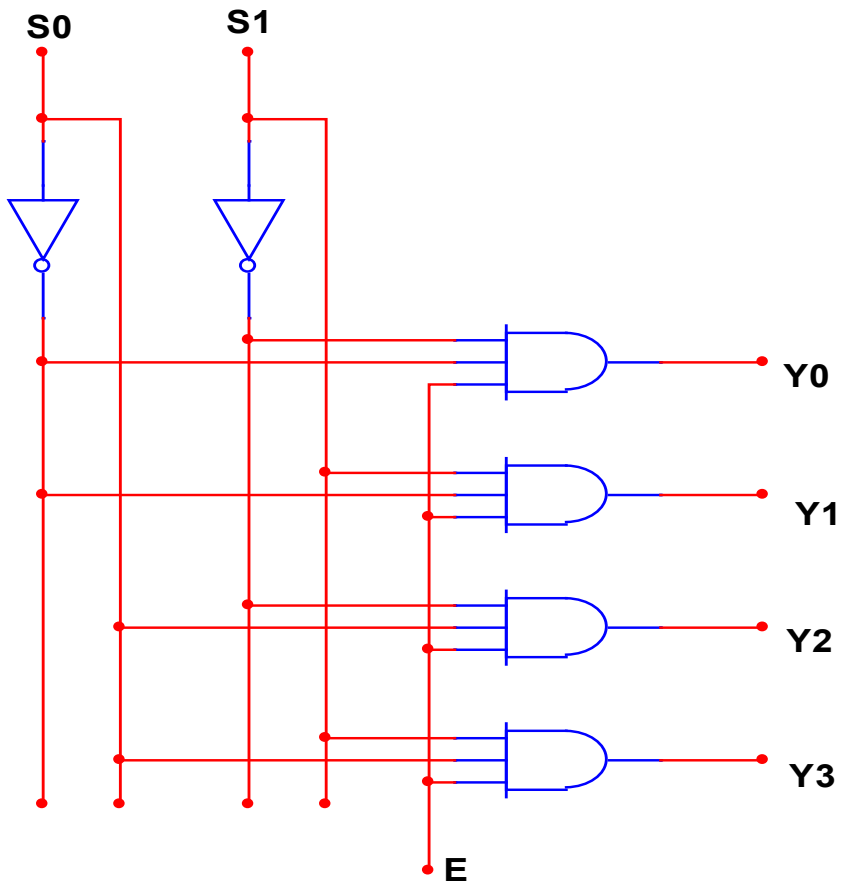

Fig.4.25: Logic Diagram of a 2x4 Decoder

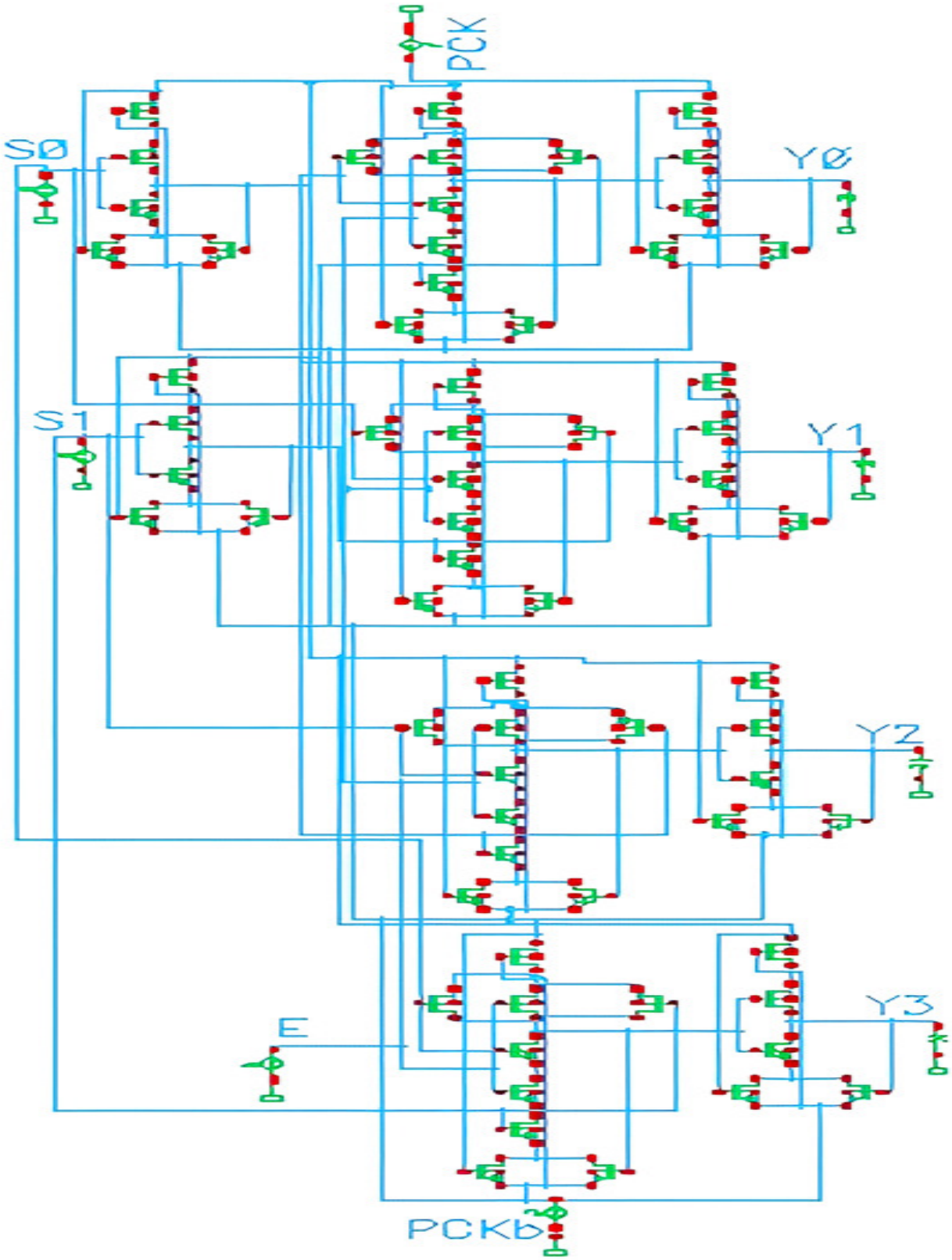

Fig.4.26: 2x4 Decoder Circuit Using IDFAL

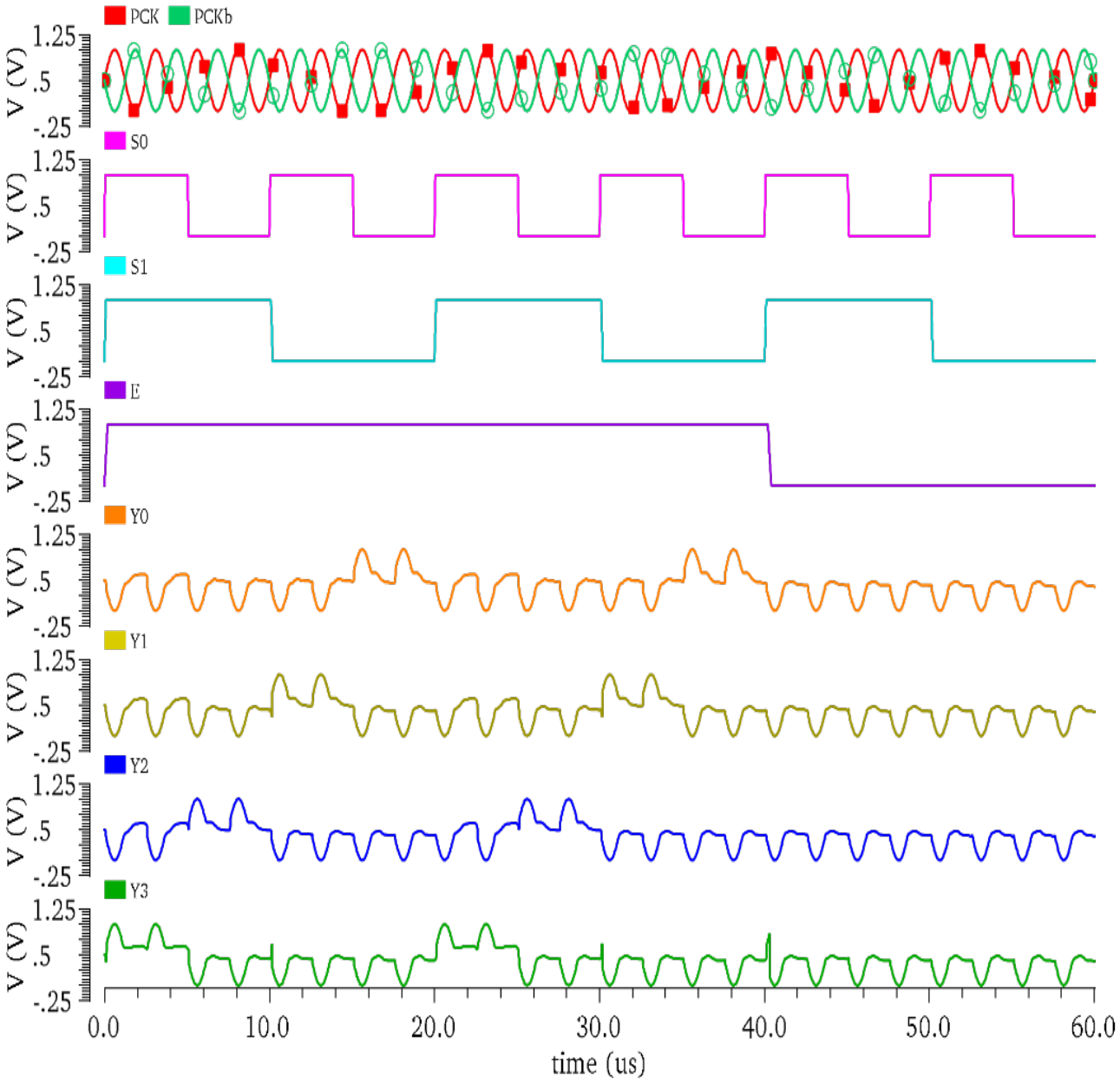

Fig.4.27: Waveform of IDFAL 2x4 Decoder Circuit.

$$Y_0 = \overline{S_1 S_0} E$$

$$Y_1 = \overline{S_1} S_0 E$$

$$Y_2 = S_1 \overline{S_0} E$$

$$Y_3 = S_1 S_0 E \qquad (4.13)$$

By utilising an additional pin called the enable input pin, denoted with the letter E, on binary decoders, the users are allowed to toggle the device's outputs on and off as needed. All outputs are zero unless the Enable input is set to one.The implementation just has to be tweaked slightly so that the enable input goes into the AND gates. If Enable is set to 0, then one of the inputs to each AND gate will be set to 0, and the gate will not create an output. When enable is 1, one of the AND gates' inputs is set to 1, and the rest of the inputs determine the gate's output. As a result, the enabler's state determines the decoder's output. The truth table of a 2x4 decoder is shown in Table 4.6, and the corresponding logic diagram is presented in Fig. 4.25. The boolean expression is also provided in Eq. 4.13. Fig. 4.26 illustrates the design of a 2x4 decoder circuit that makes use of IDFAL, and Fig. 4.27 depicts the waveforms that are associated with that design (Askarian & Akbarizadeh, 2022; Ahmadpour et al., 2021).

4.5.4. 4x1 Multiplexer Using IDFAL

Multiplexing is the act of mixing one or more signals and sending them on a single channel. Because of this, multiplexing makes it possible to send more than one signal over a single communication line. In analog communication systems, a communication channel is a limited resource that must be used as efficiently as possible. The idea of multiplexing, which makes it possible for multiple users to use a single channel in a logical way, is especially important for making it cheap and easy to use a channel. Multiplexing allowed users to use a channel in one of two ways: either sequentially or simultaneously. Multiplexing systems are ubiquitous in our everyday lives, and some of the best-known examples include the telephone network and cable television. Most multiplexers can work with either analog or digital signals.

Table 4.7: Truth Table of a 4x1 Multiplexer

Inputs	S1	S0	Outputs(Y)
D0	0	0	D0
D1	0	1	D1
D2	1	0	D2
D3	1	1	D3

When it comes to digital systems, the multiplexer is an essential building element due to its widespread use as a combination circuit. They are commonly employed in determining the best path between several origins and a final destination. The fundamental multiplexer has several lines for receiving data and just one for sending it out. Table 4.7 presents the truth table pertaining to a 4x1 multiplexer, while Fig. 4.28 illustrates the associated logic diagram. Additionally, the formula for the 4x1 MUX using a Boolean expression is shown in Eq. 4.14. The design of a 4x1 MUX circuit utilizing IDFAL is depicted in Fig. 4.29, and the corresponding waveforms are depicted in Fig. 4.30.

$$Y = S_1 S_0 D_3 + S_1 \overline{S_0} D_2 + \overline{S_1} S_0 D_1 + \overline{S_1 S_0} D_0 \tag{4.12}$$

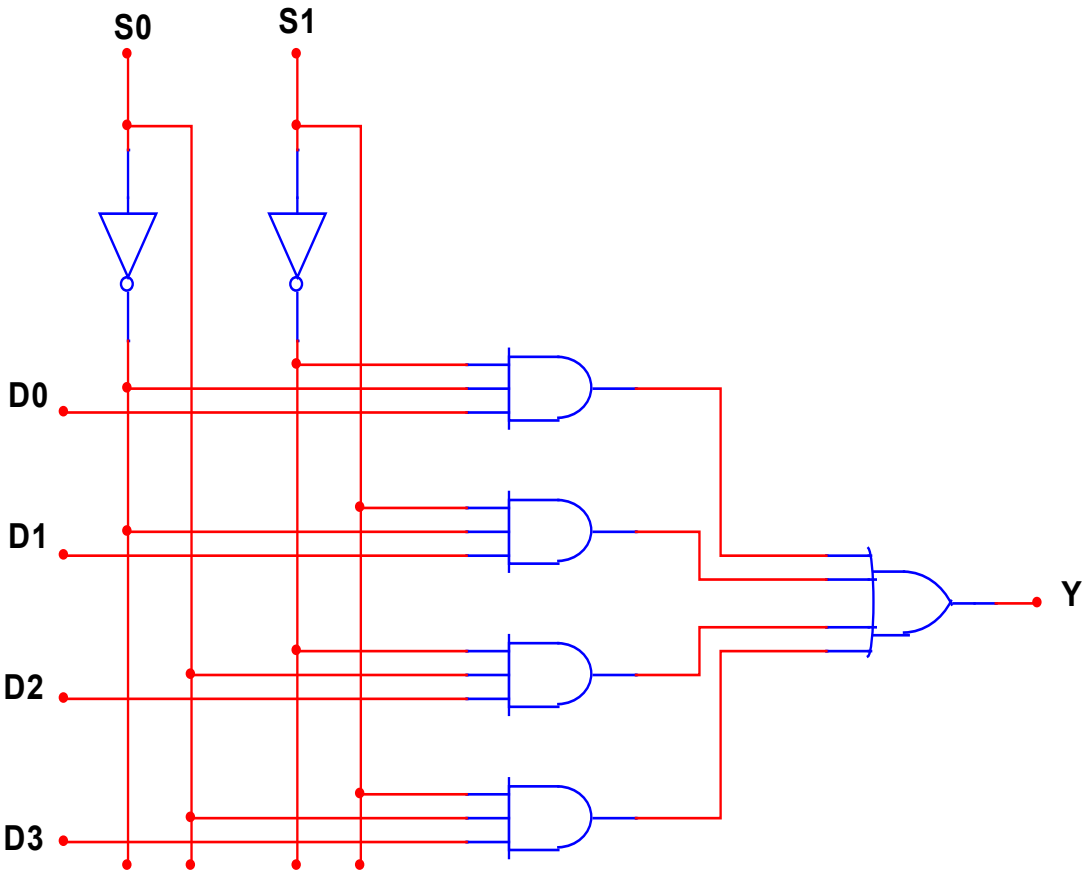

Fig.4.28: Logic Diagram of a 4x1 Multiplexer

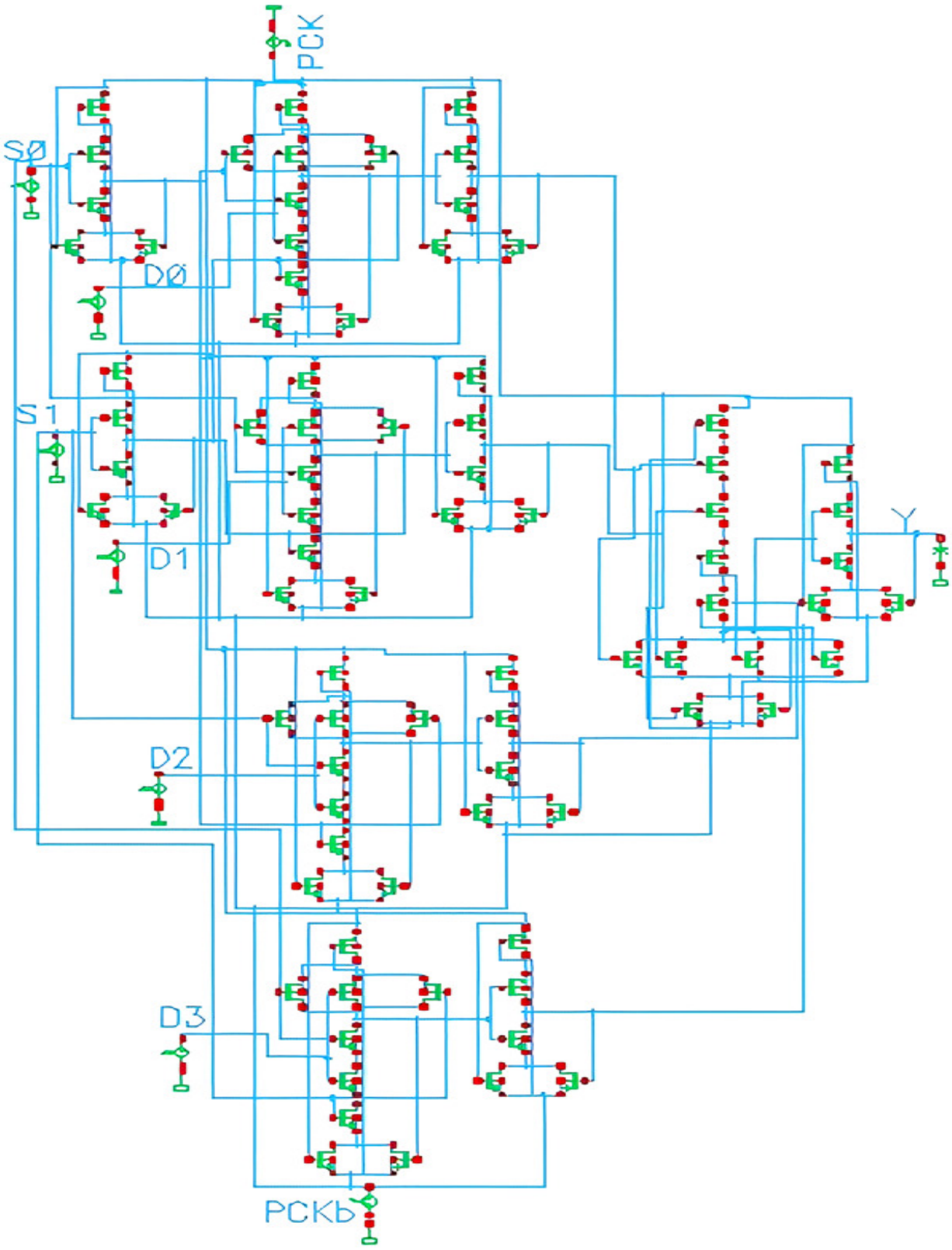

Fig.4.29: 4x1 Multiplexer Circuit Using IDFAL

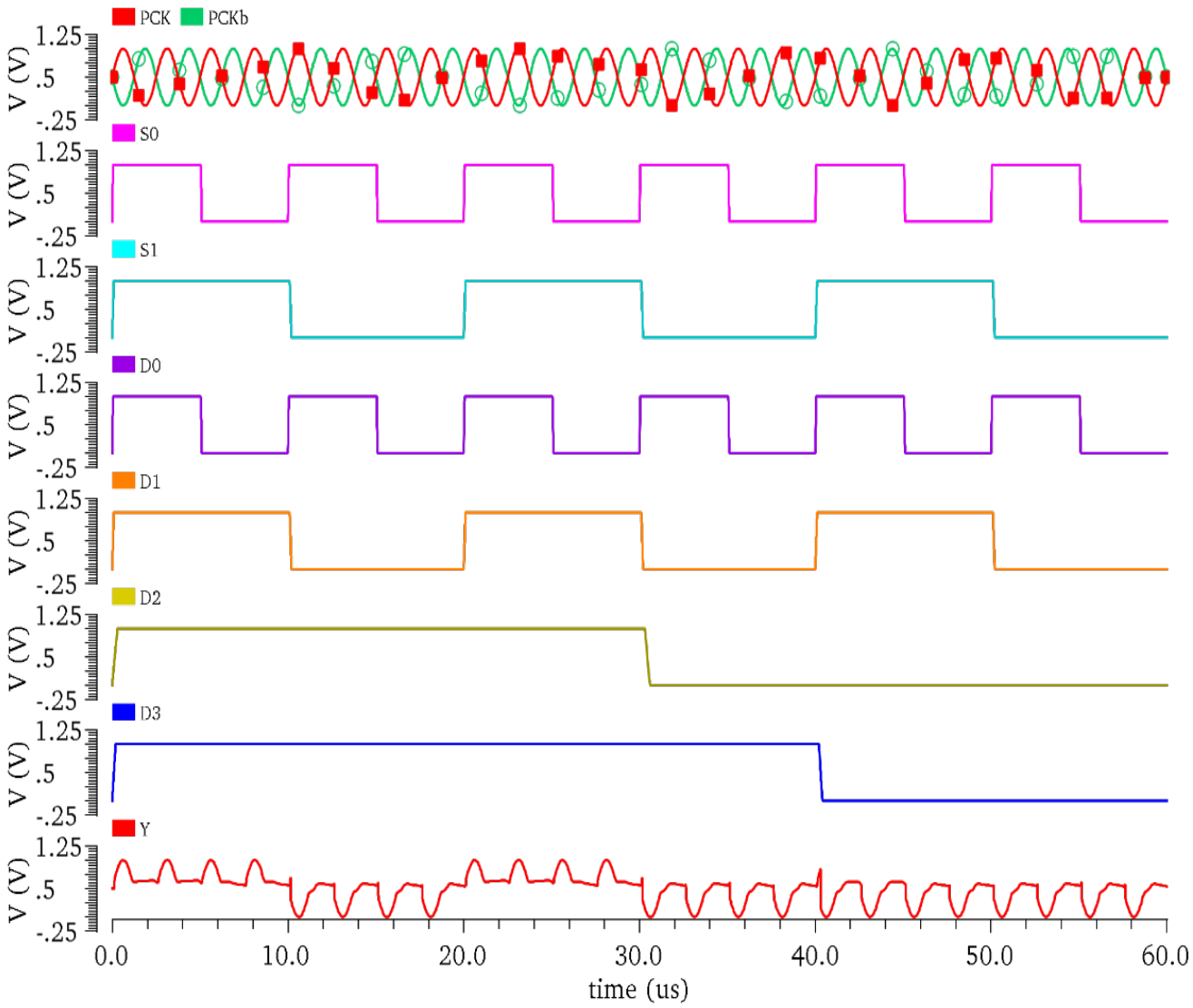

Fig.4.30: Waveform of IDFAL 4x1 Multiplexer Circuit.

Data selection and data pathways, digital calculators with complex indications, waveform generators, telephone networks, communication systems, etc. all make use of multiplexers in digital circuits. Multiplexers are a type of combinational circuit that has at most N selection lines, $2N$ data inputs, and only one output. The correlation between the ultimate result and one of these data inputs will be determined by the values of the selection lines. The presence of selection lines results in an infinite number of possible permutations of the 0s and 1s. This signifies that every possible permutation yields an entirely distinct outcome. "MUX" is an alternative abbreviation for "multiplexer." The quantity of input lines is typically a multiple of two, represented by values like 2, 4, 8, 16, and so forth. Practical multiplexer configurations include those with ratios of 2:1, 4:1, 8:1,

and 16:1. As illustrated in Fig. 4.30, the logic diagram of a 4x1 multiplexer reveals the following: Y represents the sole output; S0 and S1 represent the two selection lines; and D0, D1, D2, and D3 represent the four data inputs. The operation of a 4x1 multiplexer is depicted in the block diagram presented in Fig. 4.30. The identification of the final output is determined by the input combinations at the point of choice lines (Roa & Jung, 2013; Mishra & Akashe, 2014; Majeed et al., 2021).

4.6. Results and Discussions

The process of determining the power requirements of each individual circuit within the Cadence Virtuoso analog design environment is depicted in Fig. 4.31. The average power usage for a collection of adiabatic logic families and conventional CMOS during the design of multiple sequential and combinational circuits at 45 nm employing LP_PTM technology is depicted in the form of bar graphs in Figs. 4.32 and 4.33. For the aspect ratio $\frac{W}{L}$, the device parameters are set to $L = 45nm$, $W_n = 400nm$, and $W_p = 600nm$. In addition, the input voltage V_{in} was set to $1V$ and the load capacitance C_L to $10\,fF$ during the simulation. It was determined that the magnitude of the complementary sinusoidal split voltage is $|V_{clk}| = |\overline{V_{clk}}| = 0.5V$.

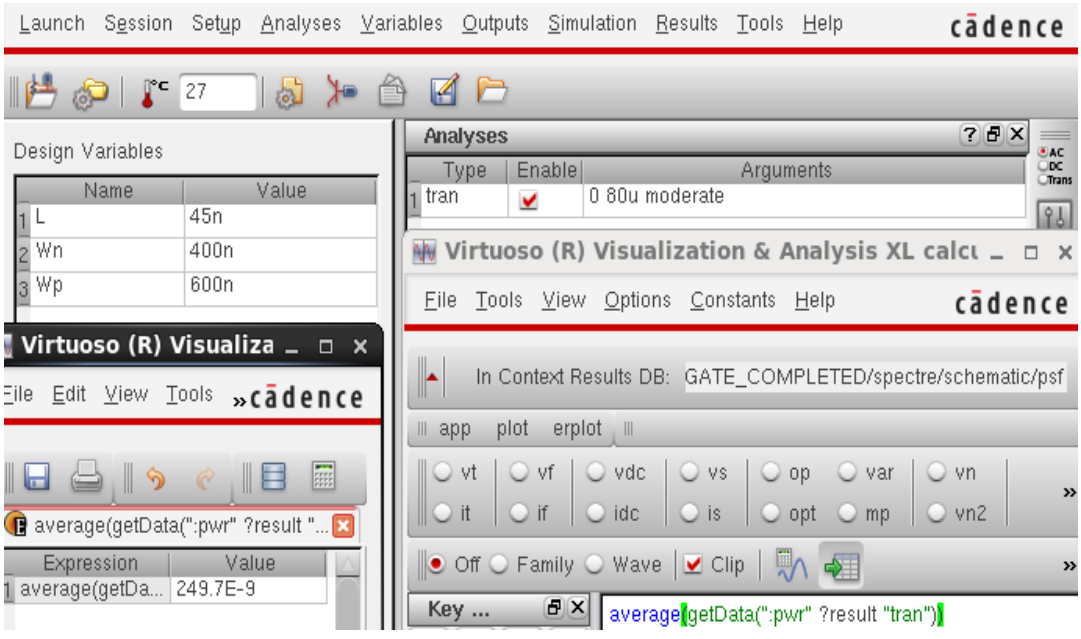

Fig.4.31: Simulation settings and average power usage in the analysis XL table in analog design environment.

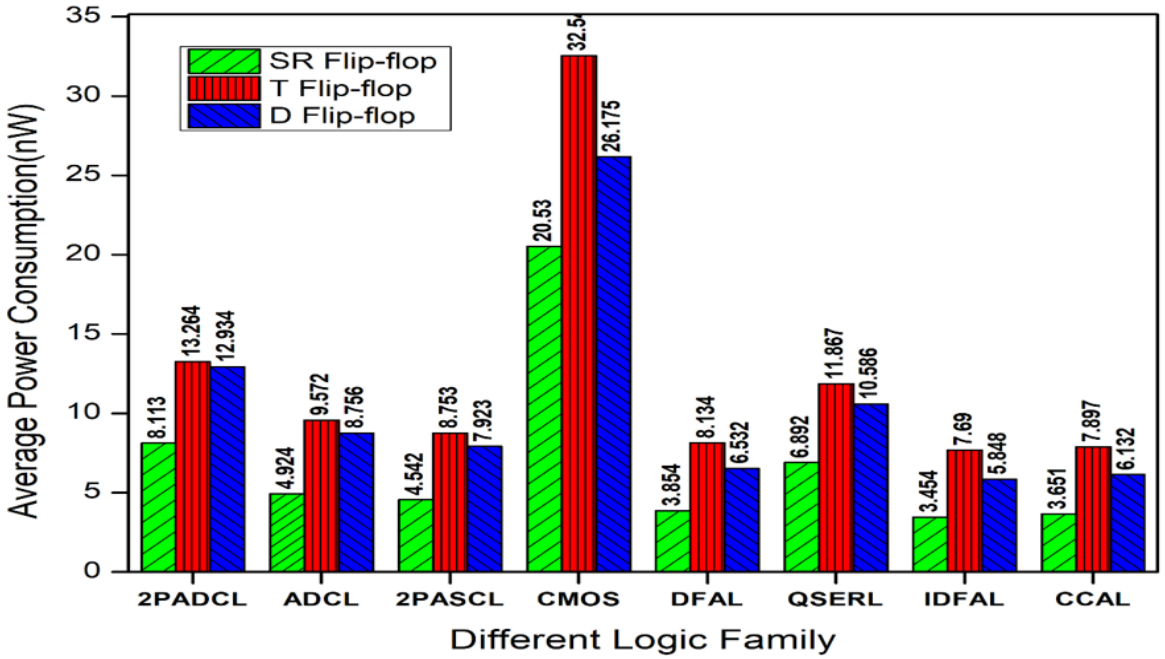

Fig.4.32: Average power consumption of sequential circuits using 45nm_LP_PTM, within 4 clock cycles at 100 kHz

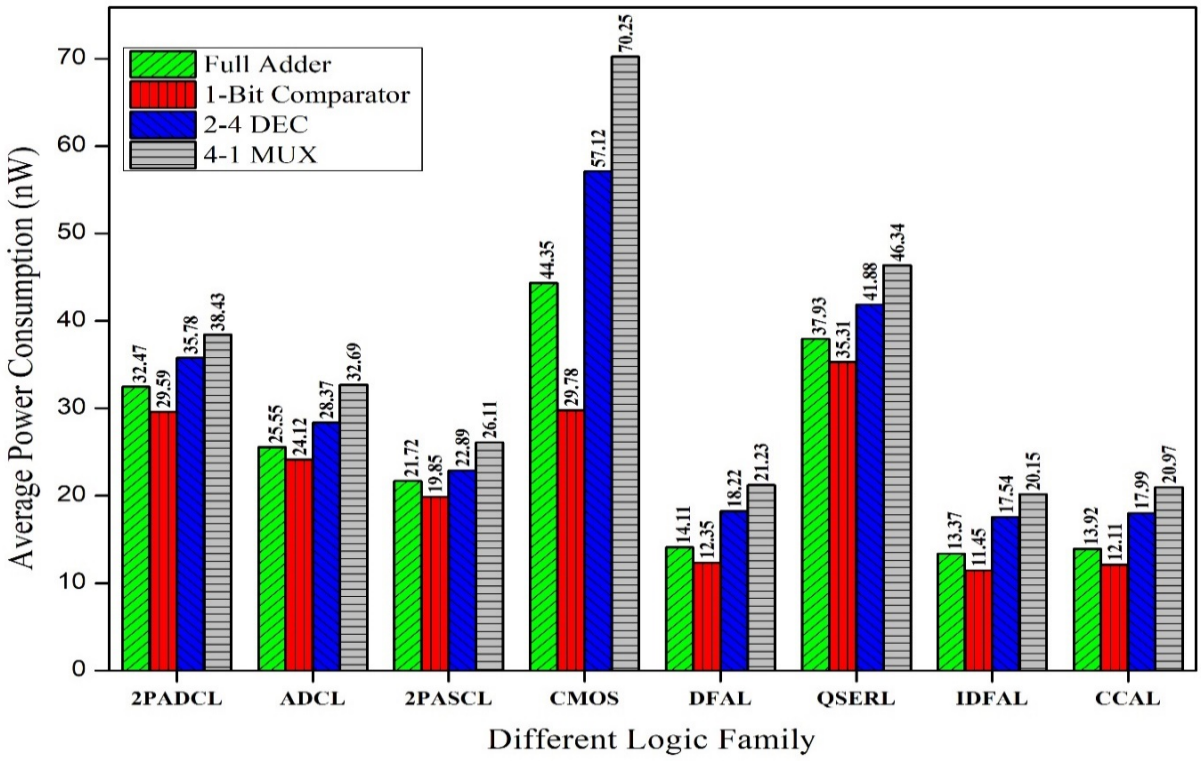

Fig.4.33: Average power consumption of combinational circuits using 45nm_LP_PTM, within 4 clock cycles at 100 kHz.

4.6.1. Comparisons of Various Result in Tables

Power supply and MOS parameters are set in accordance with (Bhushan & Ketchen, 2015). The load capacitor is always kept at $C_L = 0.01pf$. Table 4.8 compares how well different sequential logic circuits work when built on 45 nm LP_PTM and designed using both standard CMOS methods and a variety of adiabatic logic methods.

Table 4.8: 45 nm LP_ PTM: Comparing Sequential Circuits Built with Traditional CMOS and Adiabatic Logic Design Methods at 100 kHz and 40 µm Simulation Time.

45nm_LP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (nW)**	**Delays (ns)**	**PDP (E-18J)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	**SR_FF**	20.53	0.04196	0.861439	821.2	34.45755
	D_FF	26.17	0.04651	1.217399	1047	48.69597
	T_FF	32.54	0.04834	1.572984	1301.6	62.91934
2PASCL	**SR_FF**	4.542	0.34305	1.558133	181.68	62.32532
	D_FF	7.923	0.35675	2.82653	316.92	113.0612
	T_FF	8.752	0.38272	3.349565	350.08	133.9826
DFAL	**SR_FF**	3.854	0.14781	0.569661	154.16	22.78639
	D_FF	6.532	0.18959	1.238402	261.28	49.53608
	T_FF	8.134	0.19102	1.553757	325.36	62.15027
CCAL	**SR_FF**	3.651	0.11125	0.406174	146.04	16.24695
	D_FF	6.132	0.15673	0.961068	245.28	38.44273
	T_FF	7.897	0.18208	1.437886	315.88	57.51543
ADCL	**SR_FF**	4.924	1.55512	7.657411	196.96	306.2964
	D_FF	8.756	1.63573	14.32245	350.24	572.8981
	T_FF	9.572	1.78994	17.13331	382.88	685.3322
IDFAL	**SR_FF**	3.454	0.09723	0.335832	138.16	13.4333
	D_FF	5.848	0.09987	0.58404	233.92	23.36159
	T_FF	7.693	0.16807	1.292458	307.6	51.69833
QSERL	**SR_FF**	6.892	0.92125	6.349255	275.68	253.9702
	D_FF	10.58	0.95673	10.12794	423.44	405.1178
	T_FF	11.86	1.28208	15.21444	474.68	608.5777
2PADCL	**SR_FF**	8.113	0.82125	6.662801	324.52	266.5121
	D_FF	12.93	0.85673	11.08095	517.36	443.2378
	T_FF	13.26	0.98208	13.02631	530.56	521.0524

Table 4.9: 45nm_LP_PTM; Analyzing the Efficiency of Different Combinational Circuits Built with Traditional CMOS and a few Forms of Adiabatic Logic During the 40 µm simulation time at an operating frequency of 100 kHz

45nm_LP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (n W)**	**Delays (ns)**	**PDP (E-18J)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	**Full Adder**	51.048	0.095	4.84956	2041.92	193.98241
	2x4 Decoder	74.911	0.081	6.06779	2996.44	242.71164
	4x1 Multiplexer	94.442	0.085	8.02757	3777.68	321.10283
	1-Bit Comparator	38.886	0.088	3.42196	1555.44	136.87872
2PASCL	**Full Adder**	11.949	0.892	10.6585	477.961	426.34032
	2x4 Decoder	17.968	0.752	13.5119	718.722	540.47744
	4x1 Multiplexer	23.149	0.798	18.4729	925.963	738.91608
	1-Bit Comparator	9.9681	0.813	8.10398	398.721	324.15936
DFAL	**Full Adder**	9.3231	0.622	5.79891	372.922	231.95624
	2x4 Decoder	15.624	0.425	6.64023	624.963	265.60803
	4x1 Multiplexer	20.182	0.482	9.72772	807.281	389.10896
	1-Bit Comparator	7.6491	0.598	4.57410	305.963	182.96408
CCAL	**Full Adder**	8.1842	0.597	4.88584	327.361	195.43392
	2x4 Decoder	14.207	0.497	7.06087	568.283	282.43516
	4x1 Multiplexer	16.852	0.513	8.64507	674.084	345.80304
	1-Bit Comparator	7.0651	0.552	3.89988	282.621	155.99522
ADCL	**Full Adder**	13.599	1.989	27.0484	543.962	1081.9364
	2x4 Decoder	20.803	1.453	30.2267	832.123	1209.0704
	4x1 Multiplexer	26.214	1.721	45.1142	1048.56	1804.5718
	1-Bit Comparator	11.852	1.877	22.2462	474.081	889.84816
IDFAL	**Full Adder**	7.1412	0.569	4.06322	285.642	162.52916
	2x4 Decoder	10.572	0.474	5.01112	422.884	200.44512
	4x1 Multiplexer	14.119	0.513	7.24304	564.761	289.72188
	1-Bit Comparator	5.6071	0.543	3.04461	224.286	121.78404
2PADL	**Full Adder**	17.843	1.417	25.2835	713.729	1011.3412
	2x4 Decoder	28.109	1.152	32.3815	1124.36	1295.2627
	4x1 Multiplexer	33.177	1.276	42.3338	1327.08	1693.3541
	1-Bit Comparator	15.588	1.389	21.6517	623.522	866.06928
QSERL	**Full Adder**	17.795	1.573	27.9915	711.809	1119.6614
	2x4 Decoder	23.771	1.251	29.7375	950.844	1189.5008
	4x1 Multiplexer	27.054	1.342	36.3064	1082.16	1452.2587
	1-Bit Comparator	14.562	1.482	21.5808	582.488	863.23536

These include 2PASCL, DFAL, CCAL, ADCL, IDFAL, QSERL, and 2PADCL. The simulation time is 40 µs, and the operating frequency is 100 kHz. Every adiabatic design approach is compared in the table along with their average power consumption, circuit propagation delays, energy consumption, PDP, and EDP. In the same way, Table 4.9 compares the performance of different

combinational logic circuits on 45nm LP_PTM designed using traditional CMOS techniques and a variety of adiabatic logic techniques, such as 2PASCL, DFAL, CCAL, ADCL, IDFAL, QSERL, and 2PADCL, with a simulation time of 40 μs and an operating frequency of 100 KHz. The benchmark performance of the IDFAL circuit in relation to PDP and EDP is evident from the simulation results for 45nm LP_PTM and from tables 4.8 and 4.9. The advantage of employing the IDAFL circuit design strategy over conventional or sequential logic circuit designs is validated by the simulation outcomes presented in tables 4.8 and 4.9. For sequential logic circuits, including SR flip-flops, D flip-flops, and T flip-flops, Fig. 4.32 is a bar graph illustrating the mean power usage of standard CMOS and various adiabatic logic design approaches. The simulation is conducted at a frequency of 100 kHz. For a variety of combinational logic circuits, including a full adder, a 1-bit comparator, a 2x4 decoder, and a 4x1 multiplexer, at an operating frequency of 100 kHz, the average power consumption of several non-cross-coupled, CMOS static-based adiabatic logic design methods is illustrated in Fig. 4.33. The minimum average power consumption in sequential and combinational circuits is exhibited by the IDFAL, as illustrated in Figs. 4.32 and 4.33.

4.7. Summary

Power optimization, energy usage, circuit propagation delays, PDP, and EDP are some of the areas where this chapter proves the IDFAL circuit is better than traditional CMOS and other adiabatic logic circuits when it comes to creating sequential and combinational circuits. While creating an SR flip flop at a frequency of 100 kHz, the IDFAL achieves power savings of 83.17%, 57.42%, 49.88%, 23.95%, 10.37%, and 5.39% compared to CMOS, 2PADCL, QSERL, ADCL, 2PASCL, DFAL, and CCAL. By creating a 1-bit comparator at 100 kHz frequency, it saves 80.97%, 48.78%, 43.81%, 35.89%, 27.15%, 11.16%, and 2.29% of dynamic power against CMOS, 2PADCL, QSERL, ADCL, 2PASCL, DFAL, and CCAL. The IDFAL would thus be ideal and particularly advantageous for creating complicated circuits that include both sequential and combinational circuits.

CHAPTER 5

A Low Power Design Using FinFET Based Adiabatic Switching Principle: Application to 16-Bit Arithmetic Logic Unit (ALU)

5.1. Introduction

In the area of VLSI-Very Large-Scale Integration circuit design, power saving is the main design parameter since the power optimization capability of a circuit greatly affects its overall performance. ALU is the backbone of microprocessors, microcontrollers, and digital computers, as all the computations and operations are done by it. In recent years, the demand for and consequently the quest for low-power, lightweight, and non-portable gadgets have rapidly increased (Chanda et al., 2015; Nayan et al., 2012). Unavoidable and intolerable short channel effects were encountered while scaling MOS transistors down to the nanoscale (Dadoria et al., 2017; Dadoria et al., 2018). In addition, adiabatic design methodology results in much less energy loss than typical CMOS design architecture (Sharma, 2020; Anuar et al., 2009; Chanda et al., 2009; Ye & Roy, 2001).

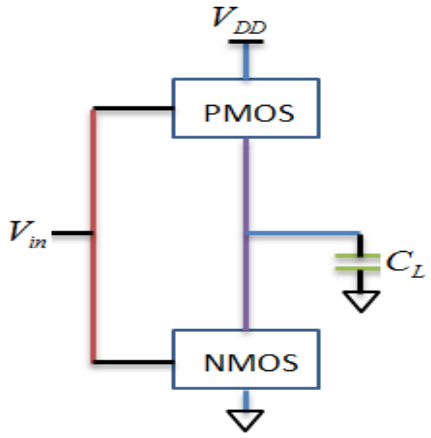

Fig. 5.1: Schematic of CMOS Inverter

However, the power consumption of FinFET-based circuits can be reduced to a great extent. For a typical CMOS inverter shown in Fig. 5.1, when the PMOS transistor is ON, the total energy drawn from the supply voltage is $E_{V_{DD}} = QV_{DD} = C_L V_{DD}^2$, while the energy stored in the load capacitance C_L is half of the same $(0.5C_L V_{DD}^2)$. Here V_{DD} is the supply voltage and $Q = C_L V_{DD}$ is the total

charge. The same amount of energy is dissipated in the PMOS transistor. When the input voltage (V_{in}) switches from 0 to 1 logic, the energy stored at the output is lost in the NMOS transistor. Therefore, the total energy lost is given by $0.5C_LV_{DD}^2 + 0.5C_LV_{DD}^2 = C_LV_{DD}^2$ (Nayan, Takahashi, & Sekine, 2010; Tomita, Takahashi, & Sekine, 2010; Monteiro, Takahashi, & Sekine, 2013). The total power dissipation (P_{tot}) in a conventional CMOS inverter is related to dynamic power (P_{dyn}), short circuit power (P_{sc}), and leakage power (P_{leak}) by the relation (Dadoria et al., 2018):

$$P_{tot} = P_{dyn} + P_{sc} + P_{leak} = \alpha C_L V_{DD}^2 f + I_{sc}V_{DD} + I_{leak}V_{DD} \quad (5.1)$$

where α, f, I_{sc} and I_{leak} denote the switching activity, charging frequency, short circuit current and leakage current, respectively. This chapter focuses on designing a FinFET-based ALU circuit using adiabatic logic. The reported results show a promising reduction in power consumption due to the combined effects of device (FinFET) technology and the adiabatic design methodology.

5.2. Proposed Method

To overcome the huge power loss in the traditional CMOS approach, a new design technique known as adiabatic logic is introduced (Dadoria & Khare, 2019; Kumar et al., 2017; Samanta, 2010). In this technique, energy loss is minimized by recycling the energy in a circuit. Instead of DC voltage, clocks of trapezoidal, sinusoidal waveforms, etc. are used. In Fig. 5.2, adiabatically charging and discharging of a capacitor C_L with trapezoidal voltage through the resistance R is shown. Here, the peak of the instantaneous voltage $v(t)$ is V_{DD}. The voltage reached its maximum value at switching instant T, and R is the resistance offered by a transistor when it is turned on. The instantaneous current $i(t)$ is given by:

$$i(t) = C\{dv(t)/dt\} = C(V_{DD}/T) \quad (5.2)$$

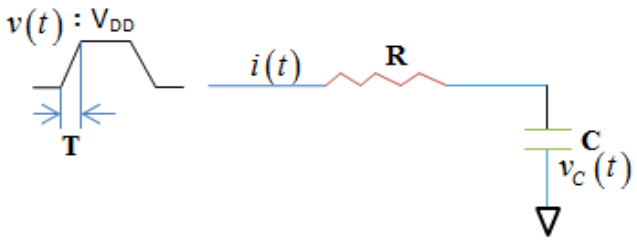

Fig. 5.2: Adiabatic switching technique.

The energy lost during a transition time is calculated by integrating the power $P(t)$ for a charging time and is given by,

$$E = \int_0^T P dt = \int_0^T v(t) i(t) dt = \int_0^T \{v_R(t) + v_C(t)\} i(t) dt \tag{5.3}$$

Since no energy is lost in the capacitor; integration of $v_c(t) \times i(t)$ yields zero. Therefore, during the charging process, energy loss is given by Dadoria & Khare (2019; Kumar et al., 2017; Samanta, 2010).

$$E = \int_0^T R\left(\frac{C^2 V^2{}_{DD}}{T^2}\right) dt = \left(\frac{RC}{T}\right) CV^2{}_{DD} \tag{5.4}$$

During the recovery period, an equivalent amount of energy is lost. Accordingly, the total energy dissipated during the whole cycle is given by:

$$E_{AL} = 2(RC/T) CV^2{}_{DD} \tag{5.5}$$

The energy loss is negatively correlated to the switching time *T.* As such, the energy loss can be optimized by manipulating the time *T,* which is missing in the typical CMOS design approach. If *T>>2RC,* then the energy consumed by an adiabatic circuit becomes less than that of a that of a conventional CMOS circuit. Moreover, the energy, after being utilized by the circuit, returns to the power source to do useful work rather than getting lost in the environment. The energy dissipation for the charging period is also calculated by using Tomita et al. (2010) and Monteiro et al. (2013).

$$E_{diss} = \xi (RC/T) C_L V_{DD}^2 \tag{5.6}$$

where ξ is the shape factor, and for sinusoidal supply, $\xi = \pi^2/8 = 1.23$. Adiabatic switching technique based on trapezoidal clock voltage along with recovery logic. Energy loss is evaluated by integrating the product of current and voltage and is given by Anuar et al. (2010) and Maksimovic et al. (2000):

$$E = \int_0^T \left(\sum_{i=1}^{n} \left(V_{pi} \times i_{pi} \right) \right) dt \tag{5.7}$$

where T is the time period of the input signal, n is the number of power sources, I_{pi} is the supply current, and V_{pi} is the supply voltage. To calculate energy dissipations in adiabatic circuits, the

transistor resistance and capacitance are required to be considered. The threshold voltage (V_t) also plays an important role in energy utilization. So, in a 2PASCL inverter circuit, the energy loss can be estimated as follows (Anuar et al., 2010):

$$E_{2PASCL} = \frac{1}{2} C_L \left[V^2{}_{tp} + V_{\phi p-p} \left| V_{tp} \right| + \left(V_{\bar{\phi} p-p} - V_{tn} \right) V_{tn} \right] \tag{5.8}$$

where C_L, V_{tp}, V_{tn}, $V_{\phi p-p}$, and $V_{\bar{\phi} p-p}$ represent the load capacitance, threshold voltage of $pMOS$, threshold voltage of NMOS, positive $(0° phase)$ voltage supply, and negative $(180° phase)$ voltage supply, respectively. The adiabatic switching technique based on trapezoidal clock voltage along with recovery logic is illustrated in Fig. 5.2. The work is implemented with a sinusoidal power supply (ξ=1.23). The use of single-phase supply in adiabatic logic is common (Kim & Papaefthymiou, 2001).

5.3. Proposed Circuit and FinFET

The schematic of the proposed inverter circuit is illustrated in Fig. 5.3. The simulated input and output waveforms of the same are as shown in Fig. 5.4. Unlike QSERL, 2PADCL, ADCL, and 2PASCL the output logic is not square-wave pattern but sinusoidal in nature and follow pass-transistor adiabatic logic output structure. The output shape is related to the patterns shown in Kumar et al. (2017) and Samanta (2010).

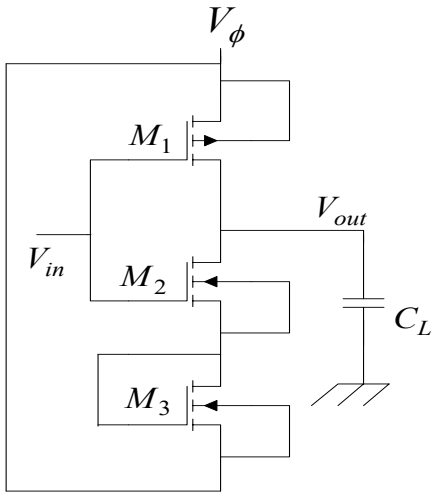

Fig. 5.3: Proposed inverter circuit.

The circuit operates in such a way that during the $1 \rightarrow 0$ transition of the input V_{in}, M_1 is on, and C_L is charged up to the peak of V_{in}. M_3 is connected in such a way that its gate and drain are shorted, acting as a reverse diode for the supply voltage V_ϕ. During the input transition, $0 \rightarrow 1$ is off and M_2 is on, while M_3 acts as a forward-biased diode, providing the energy recovery path. Therefore, the energy stored in C_L is returned to the supply source V_ϕ. When the gate and drain of M_3 are shorted, they have equal voltages $(V_{GS} = V_{DS})$. To turn on and use a transistor as a diode, the gate-to-source voltage or the drain-to-source voltage must be greater than the threshold voltage V_{TN} of the diode $(V_{GS} = V_{DS} > V_{TN})$. The energy consumed by each diode can be obtained. The proposed circuit has only one diode as compared to other design techniques. QSERL has four diodes, while 2PADCL, ADCL, and 2PASCL have two diodes each. Besides, like ADCL, the proposed circuit uses a single supply voltage and is relatively simpler.

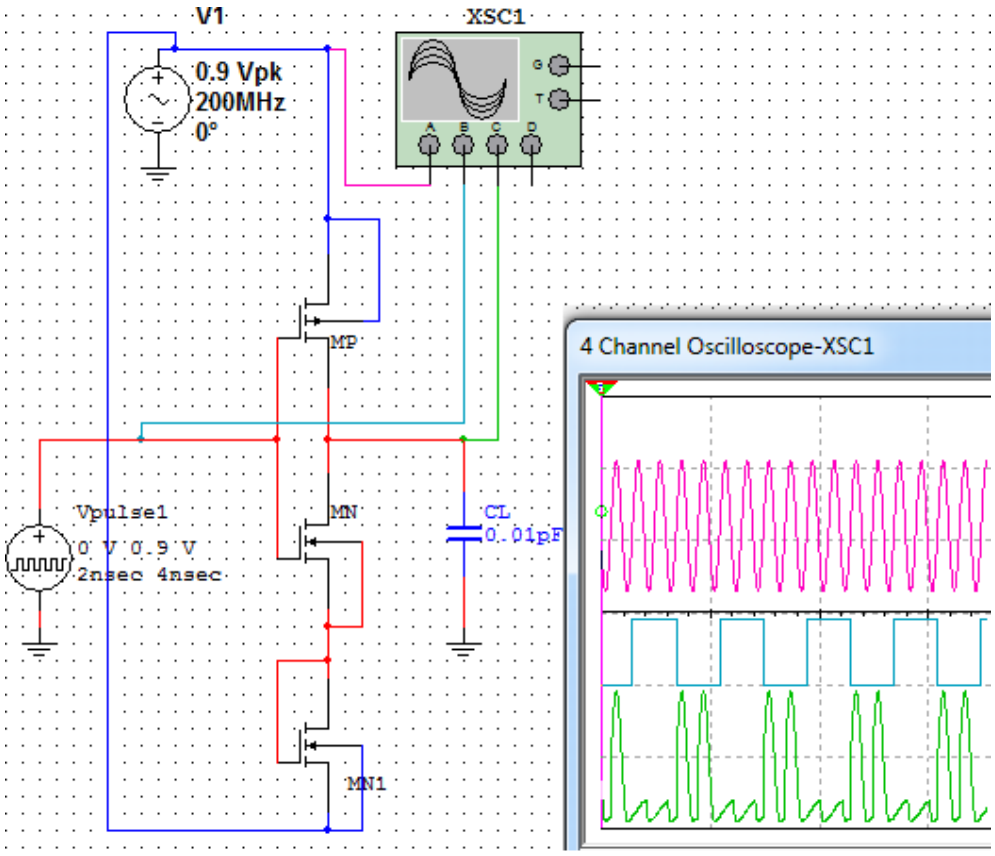

Fig. 5.4: Proposed simulated inverter circuit

The FinFET is a kind of field-effect transistor that has two gates connected to both the front and rear sides of the fin. Due to its dual gates, this technology has complete control over the channel, leading to a substantial decrease in the negative impacts of short channels commonly found in traditional CMOS technology (Dadoria et al., 2017; Dadoria et al., 2018). FinFET may be configured to function in several modes. In the short-gate (SG) mode, the two gates are connected in order to improve the speed at which it operates. It is suitable for high-performance applications. During low-power (LP) mode, the back gate is biased in the opposite direction to minimize the amount of power lost due to leakage.

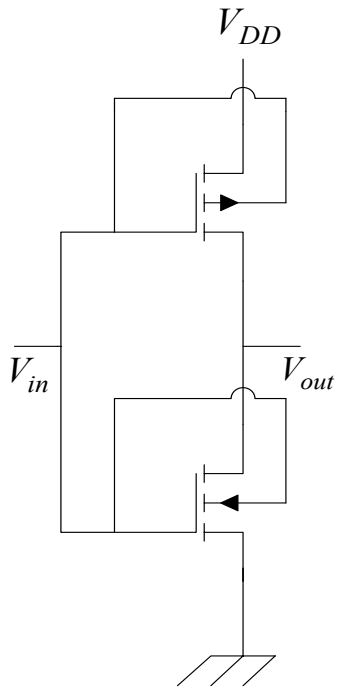

Fig. 5.5: Schematic of proposed FinFET Inverter circuit in SG mode

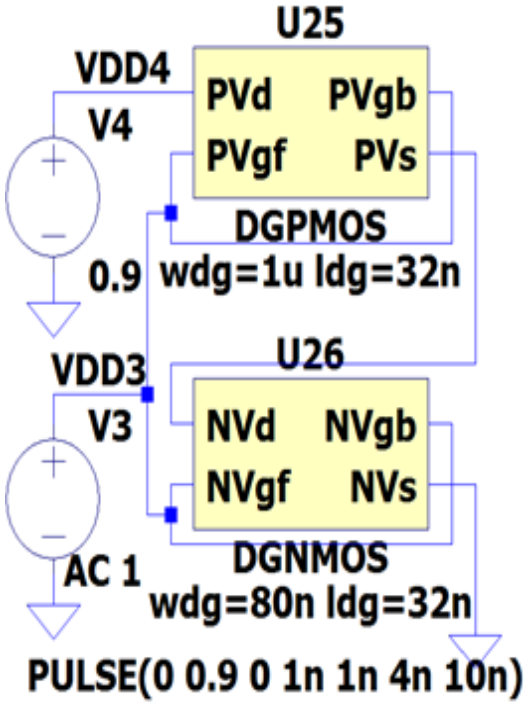

Fig. 5.6: Simulated proposed FinFET Inverter circuit in SG mode

Fig. 5.5 shows a schematic of FinFET Inverter in SG mode, where the front and back gates are joined together. Fig. 5.6 shows a realistic FinFET Inverter in SG mode. For a P-type FinFET, the drain, source, front-gate and back-gate are denoted by PV_d, PV_s, PV_gf and PV_gb respectively. Likewise, for N-type FinFET, NV_d, NV_s, NV_gf and NV_gb, are the drain, source, front-gate, and back-gate terminals, respectively. The FinFET sub-circuit device is instanced from a code of PTM at 32nm

technology. The width and length of drain to gate for PMOS are $wdg = 1\mu m$ and $ldg = 32nm$. Also, the corresponding parameters for NMOS are $wdg = 80nm$ and $ldg = 32nm$.

Fig. 5.7 shows a FinFET inverter in LP Mode. In this mode, the back gate of PMOS is connected to high voltage, whereas the back-gate of NMOS is connected to low-voltage. The optimum high and low voltages are found to be 1.7 V and -0.5 V, respectively. SPICE simulation in transient analysis up to 40 ns shows that the average power consumption of FinFET inverter is 5.3465nW or the average energy consumption is 0.21333fJ. Fig. 5.8 presents the power analysis of CMOS inverter at 32*nm* Barkley PTM technology at time intervals of 0–40ns. The average power dissipation is found to be 382.96nW or the average energy consumption is 15.28fJ.

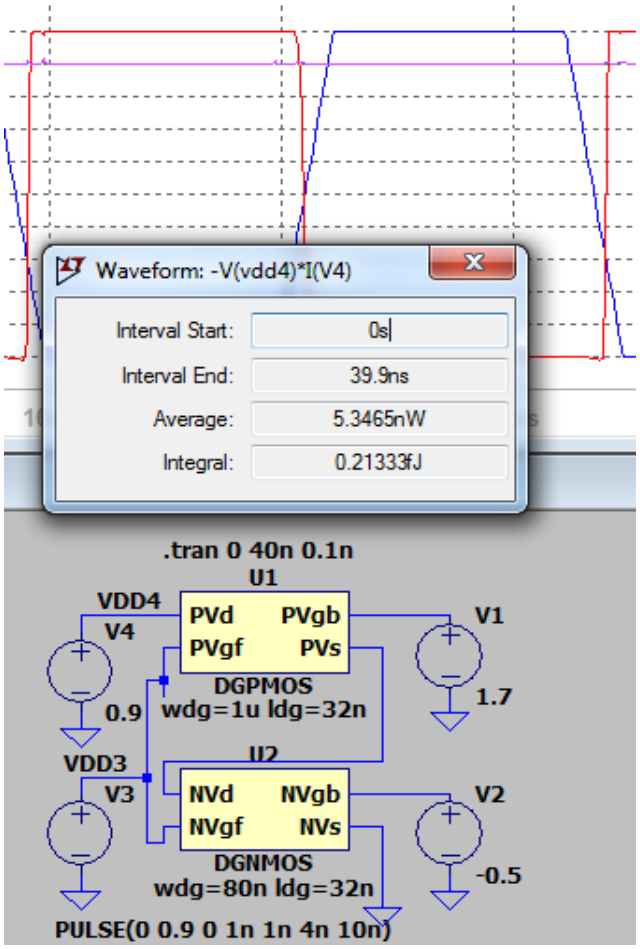

Fig. 5.7: FinFET Inverter in LP mode

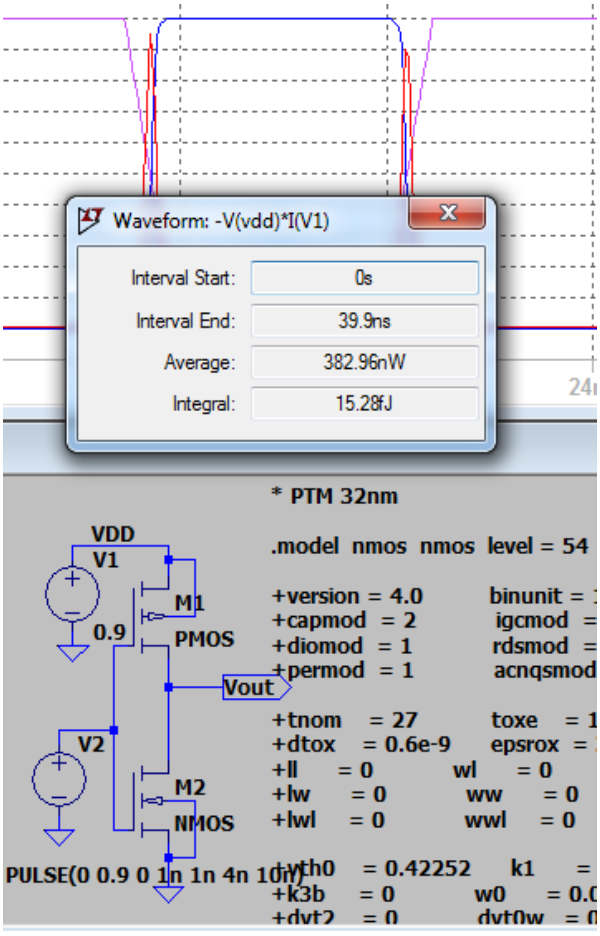

Fig. 5.8: CMOS Inverter at 32nm Barkley PTM technology

The power analysis for the MOSFET inverter using the typical CMOS technique and adiabatic switching is shown in Fig. 5.9. The analysis is performed between operating frequencies of 0–500 MHz with magnitude of both V_{DD} and V_{ϕ} fixed at 0.9V and load capacitor C_L at 0.01pf. From the graph, it can be seen that CMOS consumes the most power and dissipates 40 nW at 500 MHz, whereas the proposed adiabatic logic family of circuits consumed the least power and dissipated approximately 13 nW at 500 MHz. It can be found that at 500 MHz, the proposed circuit has 67.5% power savings compared to typical CMOS. With the same frequency, magnitude of supply voltage, and load capacitor, Fig. 5.10 depicts the power consumption of an inverter circuit using FinFET devices in conventional techniques as well as various adiabatic logic design approaches.

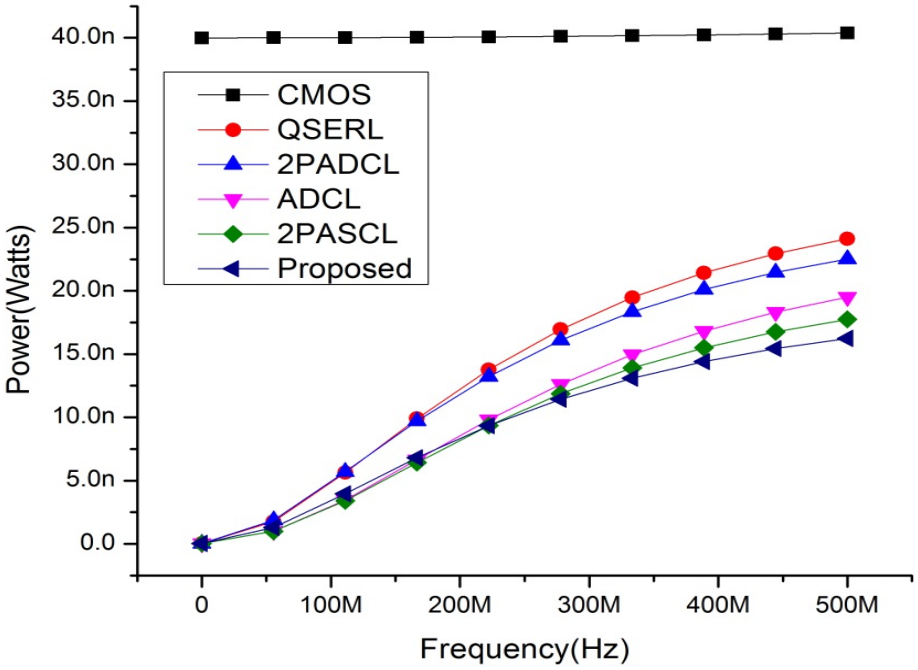

Fig. 5.9: Power analysis of basic inverter using MOSFET

In the case of FinFETs, the power consumption difference between the traditional method and the adiabatic logic technique is quite large.In the case of FinFETs, the power consumption difference between the traditional method and the adiabatic logic technique is quite large. The adiabatic logic family consumes power in the range of pW, while the traditional design method consumes power in terms of nW

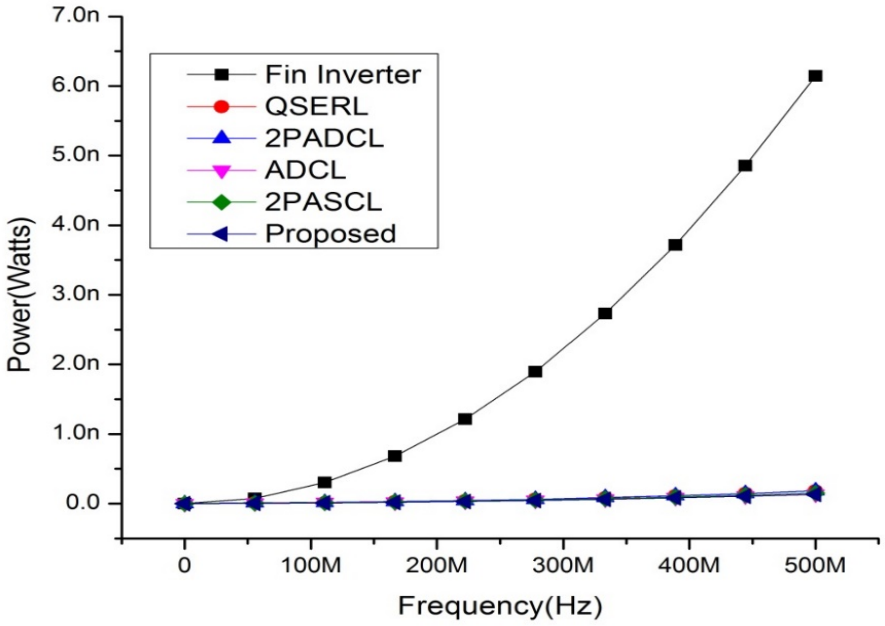

Fig. 5.10: Power analysis of basic inverter using FinFET

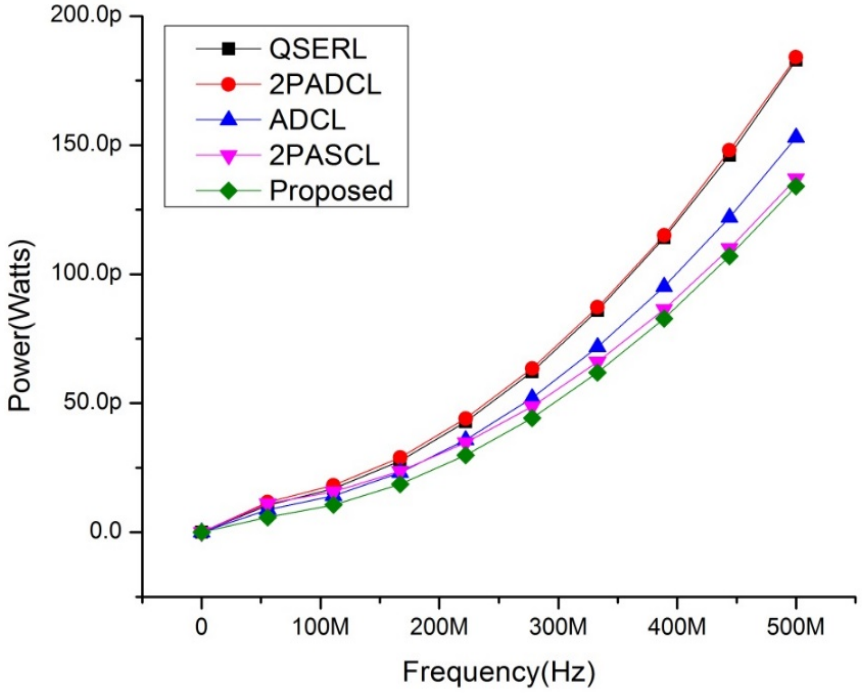

Fig. 5.11: Power analysis of adiabatic basic inverter using FinFET

Since there is a huge difference in power loss, the adiabatic family lies on a straight line as compared to the traditional method, as illustrated in Fig. 5.10. The power consumption of FinFET technology with adiabatic logic design alone is shown in Fig. 5.11. As seen from the graph, the QSERL consumes the most power, while our proposed technique consumes the least power. From Figs. 5.10 and 5.11, the evaluated power saving of the proposed technique as compared with the conventional approach is 97.95% less at 500 MHz. The frequency of the clock voltage in all analyses was fixed at 200 MHz.

5.4. ALU Design Approach

Fundamentally, the ALU is the cornerstone of any computation done by the CPU. It is a combinational digital circuit that performs arithmetic and digital operations. Modern computers have very complex and powerful ALUs. Augmented digital signal processing and computer applications have a higher demand for low-power operations. The throughput of ALU needs to be high for better performance in any signal processing application (Sharma & Tiwari, 2016; Shylashree et al., 2019). This chapter presents a 16-bit ALU derived from the basic 1-bit ALU. It has four functions: one arithmetic operation and three logical operations. We intended to investigate and analyze the performance of a novel prototype 16-bit ALU realized from a basic 1-bit ALU in terms of its power savings and a PDP using a FinFET device incorporating the adiabatic logic technique. A larger number of operations can be added by increasing the size of the multiplexer used and signaling select lines. Figs. 5.12 and 5.13 show the symbol of the 16-bit ALU and the block diagram of the basic 1-bit ALU.

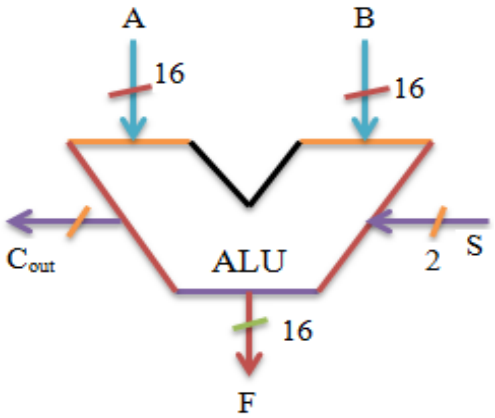

Fig. 5.12: 16-bit ALU

Table 5.1 shows the truth table of a basic 1-bit ALU. The logical operations include AND, OR, and NAND, apart from the single arithmetic full-adder operation. One 4:1 multiplexer is used to select the operations and carry the evaluated input to output terminal F.

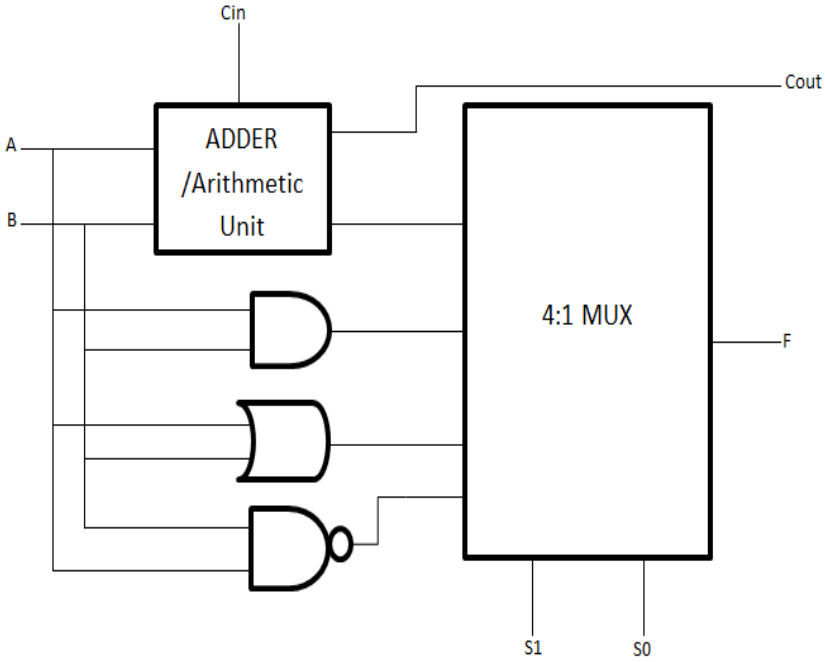

Fig. 5.13: Block diagram of basic 1-bit ALU

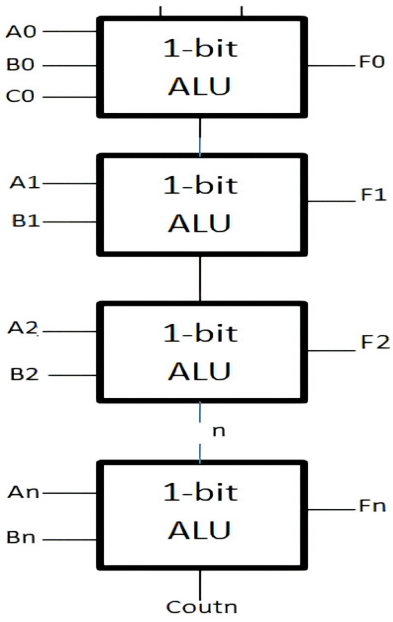

Fig. 5.14: Block diagram of n-bit ALU by cascading 1-bit ALU

The block diagram of an n-bit ALU is shown in Fig. 5.14. It is obtained by combining a single 1-bit ALU in such a manner that the carry output (C_{out}) of the first 1-bit ALU block is connected to the next block as C_{in}, and so on until the last block. By cascading, we can configure an n-bit ALU. Fig. 5.15 shows the proposed 1-bit FinFET-based ALU, and input and output waveforms are generated as per the truth table. The structure and shape of the output signal could be affected by the value of the load capacitance. The character of the output is analogous to a sinusoidal pattern (Kumar et al., 2017; Samanta, 2010; Konwar et al., 2014). In Fig. 5.15, each module such as Adder, AND, OR, NAND, and MUX in the ALU block can be seen distinctly. The cascading of 1-bit ALU for 16-bit ALU is illustrated in Fig. 5.16. FinFETs are connected in LP mode for optimum power utilization. All waveform results in Fig. 5.16 can be checked directly in accordance with the truth table as shown in Table 5.1.

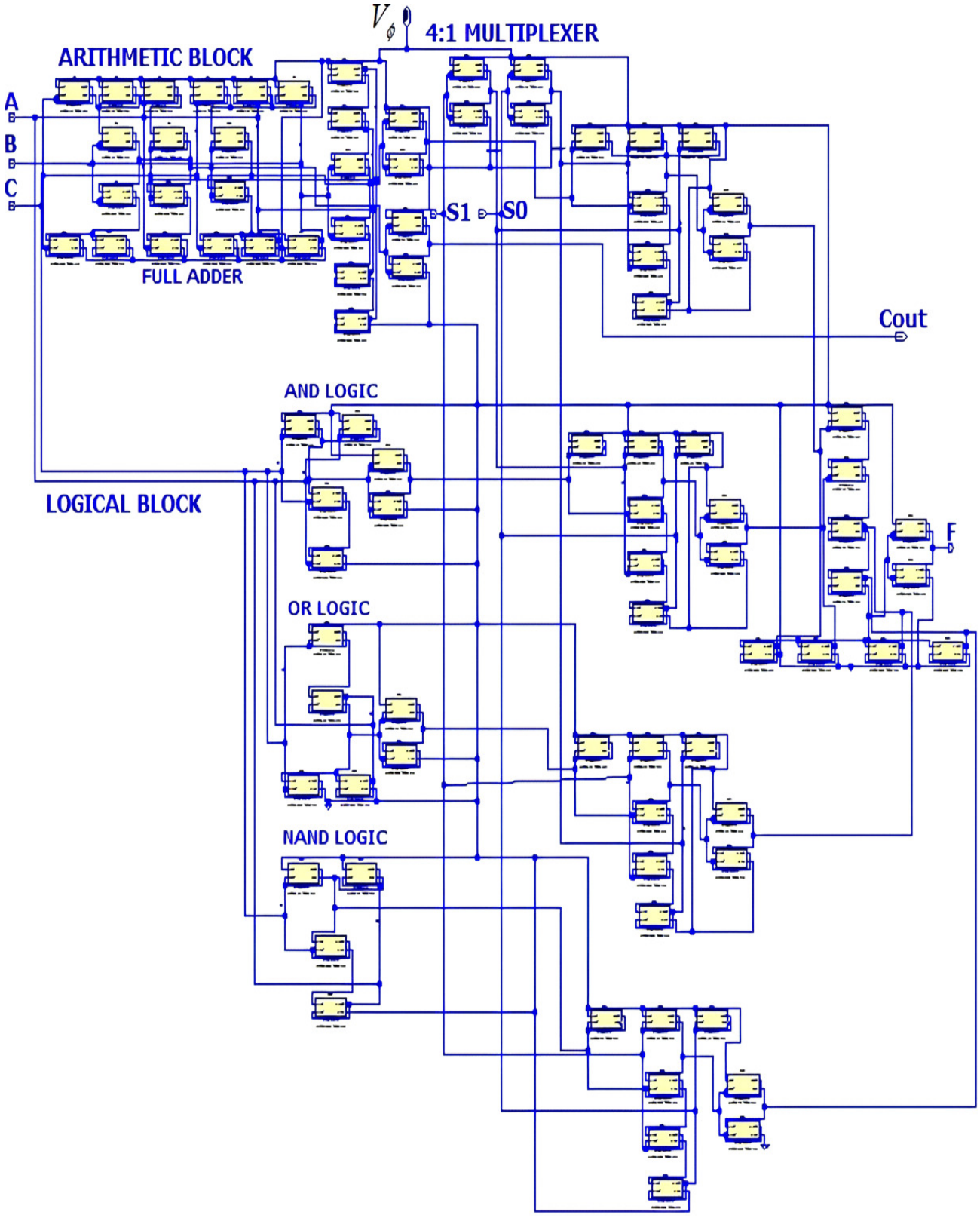

Fig. 5.15: Proposed 1-bit ALU using FinFET

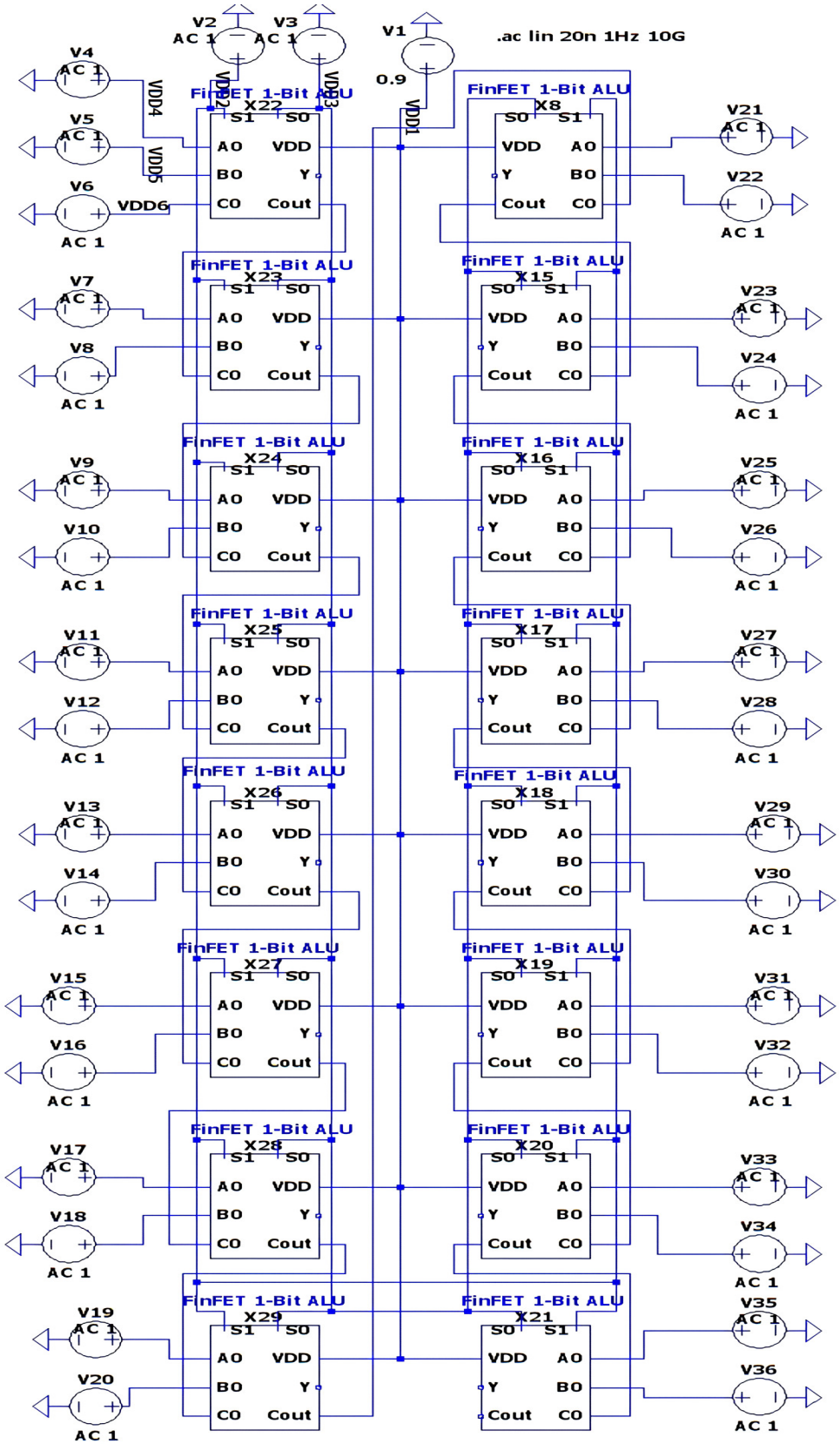

Fig. 5.16: Proposed 16-bit ALU using FinFET

Table 5.1: Truth Table of Basic 1-Bit ALU

S1	S0	Function	
0	0	Arithmetic Unit	FULL ADDER
0	1	Logic Unit	AND
1	0	Logic Unit	OR
1	1	Logic Unit	NAND

5.5. Results and Discussion

The power usage evaluations were conducted using SPICE and NI Multisim-14.1, using 32nm node technology (MOSFET and FinFET). According to many studies (Dadoria & Khare, 2019; Kumar et al., 2017; Yuejun et al., 2018; Houri et al., 2015), the SPICE net-lists for both the MOSFET and FinFET are maintained as follows: $V_{DD} = 0.9V$ and $V_{\phi} = 0.9V$ at $500\,MHz$, $C_L = 0.01pf$, and a logic input of $V_{in} = 0.9V$.

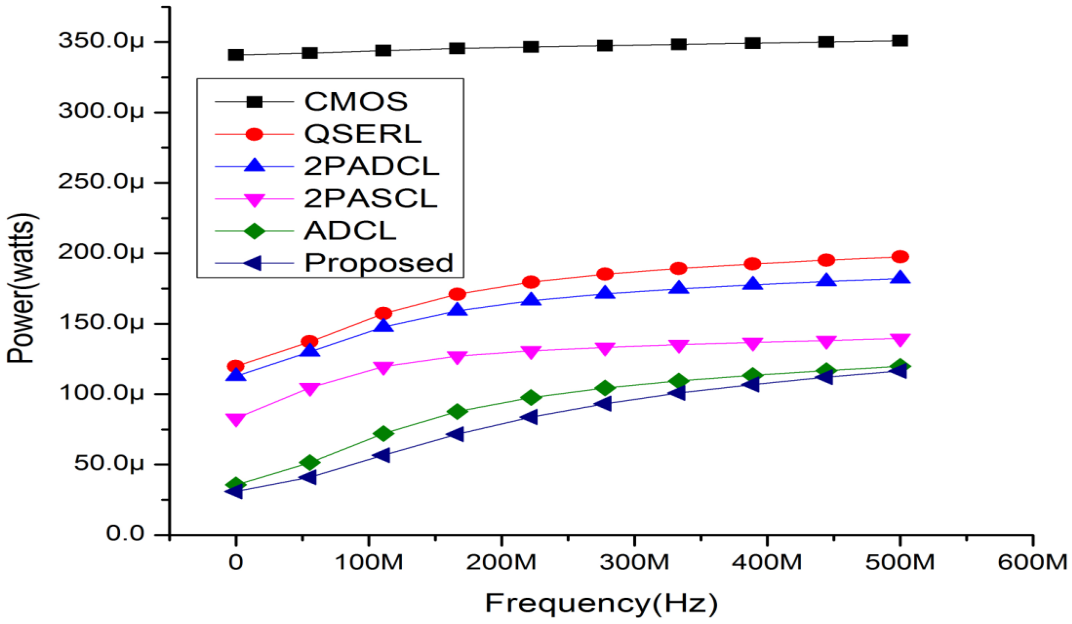

Fig. 5.17: Power evaluation of 16-bit ALU using MOSFET

The analysis of power consumption versus operating frequency of MOSFETs in traditional approaches and adiabatic logic styles for 16-bit ALU is shown in Fig. 5.17. Fig. 5.18 shows the power analysis for FinFET-based ALU in the adiabatic logic approach. Fig. 5.19 mentions FinFET-

based 16-bit ALUs in conventional and adiabatic logic design approaches. Adiabatic families employed are standard or fully adiabatic and show better performance in terms of power utilization.

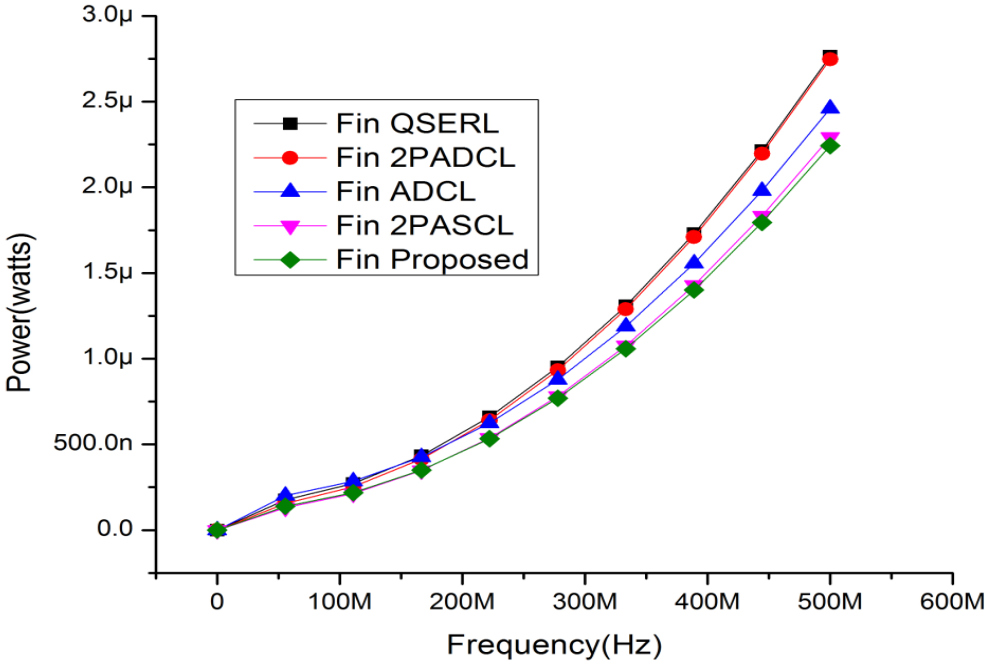

Fig. 5.18: Power evaluation of adiabatic 16-bit ALU using FinFET

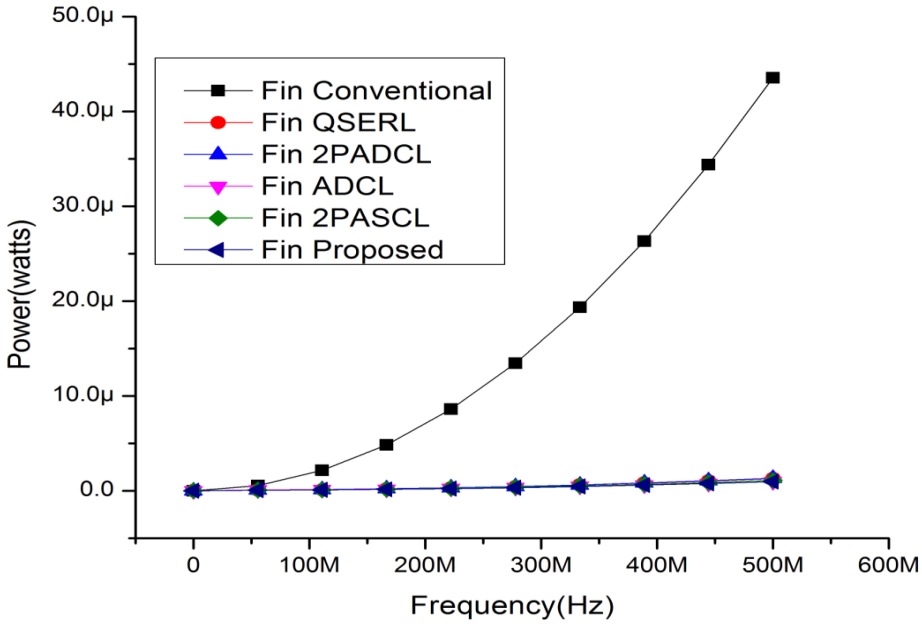

Fig. 5.19: Power evaluation of 16-bit ALU using FinFET

Table 5.2 and Table 5.3 depict the comparison tables of various parameters (transistor count, area occupancy, and power dissipation at 500 MHz) for traditional style CMOS, QSERL, 2PADCL, ADCL, 2PASCL, and the proposed logic as well as FinFET based conventional designs.

Table 5.2: Performance of different logic styles for 16-bit ALU (MOSFET)

Parameter	CMOS Logic	QSERL Logic	2PADCL Logic	ADCL Logic	2PASCL Logic	Proposed Logic
Transistor count	1440	1504	1472	1472	1472	1456
Area per chip (μm^2)	3.68	3.85	3.76	3.90	3.76	3.72
Total power consumption (µW) [at 500MHz]	350	190	176	126	120	115

Tables 5.2 and 5.3 depict the comparison tables of various parameters (transistor count, area occupancy, and power dissipation at 500 MHz) of the ALU circuit design using both MOSFET and FinFET devices, incorporating both conventional design-style and CMOS design techniques, as well as various adiabatic design methodologies such as QSERL, 2PADCL, ADCL, 2PASCL, and the proposed logic.

Table 5.3: Performance of various logic techniques for 16bit ALU (FinFET)

Parameter	Conv. Logic	QSERL Logic	2PADCL Logic	ADCL Logic	2PASCL Logic	Proposed Logic
Transistor count	1440	1504	1472	1472	1472	1456
Area per chip (μm^2)	3.68	3.85	3.76	3.90	3.76	3.72
Total power consumption (µW) [at 500MHz]	44	2.67	2.65	2.49	2.3	2.1

The results show that the proposed circuit consumes the least power in both MOS and FinFET-based designs. Tables 5.4 and 5.5 depict the comparison of power savings of the proposed logic for 16-bit ALU at 500 MHz for MOSFET-based traditional style as well as FinFET-based conventional style. Power-saving percentages for MOSFET and FinFET technologies for various logics are shown in Table 5.6.

Table 5.4: Power saving (in %) for proposed logic (MOSFET) at 500 MHz

CMOS	QSERL	2PADCL	ADCL	2PASCL
67.14%	39.47%	34.65%	8.73%	4.16 %

Table 5.5 *Power saving (in %) for proposed logic (FinFET) at 500 MHz*

Conventional	QSERL	2PADCL	ADCL	2PASCL
95.22%	21.34%	20.75%	15.66%	8.69%

Table 5.6: Power saving (in %) from MOSFET to FinFET

CMOS	QSERL	2PADCL	ADCL	2PASCL	Proposed
85%	98.59%	98.49%	98%	98%	98.17%

At 500 MHz, the proposed ALU design has power savings of 67.14%, 39.47%, 34.65%, 8.73%, and 4.16% as compared with CMOS, QSERL, 2PADCL, ADCL, and 2PASCL on MOSFET technology. Compared to FinFET technology, the proposed ALU design saves 95.22%, 21.34%, 20.75%, 15.66%, and 8.69%, respectively.

5.6. Summary

In this chapter, we introduce a novel 16-bit ALU based on FinFET technology that incorporates the adiabatic switching principle. Our investigation utilizes the 32-nm Barkley PTM technology for both FinFET and MOSFET. The prototype ALU, designed with adiabatic logic and FinFET technology, encompasses four functions: one arithmetic operation and three logical operations. Notably, additional functions can be accommodated by increasing the multiplexer size. The results obtained demonstrate the superiority of FinFET-based design when compared to other techniques. Specifically, the incorporation of adiabatic techniques yields substantial power savings across various technologies: 85%, 98.59%, 98.49%, 98%, 98%, and 98.17% for CMOS, QSERL, 2PADCL, ADCL, 2PASCL, and the proposed circuit. Furthermore, when comparing power efficiency and energy optimization, FinFET technology surpasses MOSFET. One intriguing strategy for low-power VLSI design is to combine digital CMOS with adiabatic logic types used by FinFET devices. Notably, compared to other adiabatic logic circuits in the literature, our suggested design has the smallest effective area per chip and the lowest power usage. Consequently, it holds significant advantages for low-power VLSI circuits.

CHAPTER 6

Efficient Low-Power Circuits With Enhanced Positive Feedback Adiabatic Logic (EPFAL)

6.1. Introduction

Enhanced Positive Feedback Adiabatic Logic (EPFAL) is a brand new, innovative family of adiabatic logic designed for applications requiring minimal power. Based on two-phase sinusoidal power-clock sources, suggested circuit's dual-rail encoded and sense-amplifier-structured quasi-adiabatic circuits provide two supplementary outputs. A part of the energy that is recovered through the evaluation process is reused for subsequent calculations by the quasi-adiabatic switching circuits. Efficiency of this circuit is defined by the adiabatic and non-adiabatic losses it undergoes during charging and recovery. Controlling these losses is a process including the operating frequency, charge sharing, leakage effects, and the remaining charge trapped in the floating internal circuit nodes. Suggested EPFAL circuits reduce power loss by enhancing charge recovery and decreasing peak current flow. We determined overall power loss of the EPFAL inverter circuit by studying its behavior, modeling its charging RC analogous circuit, and drawing analytical conclusions. For basic gates like inverter/buffer, NOR/OR, XNOR/XOR, and NAND/AND, we look at dynamic power usage since adiabatically powered logic operation is better when power conservation is of greater significance than processing speed for the device's performance. By using an adiabatic design procedure, low-frequency-powered devices like sensors, smart cards, and RFIDs may be enhanced. Building on the EPFAL, we build and study checker circuits, parity generators (both even and odd), and more. The analysis results demonstrate that the suggested EPFAL circuit outperforms existing reference circuits and has significantly reduced average power consumption. The simulations were performed using Cadence Virtuoso, utilizing the Low Power Berkeley Predictive Technology Model (45 nm LP_PTM) at various operating frequencies. The recommended EPFAL circuits reduce average power consumption in the odd parity generator circuit by 82.14% and in the checker circuit by 77.53% compared to conventional CMOS design methods.

The proliferation of handheld electronics is directly linked to the recent development of portable and wearable electronic devices. More and more, sophisticated digital technologies are being used by portable gadgets that are Wi-Fi capable. System architecture, increasing integration densities, and putting more attention on energy savings are now the most essential concerns. The need to reduce power loss is a major obstacle in the design of high-performance circuits for applications such as mobile devices (Chanda et al., 2015; Nayan et al., 2012). Traditional CMOS circuits use voltage scaling to cut down on power consumption. However, it is difficult and predictable to scale down MOS devices to nanoelectronics since unacceptable short-channel effects (SCEs) have been reported (Panchanan et al., 2021). In addition, it has significant drawbacks, while lowering the transistor threshold voltage causes a much higher subthreshold leakage current (Panchanan et al., 2021; Maity et al., 2017). Additionally, dynamic logic families are recommended for low-power circuit design; nevertheless, this approach necessitates pre-charging the circuit after each evaluation cycle (Uma et al., 2017). Athas et al. (1994) proposed an adiabatic circuit, sometimes called an energy-recovery circuit, as a possible method. Either completely adiabatic or quasi-adiabatic describes it. In order to prevent non-adiabatic loss, fully-adiabatic circuits are additional complex than quasi-adiabatic ones (Bhaaskaran & Raina, 2010). As a further complication, fully adiabatic circuits can have problems with operating speed and power clock synchronization. However, due to the very slow transition, no net gain or loss of heat occurs in completely adiabatic circuits. For this purpose, conventional DC power sources have been superseded with sinusoidal power clocks. One of the most reliable low-power design choices is an energy recovery circuit that uses the adiabatic switching principle. Several quasi-adiabatic architectures for dual-rail outputs, such as ECRL (Moon & Jeong, 1996), PFAL (Vetuli et al., 1996), 2N-2N2P (Chaudhuri et al., 2015; Kramer et al., 1995), 2P-PFAL (Jain et al., 2019), IPGL (Varga et al., 2001), DCPAL (Bhaaskaran & Raina, 2008), CDCAL (Sasipriya & Bhaaskaran, 2018), and A-DCVSL (Gupta et al., 2022), have already been suggested.

6.2. Structure of the Circuit

It consists of a cross-coupled inverter with a back-to-back connection that has created a latch. It therefore forms and generates a dual-rail output, denoting the output as OUT and its complementary output as $\overline{OUT}$. Two sinusoidal power supplies, denoted as V_ϕ and $\overline{V_\phi}$, operate the circuit 180 degrees out of phase. Fig. 6.1 shows that the EPFAL incorporates two additional transistors, M1 and M2, at the top and bottom of the circuit, in addition to the conventional PFAL.

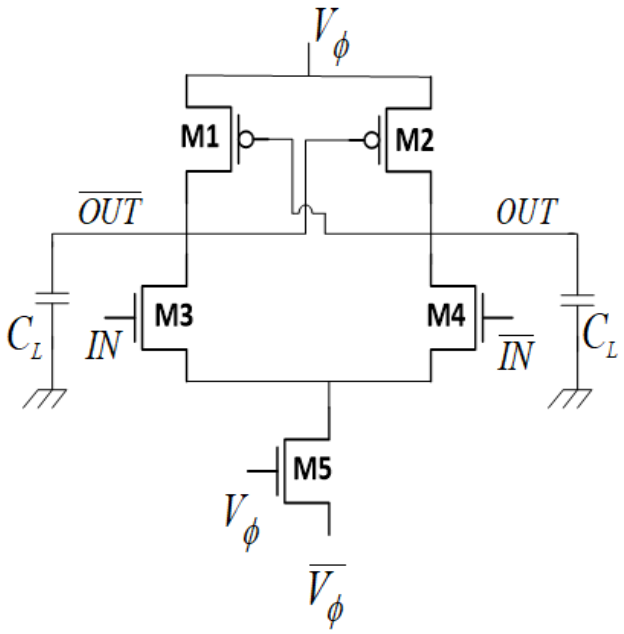

Fig.6.1: Structure of EPFAL

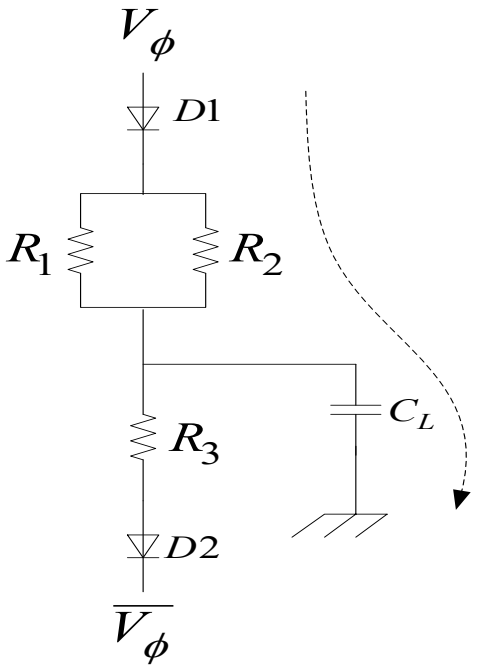

Fig.6.2: RC-diode equivalent circuit of the right side the dual-rail of EPFAL

.

The arrangement of the transistors enables them to act as diodes, controlling the flow of electric charge in one direction and blocking it in the other. We denote the input and its complimentary input as IN and $\overline{IN}$, respectively. The EPFAL circuit reduces the amplitude of each power source to half of the input signal's amplitude (Anuar et al., 2010). The circuit functions using two distinct phases, namely *evaluation* and *hold*. Transistors M1, M5, and M3 charge the load capacitor C_L on the right side of the dual-rail output during the charging phase. Conversely, during the discharging phase, transistors M7 and M8 release the energy that the output node capacitor has stored as charge. The use of parallel transistors M3 and M5 reduces the charging circuit's on-resistance. M1 and M8 function as forward diodes. Figure 6.2 depicts the charging diagram of the right-hand side of the dual-rail circuit, which includes diodes and an RC-equivalent circuit (Jadav & Chandel, 2019).

6.3. Mathematical Analysis

The diodes D1 and D2 are analogous to transistors M1 and M8 in this context. The ON-resistances of transistors M5, M3, and M7 are represented by resistors R1, R2, and R3, respectively. The charge Q is taken via the power source V_ϕ and charged to the load capacitor C_L by means of diode D1 and resistors R1 and R2. This results in a swing in the output voltage at $(V_p - V_d)$ when the

input voltage $IN$is HIGH or logic level 1. In this case, V_p represents the peak voltage of the power supply V_ϕ, while V_d represents the voltage drop at the charging channel diode D1, which is nearly at the diode's operational threshold. Consequently, the total amount of charge that is extracted from the supplied voltage V_ϕ throughout the charging process is presented as (Dickinson & Denker, 1995; Takahashi & Mizunuma, 2000).

$$Q = C_L(V_p - V_d) \tag{6.1}$$

Then, the energy consumed through the diode D_1 is formulated as in Eq. (6.1).

$$E_{D1} = QV_d = C_L(V_p - V_d)V_d \tag{6.2}$$

The energy dissipated in the parallel charging resistances of R_1 and R_2 which is denoted as R_p is represented as,

$$E_{R_p} = i^2 R_p T = \left(\frac{Q}{T}\right)^2 R_p T \tag{6.3}$$

where T is the time period and i represent the current flowing through the parallel resistor R_p

$$E_{R_p} = \frac{(R_p C_L)}{T} C_L(V_p - V_d)^2 \tag{6.4}$$

The total adiabatic energy consumption while charging is given as,

$$E_{Total} = E_{D1} + E_{R_p} \tag{6.5}$$

$$E_{chg} = 2\frac{(R_p C_L)}{T} C_L(V_p - V_d)^2 + 2C_L(V_p - V_d)V_d \tag{6.6}$$

Assuming the ON-resistances of PMOS and NMOS transistors are similar. During discharging, the energy consumed at diode D_2 is similar to the energy consumed at diode D_1 while charging, as shown below as,

$$E_{D2} = QV_d = C_L(V_p - V_d)V_d \tag{6.7}$$

The same charge with the expression: $Q = C_L(V_p - V_d)$, which was loaded in the output node, will be discharged through the pull-down resistor R_3, and the energy dissipated at resistor R_3 is given as,

$$E_{R_3} = i^2 R_3 T = \left(\frac{Q}{T}\right)^2 R_3 T \tag{6.8}$$

$$E_{R_3} = \frac{(R_3 C_L)}{T} C_L (V_p - V_d)^2 \quad (6.9)$$

The total adiabatic energy consumption while discharging is given as,

$$E_{dis-chg} = E_{D2} + E_{R_3} = \frac{(R_3 C_L)}{T} C_L (V_p - V_d)^2 + C_L (V_p - V_d) V_d$$

$$E_{Adb} = E_{chg} + E_{dis-chg}$$

$$E_{Adb} = \left[\frac{(R_p C_L)}{T} C_L (V_p - V_d)^2 + C_L (V_p - V_d) V_d\right] + \left[\frac{(R_3 C_L)}{T} C_L (V_p - V_d)^2 + C_L (V_p - V_d) V_d\right]$$

$$= 2C_L (V_p - V_d) V_d + \frac{(R_p C_L)}{T} C_L (V_p - V_d)^2 + \frac{(R_3 C_L)}{T} C_L (V_p - V_d)^2 \quad (6.10)$$

$Let R_p \approx R_3 = R_{on}$, and assuming that the ON resistances of NMOS and PMOS transistors are identical, the resistor on the charging and discharging paths is denoted as R_{on}. Therefore,

$$E_{Adb} = 2\frac{(R_{on} C_L)}{T} C_L (V_p - V_d)^2 + 2C_L (V_p - V_d) V_d \quad (6.11)$$

The overall energy lost is given as (Bhaaskaran & Raina, 2010),

$$E_{Total} = E_{adb} + E_{PMOS,Latch} + E_{Leak} \quad (6.12)$$

$$E_{PMOS,Latch} = E_{Non-Adb} + E_{Open} \quad (6.13)$$

The non-adiabatic loss, as mentioned in (Moon & Jeong, 1996),

$$E_{Non\_Adb} = \frac{1}{2} C {V_{tp}}^2 \quad (6.14)$$

In every cross-couple, sense-amplifier-based dual rail adiabatic circuit, according to Sathe et al. (2005),

$$E_{open} = \frac{\pi^2}{2T} R_{on} (V_p - V_d) C_L \quad (6.15)$$

The charging path resistance of EPFAL can be approximated as (Sathe et al., 2005),

$$R_{on} = \left[\mu_{eff,p} C_{ox} \left(\frac{W_{eff,p}}{L_{eff,p}}\right) (V_\phi - 2|V_{th}|)\right]^{-1} \quad (6.16)$$

The leakage energy can be related (Bhaaskaran, 2011; Maksimovicl et al., 1997).

$$E_{Leak} \approx (V_p - V_d) I_{Leak} kT \quad (6.17)$$

The voltage swing at the output node is referred to as $(V_p - V_d)$. Hence, the total energy usage of an EPFAL circuit may be estimated as,

$$E_{Total} = 2\frac{(R_{on}C_L)}{T}C_L\left(V_p - V_d\right)^2 + 2C_L\left(V_p - V_d\right)V_d + \frac{1}{2}CV_{tp}{}^2 + \frac{\pi^2}{2T}R_{on}\left(V_p - V_d\right)C_L + \left(V_{dd} - V_d\right)\mu C_{ox}\left(\frac{W}{L}\right)V_T{}^2 \exp\left(V_{gs} - V_{th}/\eta V\right)kT \quad (6.18)$$

6.4. Adiabatic logic family employed in the work

This study uses a number of well-known reference transistor-based adiabatic logic families, as already mentioned in section 6.1. Figs. 6.3–6.10 depict the corresponding fundamental inverter circuits for ECRL, PFAL, 2N-2N2P, IPGAL, 2P-PFAL, CDCAL, A-DCVSL, and DCPL. In these dual-rail encoded adiabatic logic circuits, the sense-amplifier structure is used for charging and recovering. Fig. 6.3 depicts a cross-coupled pair of PMOS transistors of ECRL inverter, an NMOS tree used to build logic operations, and the corresponding function. An ECRL cascade requires a 90-degree phase shift between the first and last power clocks. The CV_{tp}^2 circuit experiences non-adiabatic power loss throughout the processes of charging and recovery, which is caused by the PMOS threshold voltage. PFAL utilizes a pull-up network for logic implementation, as opposed to ECRL and 2N-2N2P, which use pull-down networks. Each group of PMOS transistors has the ability to charge one of two output nodes at the same time, which decreases the resistance and power loss. In order to achieve optimum performance, the PFAL cascade need an equal power clock to the ECRL. Node coupling is not allowed due to the absence of any freely moving nodes in the circuit, save for those generated by the PMOS threshold limit. Furthermore, PFAL exhibits substantial power loss due to leakage. Figure 6.4 depicts the circuit diagram of a PFAL inverter. In contrast, the 2N-2N2P logic family employs a cross-coupled inverter circuit, as seen in Fig. 6.5, to generate an adiabatic amplifier. This amplifier is both quicker and more energy-efficient compared to the ECRL. During the hold phase, the presence of parallel channels formed by NMOS transistors results in a decrease in resistance. For best performance in a 2N-2N2P cascade, it is necessary to have four power clocks, such as the ECRL. Figure 6.6 illustrates the concept of an IPGL inverter construction. To minimize the area overhead, IPGL restricts non-adiabatic loss during the clock's charging phase, but may tolerate some non-adiabatic loss during the clock's recovery phase.

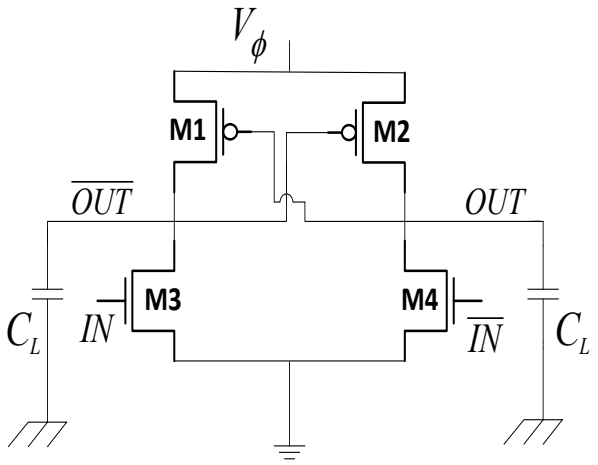

Fig.6.3: ECRL Inverter

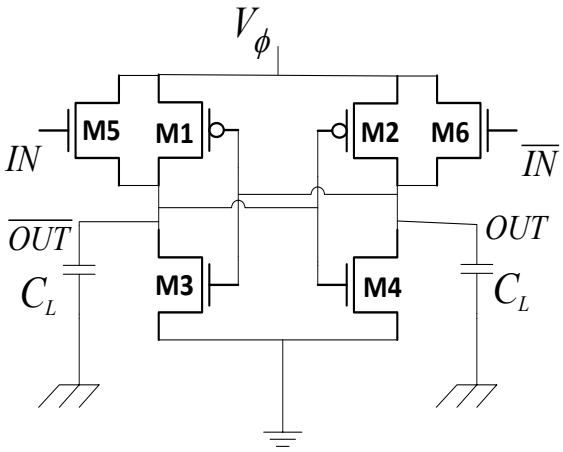

Fig.6.4: PFAL Inverter

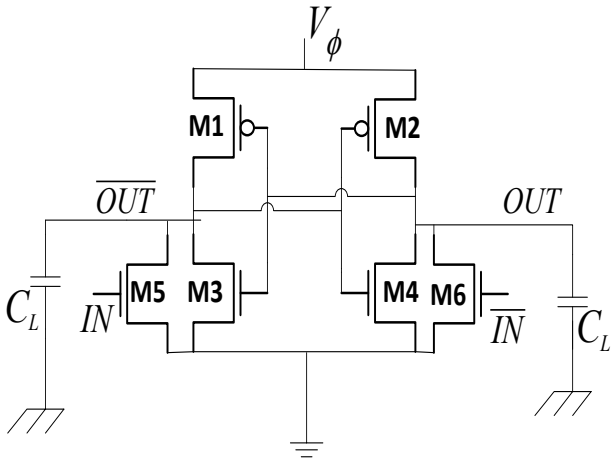

Fig.6.5: 2N-2N2P Inverter

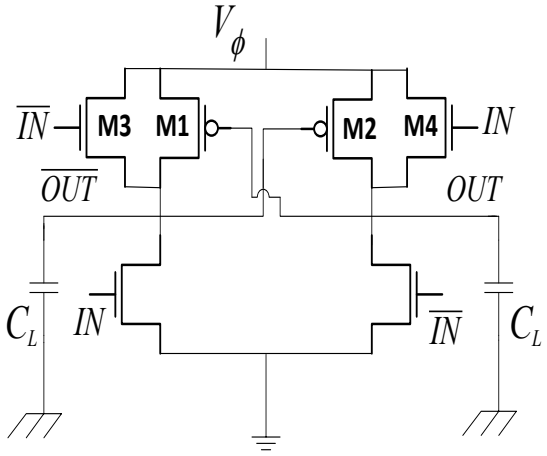

Fig.6.6: IPGAL Inverter

The architectural structure of IPGAL requires a larger number of devices and a higher C_L in order to carry out complex logic operations. This is one of the disadvantages of IPGAL. Figure 6.7 depicts the configuration of a 2P-PFAL inverter. Although the 2-Phase PFAL utilizes two supply voltages that are complimentary and have a phase difference of 180 degrees, the power sources themselves are not split-level sinusoidal supplies. Consequently, the 2-phase PFAL exhibits a lesser benefit in average power usage when compared to other systems using split-level power supplies. Figure 6.8 displays the schematic of the CDCAL inverter. It is affected by the disadvantage of the output of floating nodes. Complex digital circuits implemented using CDCAL may have performance challenges due to this factor. The A-DCVSL circuit is formed by using a two-phase power clock and an extra NMOS transistor in the footer.

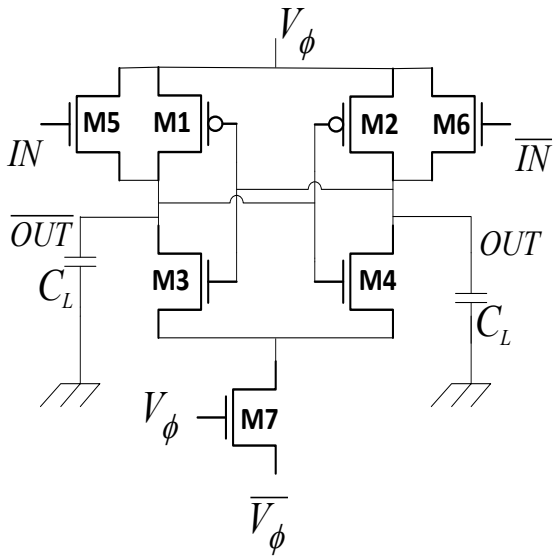

Fig.6.7: 2P-PFAL Inverter

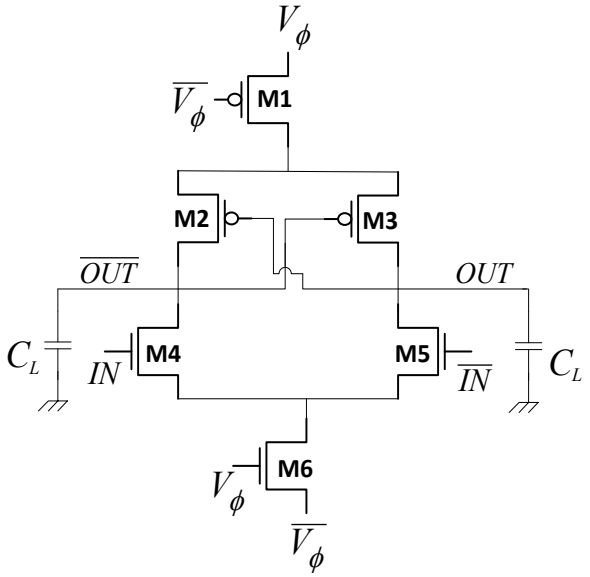

Fig.6.8: CDCAL Inverter

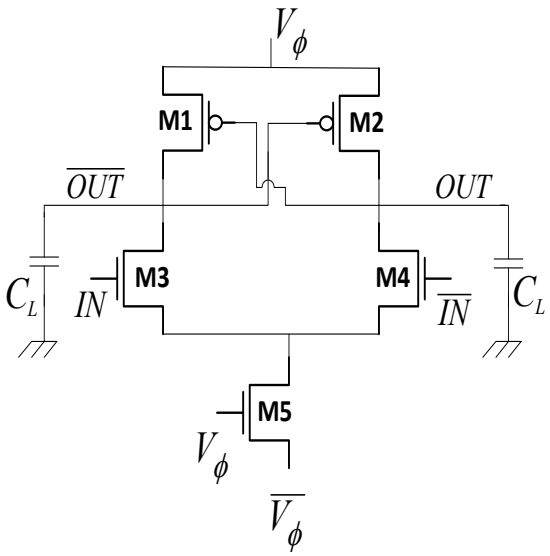

Fig.6.9: A-DCVSL Inverter

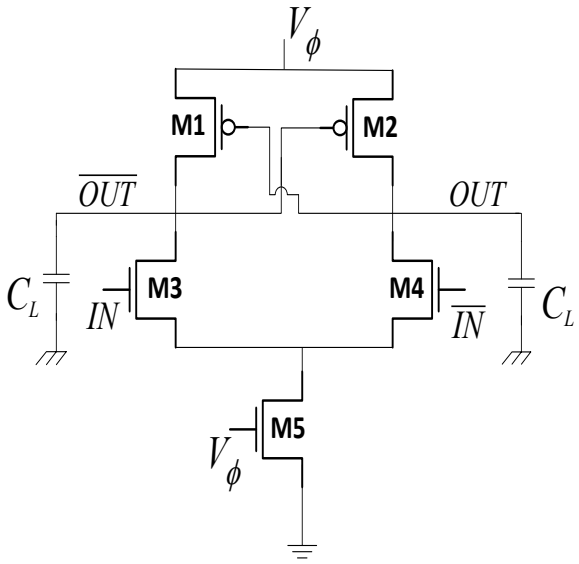

Fig.6.10: DCPAL Inverter

Figure 6.9 displays a split-level sinusoidal power supply and a generalized A-DCVSL gate design. $V_\phi$is responsible for regulating and releasing the output from the NMOS in the footer. Compared to other adiabatic logic families, it consumes much less current to discharge the output node, leading to energy conservation. An inherent limitation of the A-DCVSL circuit is its use of dynamic power during transitions from low to high or high to low states (Gupta et al., 2022). Due to the presence of leakage routes from V_{DD} to ground in the circuit design structures of DCPAL,

leakage loss of power is unavoidable. The inverter architecture of DCPAL can be seen in Fig. 6.10. However, in the case of EPFAL, the utilization of split-level sinusoidal power supplies V_ϕ and $\overline{V_\phi}$ at the pull-up network and pull-down network leads to a noteworthy reduction in leakage power. Furthermore, the presence of parallel PMOS in the pull-up network of the EPFAL results in a decrease in its R_{on} value, thereby minimizing dynamic power consumption.

6.5. Circuits Simulations

Figure 6.11 shows how the average power usage of each basic gate and combinational circuit has been calculated in Cadence Virtuoso's analog design environment, and it also shows the design factors, analysis arguments, average power usage, and simulation model file, which has a 45 nm LP_PTM running at 100 kHz and with simulation times varying from 0 to 80 µm. The complimentary outputs of each basic gate are achieved by using a cross-coupled sensing amplifier in conjunction with dual rail outputs.

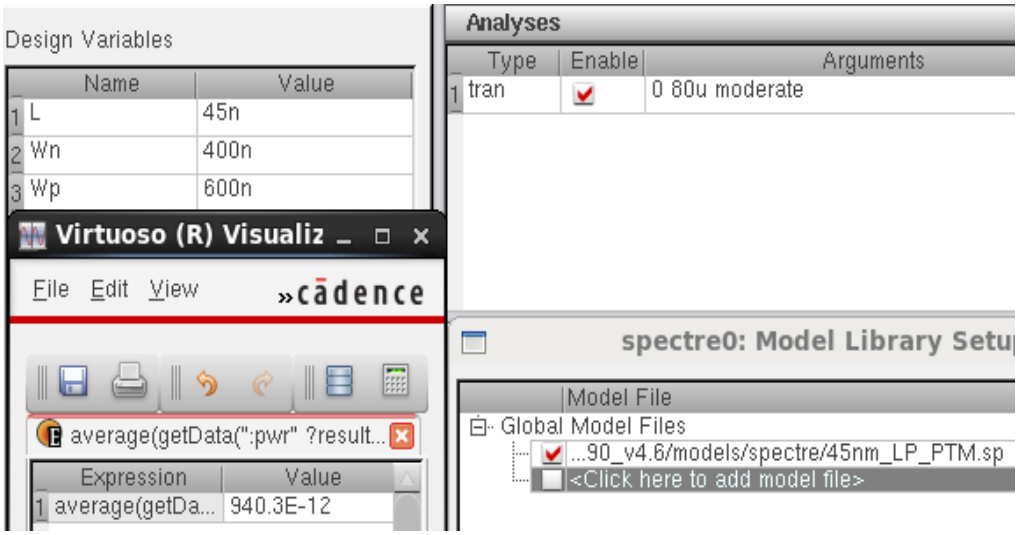

Fig. 6.11: Simulation model and EPFAL Inverter average power Consumption at 100 kHz in analogue design environment.

The EPFAL circuit is related to PFAL circuit excluding for the transistors M1 and M2, which are shown in Fig. 6.1. The EPFAL also incorporates a two-phase sinusoidal power supply V_ϕ and $\overline{V_\phi}$ communicates with pull-up and pull-down networks for control of discharge and charge. Consequently, EPFAL utilizes NMOS transistors parallel to PMOS within the pull-up network for the construction of every functional logic.

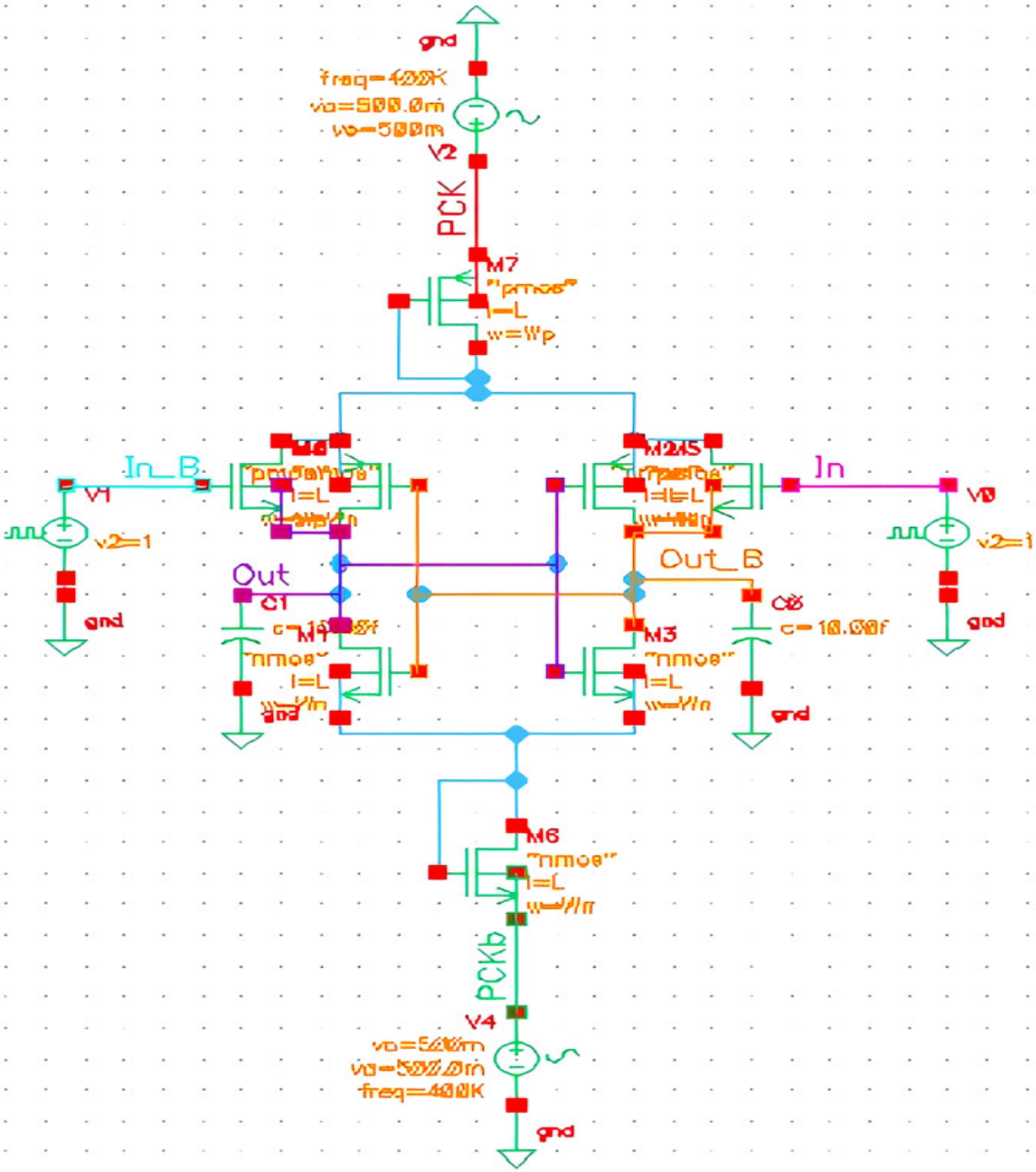

Fig.6.12: EPFAL Inverter/Buffer Circuit

Illustrated in Figs. 6.12 and 6.13 are the inverter and buffer configurations adopted by EPFAL, along with corresponding simulation outcomes. Figure 6.14 elucidates the NAND/AND circuit implemented via EPFAL, while the simulation waveform is represented in Fig. 6.15. Figures 6.16 and 6.17 provide an overview of the NOR/OR circuit integrated into the EPFAL design, complemented by simulation waveforms. The XNOR/XOR diagram, along with EPFAL simulation waveforms, are showcased in Figs. 6.18 and 6.19. Notably, simulations are conducted at a frequency of 400 kHz, utilising 45 nm LP-PTM technology.

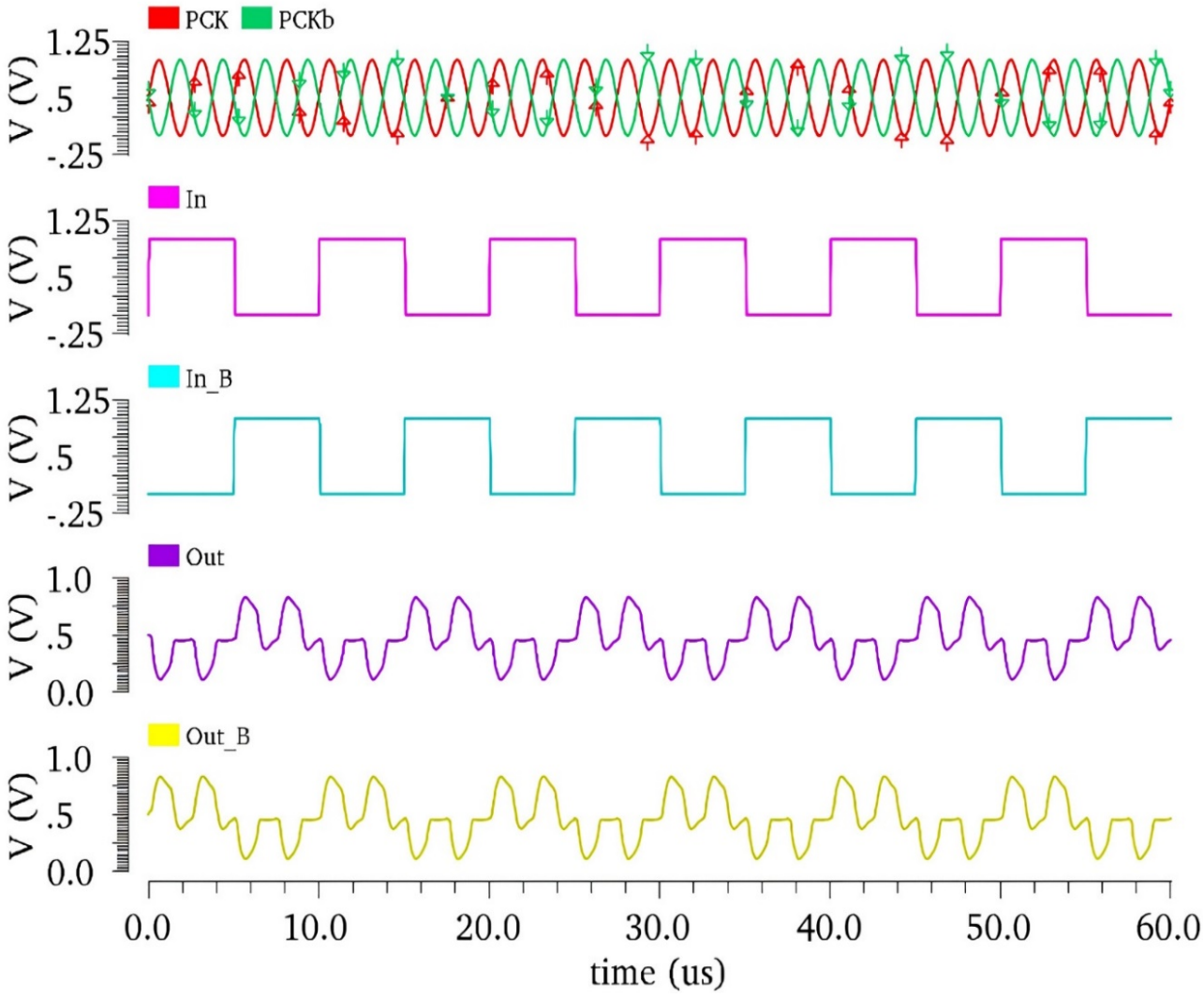

Fig.6.13: Waveform of the EPFAL Inverter/Buffer Circuit

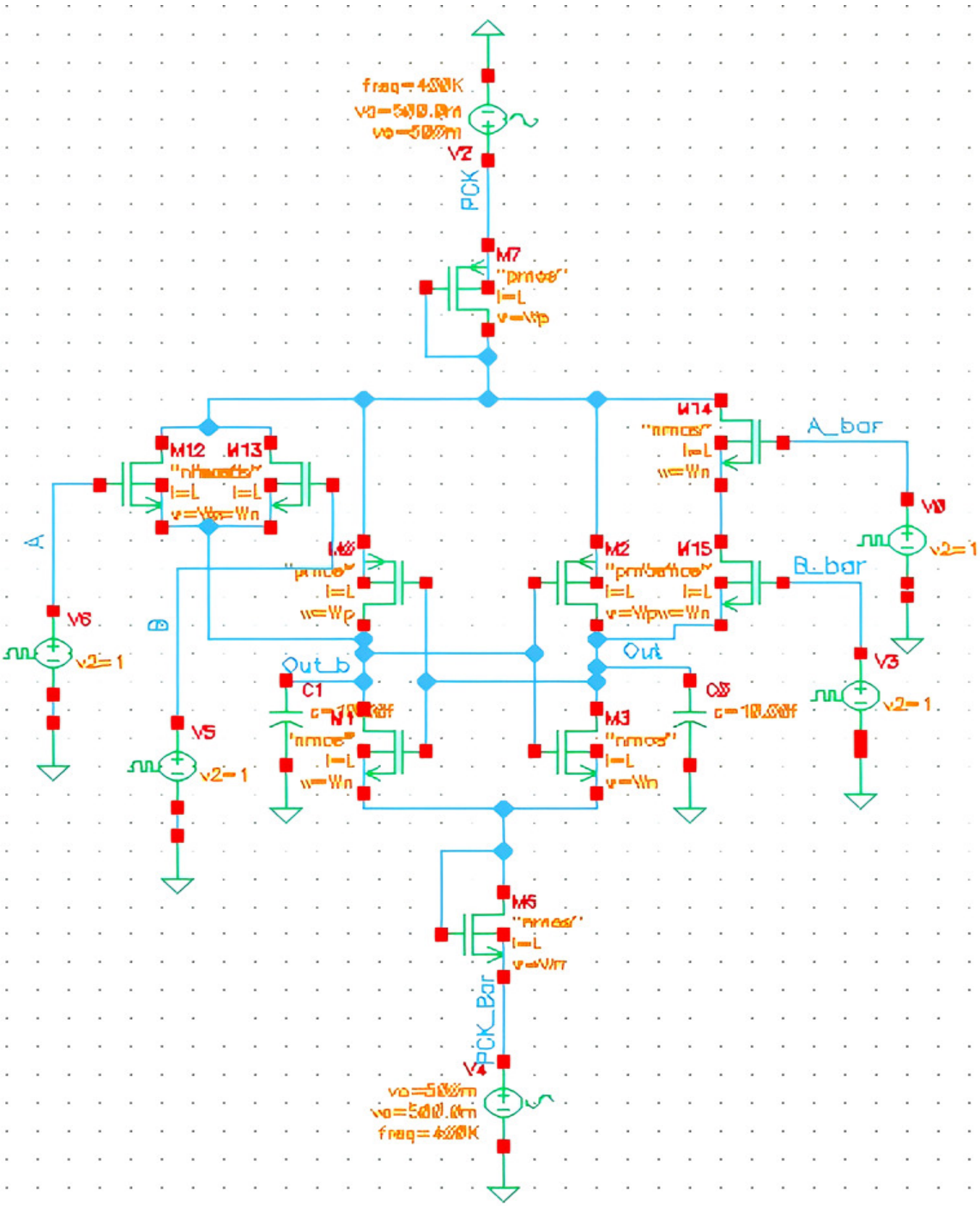

Fig.6.14: EPFAL NAND/AND Circuit

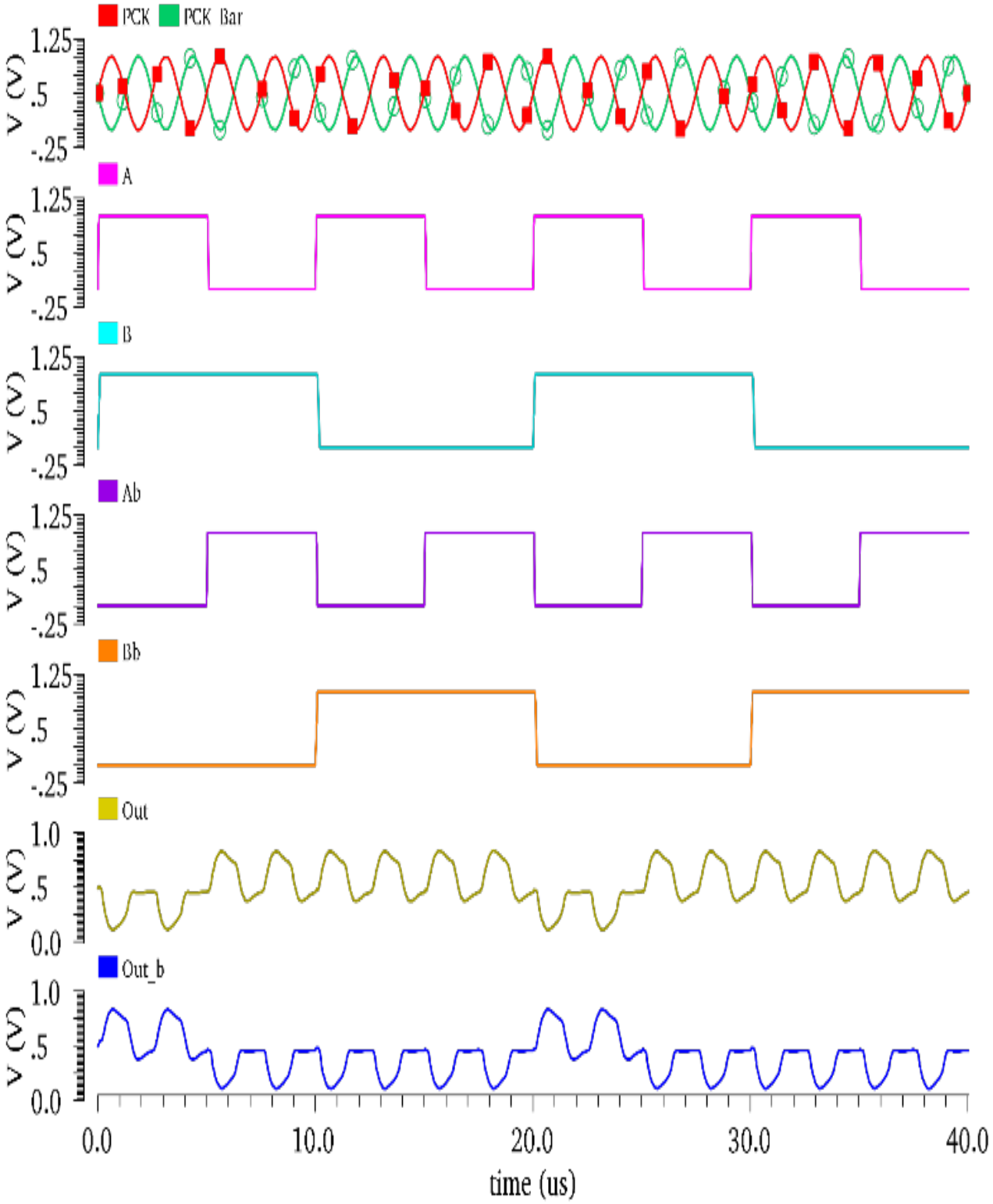

Fig.6.15: Waveform of the EPFAL NAND/AND Circuit

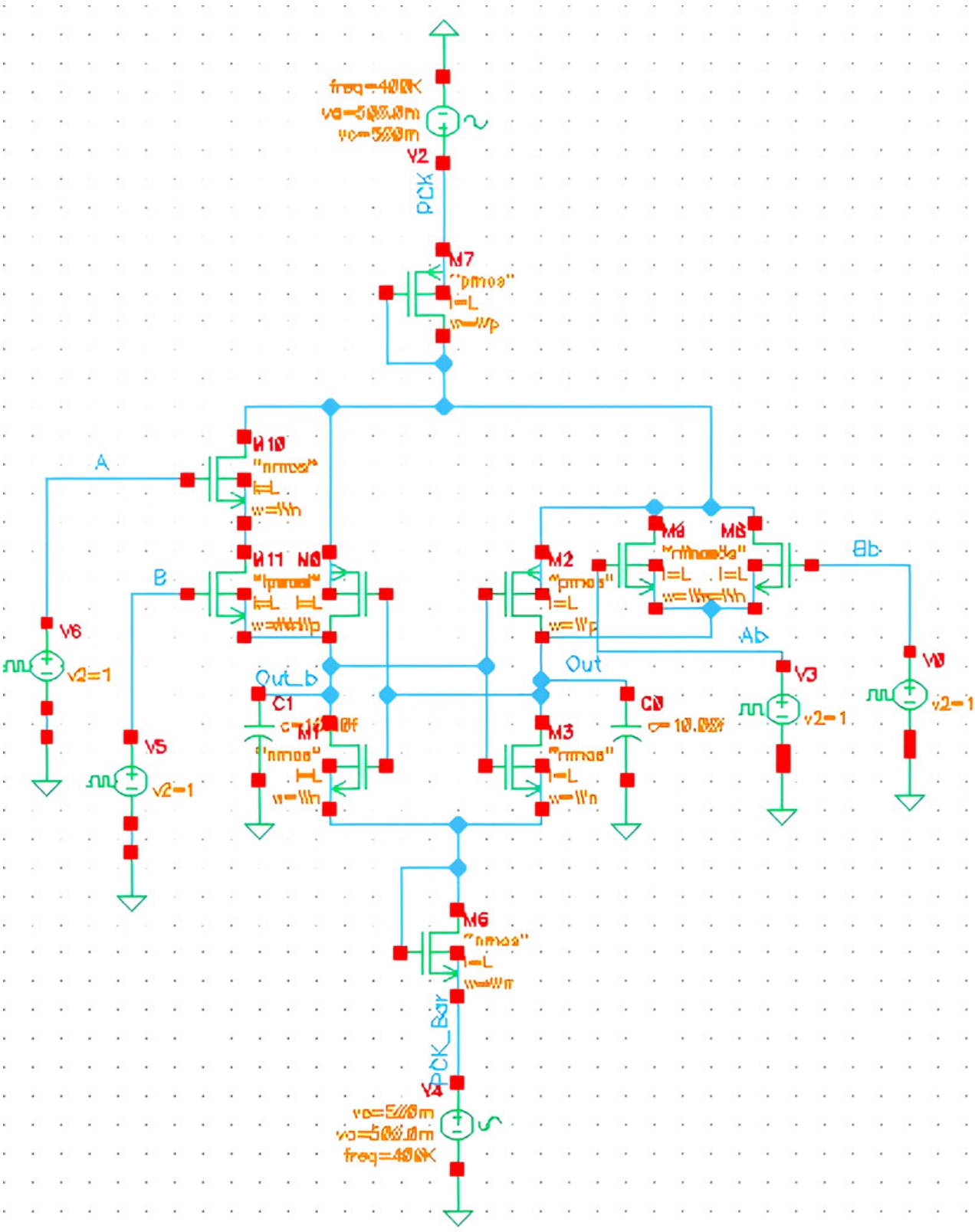

Fig.6.16: EPFAL NOR/ OR Circuit

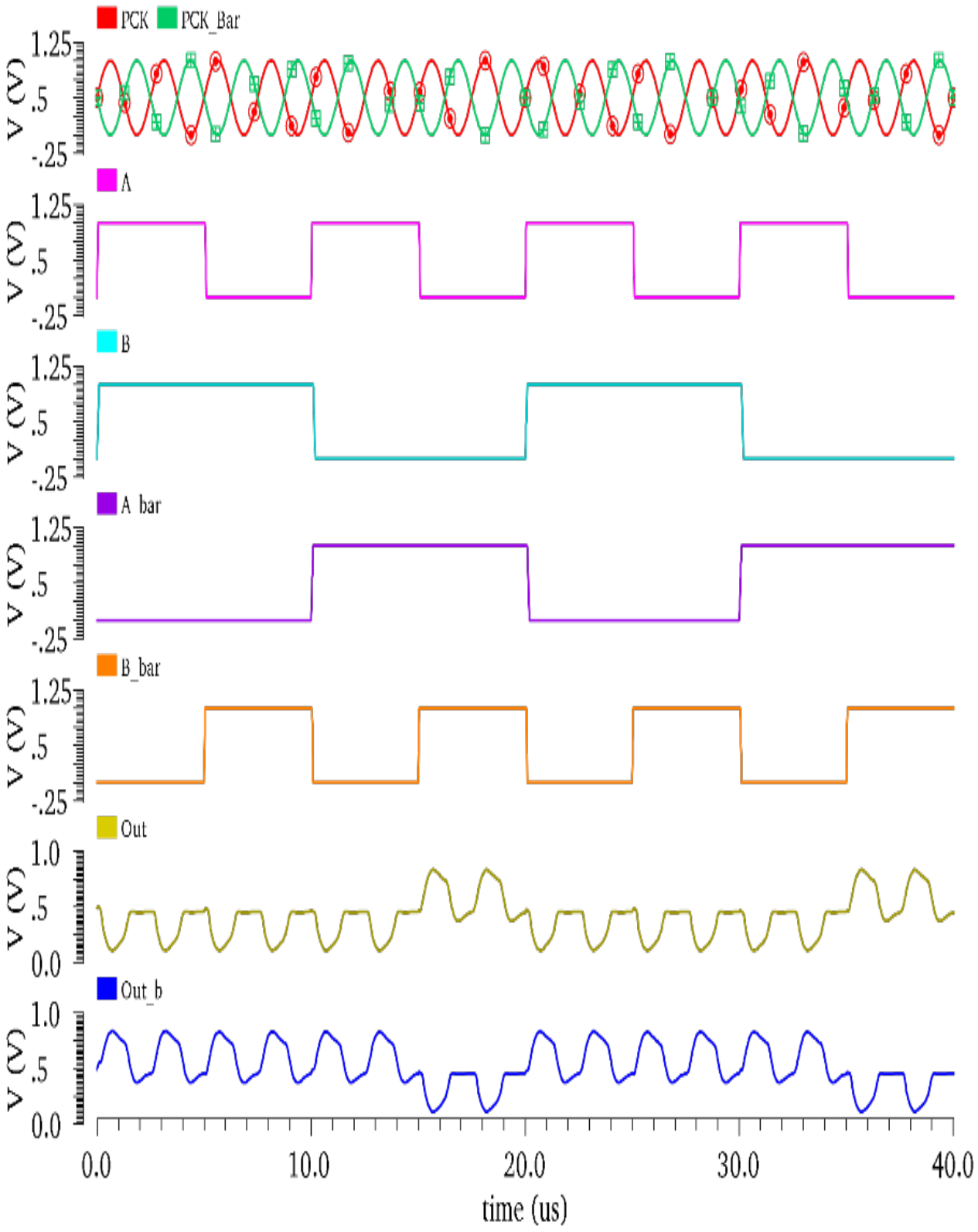

Fig.6.17: Waveform of the EPFAL NOR/OR Circuit

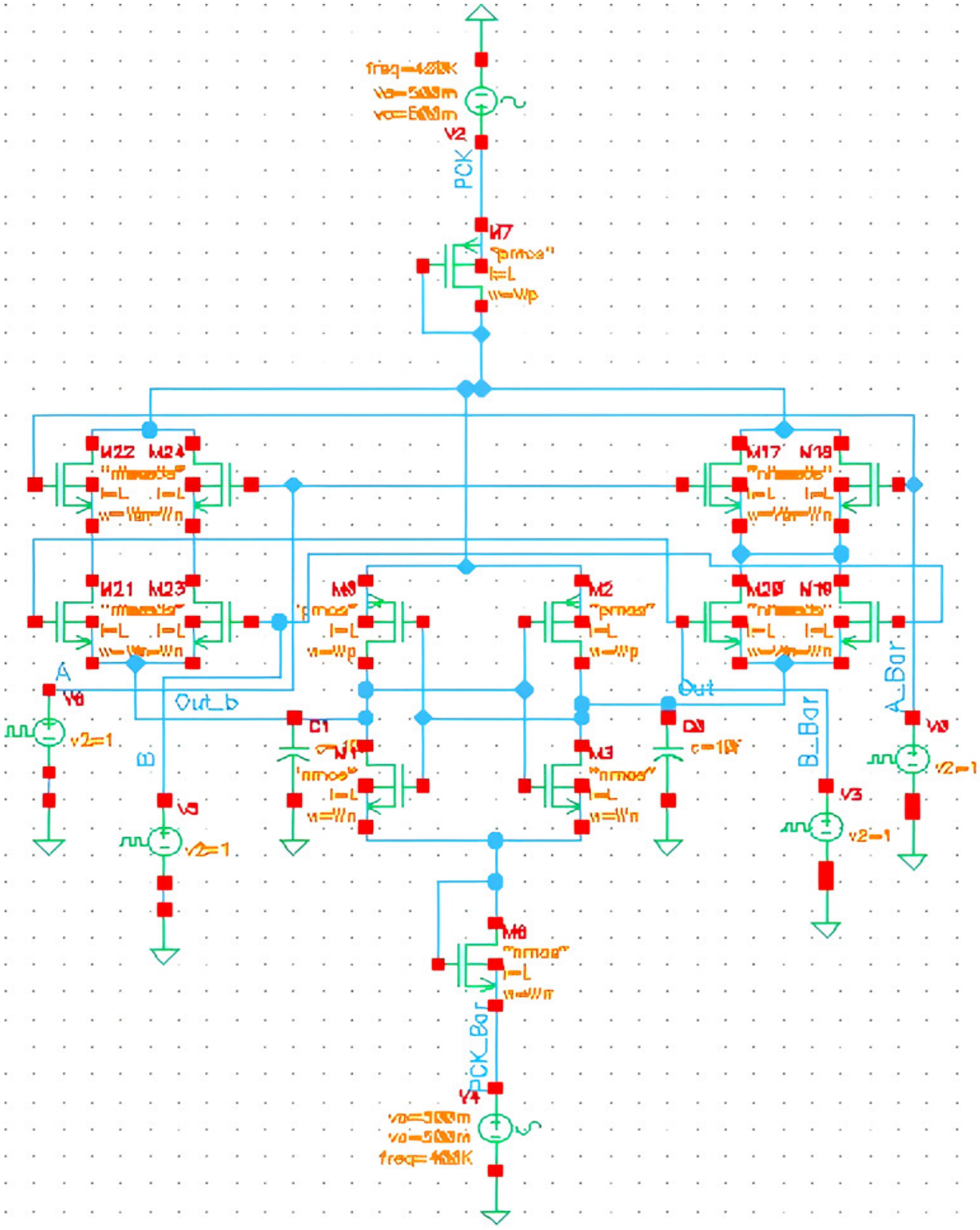

Fig.6.18: Waveform of the EPFAL XNOR/XOR Circuit

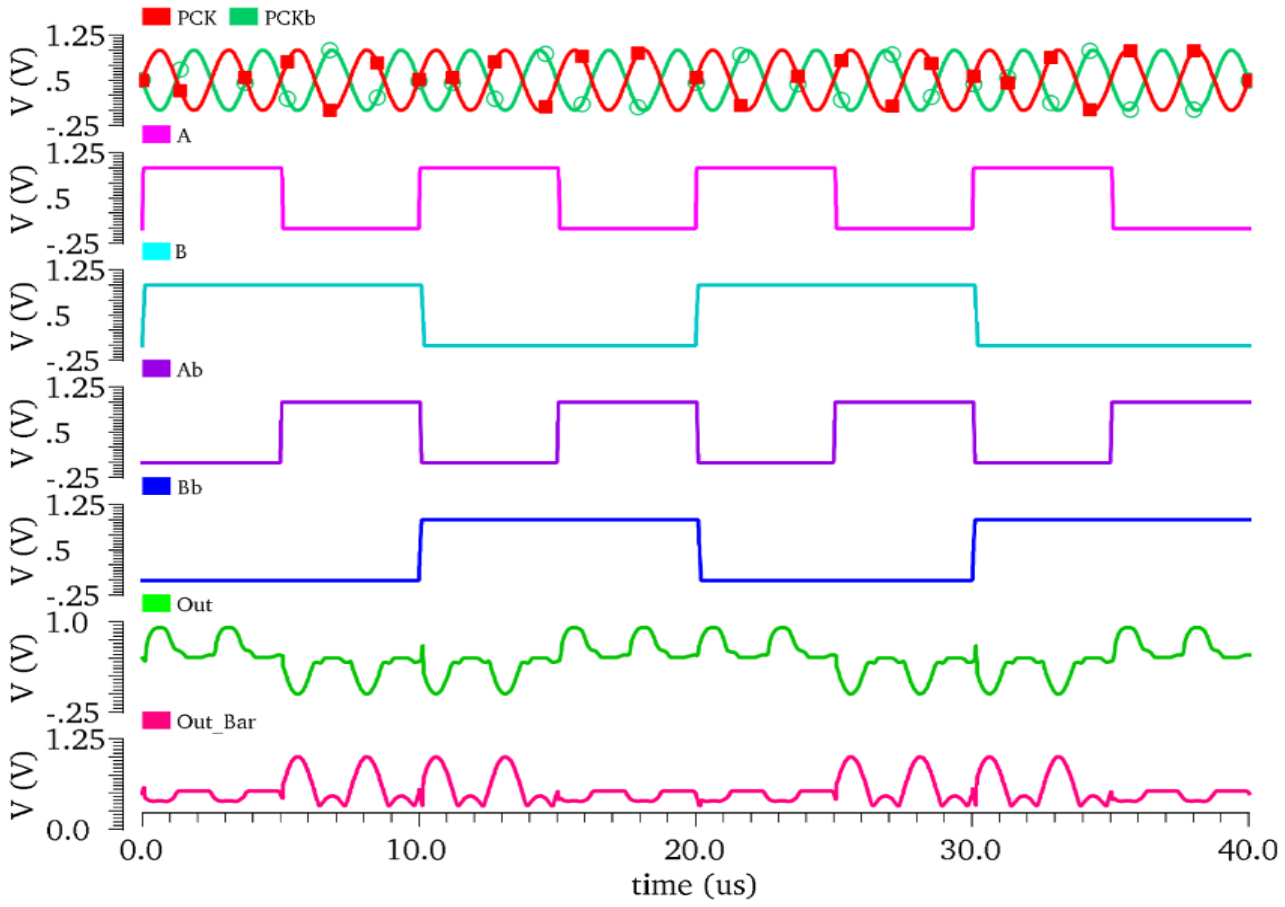

Fig.6.19: EPFAL XNOR/XOR Circuit

6.6. The Parity Circuits

The approach of creating parity is widely utilized as a means of error detection during data transmission. Binary data in digital systems may be subject to noise during transmission and processing. The 0s and 1s in the data bits might be distorted by the background noise. For this reason, it is employed for the purpose of identifying faulty binary data transmission. The transmitting node transmits the data bits together with the parity bit to the receiving node. There was a mistake in the data transfer if the recipient received fewer or more ones than what was provided. The parity bit is produced by a combinational logic circuit called a parity generator, which is used by the transmitter. On the other hand, a circuit known as a parity checker ensures that the receiver has parity. Two parts of a digital system, a parity generator and a parity check, collaborate to detect data transmission errors that are one bit in size. The total of the data bits plus the parity bits could include both even and odd numbers. With odd parity, the whole number of ones becomes an odd number, and with even parity, it becomes an even number, all thanks to the additional parity bit. If you want

your parity circuit to function, you have to follow the rule that states that adding up an odd number of ones is one and adding up an even number of ones is zero. By using XOR gates, which provide zero output for an even number of inputs, inaccurate data may be identified and corrected. The addition of two bits may be accomplished with a single XOR gate, whereas the addition of three bits requires two of these gates (Bhaaskaran, 2011; Kumar & Amphawan, 2016).

6.6.1. The Parity Generator

Parity generators are combinational circuits that receive an n-bit stream of data and produce an additional bit that is sent in conjunction with it, as previously mentioned. This supplementary bit is referred to as a ("parity bit"). A “0” is assigned to the parity bit in an even parity bit technique when the number of 1s in the data stream is even, and a “1” otherwise. In contrast, an odd parity generator utilizes a parity bit of 1 when there are an even number of ones in the data stream, and 0 when there are an odd number of ones (Maji et al., 2020).

6.6.1.1. Even Parity Generator

When sending data, consider using an odd parity bit and three bits of data. It takes three inputs, namely, A, B, and C, and uses P as the parity bit for the output.

Table 6.1: Truth Table of Three Bit Even Parity Generator

3-Bit Message			Even Parity Bit Generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

If the given truth table has rows with an odd number of 1s, then the parity bit gets increased by 1 to make the total number of bits even. Truth tables for three-bit even-parity generating circuits are shown in Table 6.1.

The simplified equation for the parity bit, derived from the preceding truth table, is as follows:

$$P = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$
$$= \overline{A}(\overline{B}C + B\overline{C}) + A(\overline{B}\overline{C} + BC)$$
$$= \overline{A}(B \oplus C) + A(\overline{B \oplus C})$$
$$= A \oplus B \oplus C \qquad (6.20)$$

The above Boolean formula may be implemented using two Exclusive-OR gates (Fig. 6.20), in order to generate an output with even parity. This circuit produces a three-bit message with corresponding parity, which is subsequently sent to an acceptance end where a parity checker circuit endorses the presence or absence of mistakes. To calculate the even parity bit for a 4-bit value, three exclusive-OR gates are prerequisite (Abdalla & Sharroush, 2019).

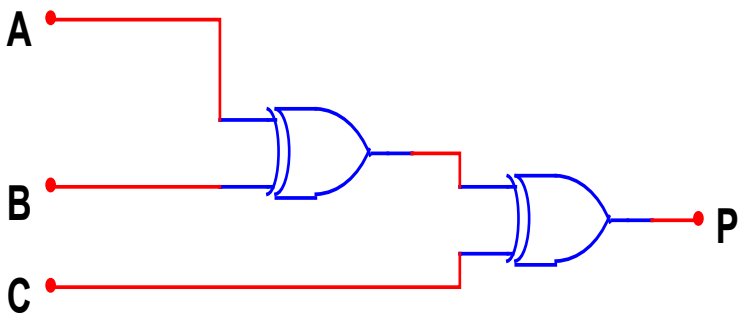

Fig.6.20: Logic of Even Parity Generator

Figure 6.21 is a schematic illustration of the even parity generating circuit, built using the EPFAL approach. The evaluation and recovery phases are integral components of the split-level sinusoidal power supply used to energize the circuit. The simulation waveform of the Even Parity Generator circuit is shown in Fig. 6.22 for a simulation duration of 80µm.

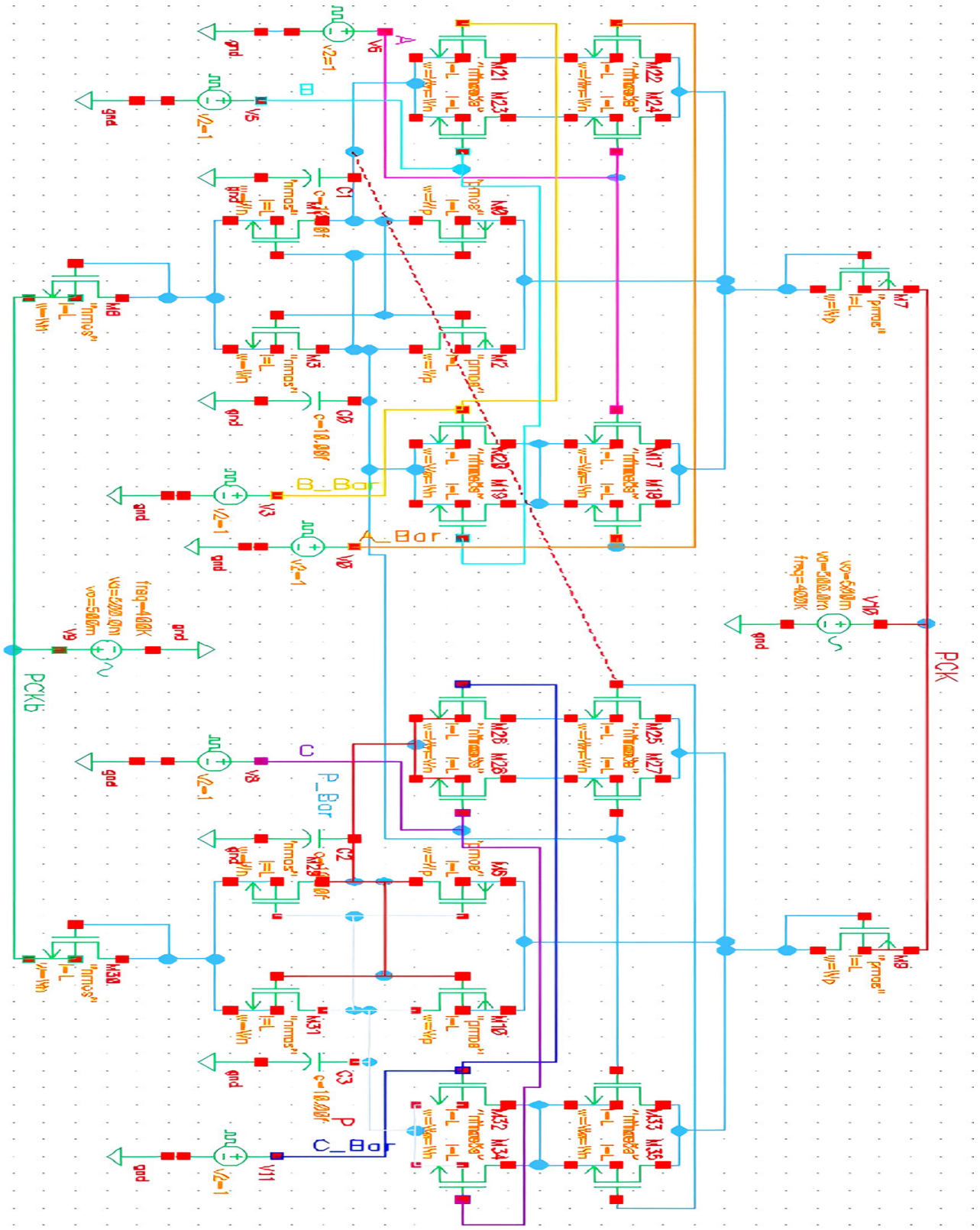

Fig.6.21: EPFAL Even Parity Generator Circuit

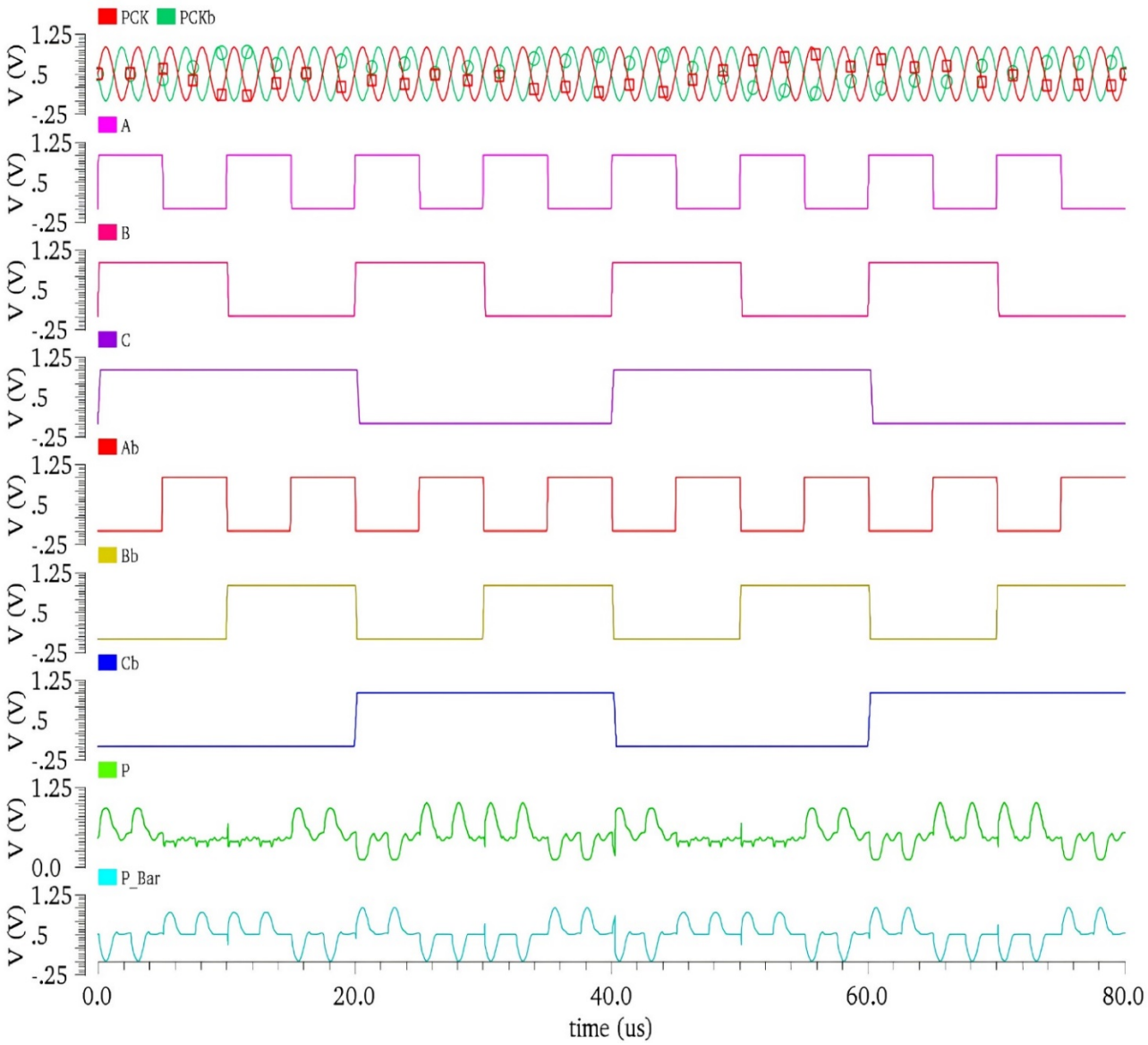

Fig.6.22: Waveform of an EPFAL Even Parity Generator Circuit

6.6.1.2. Odd Parity Generator

Take into consideration the transfer of 3-bit data accompanied by an odd parity bit. With three inputs (A, B, and C) and one parity bit (P) for output, an event has occurred. One requirement for the creation of odd parity bit is that the total number of bits be odd. The truth table of a three-bit odd-parity generating circuit is shown in Table 6.2 (Abdalla & Sharroush, 2019; Norouzi & Heikalabad, 2019)

Table 6.2: Truth Table of Three Bit Odd Parity Generator

3-Bit Message			Odd Parity Bit Generator (P)
A	**B**	**C**	**Y**
0	**0**	**0**	1
0	**0**	**1**	0
0	**1**	**0**	0
0	**1**	**1**	1
1	**0**	**0**	0
1	**0**	**1**	1
1	**1**	**0**	1
1	**1**	**1**	0

Truth table results Odd-parity generator Boolean equation

$$P = \overline{ABC} + \overline{A}BC + A\overline{B}C + AB\overline{C}$$

$$= \overline{A}(B \odot C) + A\overline{(B \odot C)} \quad (6.22)$$

$Let (B \odot C) = X$

$Therefore,$

$P = \overline{A}X + A\overline{X}$

$= A \oplus X$

Substitute the value of X, then:

$$P = A \oplus (B \odot C) \quad (6.23)$$

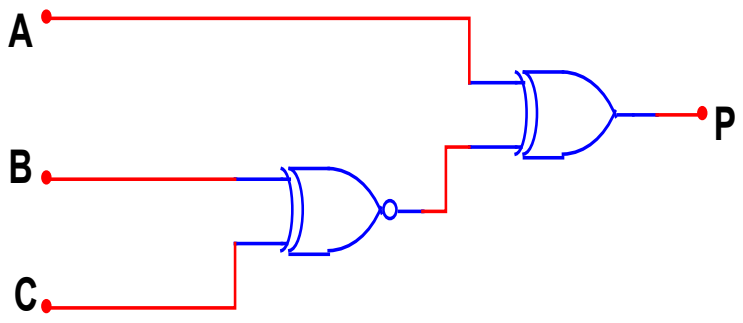

Fig.6.23: Logic diagram of Odd Parity Generator

As shown in Fig. 6.23, the odd parity generator circuit may be built utilizing a single XOR gate and a single XNOR gate. Figure 6.24 shows the circuits for the EPFAL odd parity generator, whereas Fig. 6.25 shows the waveforms that match them.

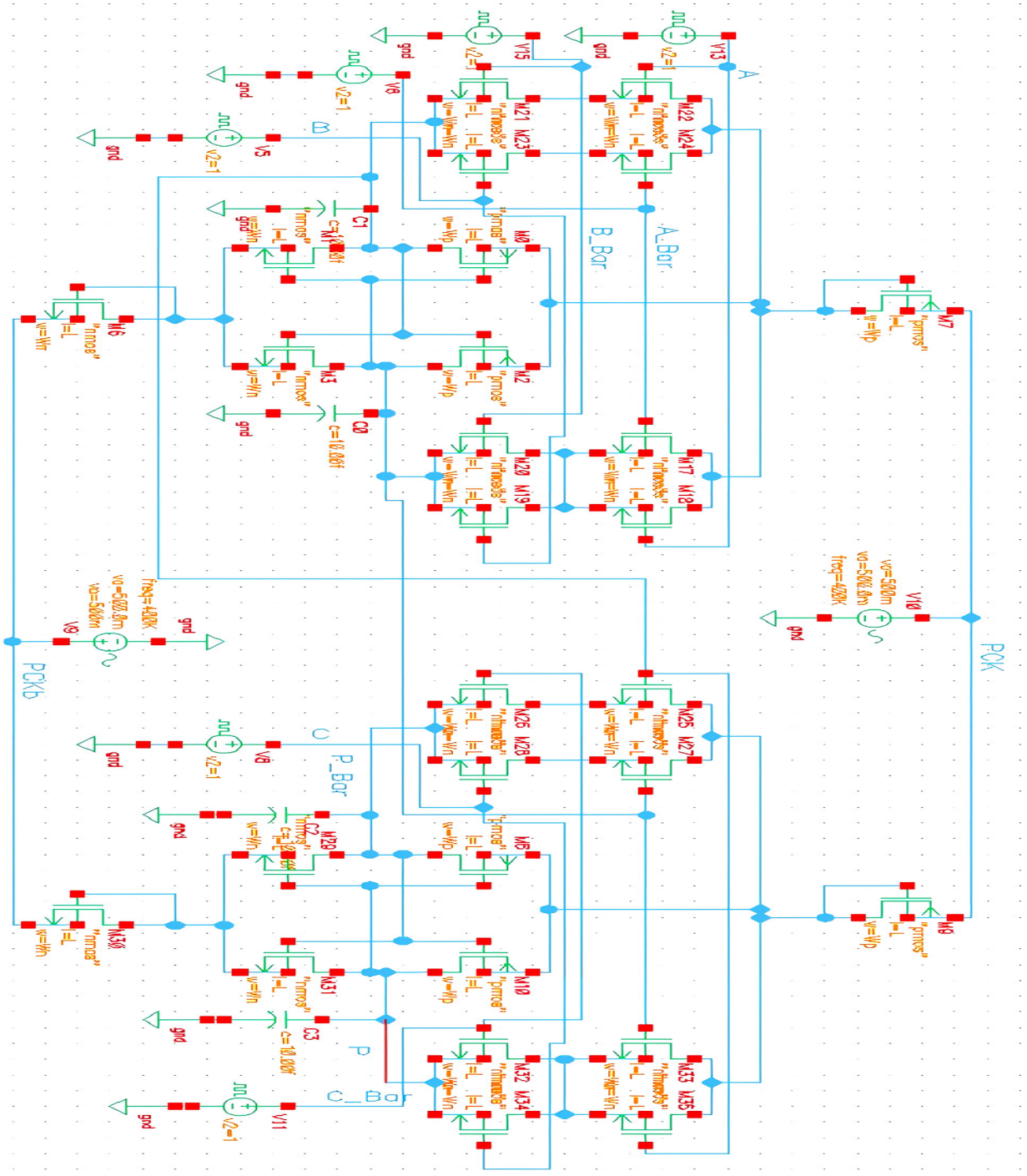

Fig.6.24: EPFAL Odd Parity Generator Circuit

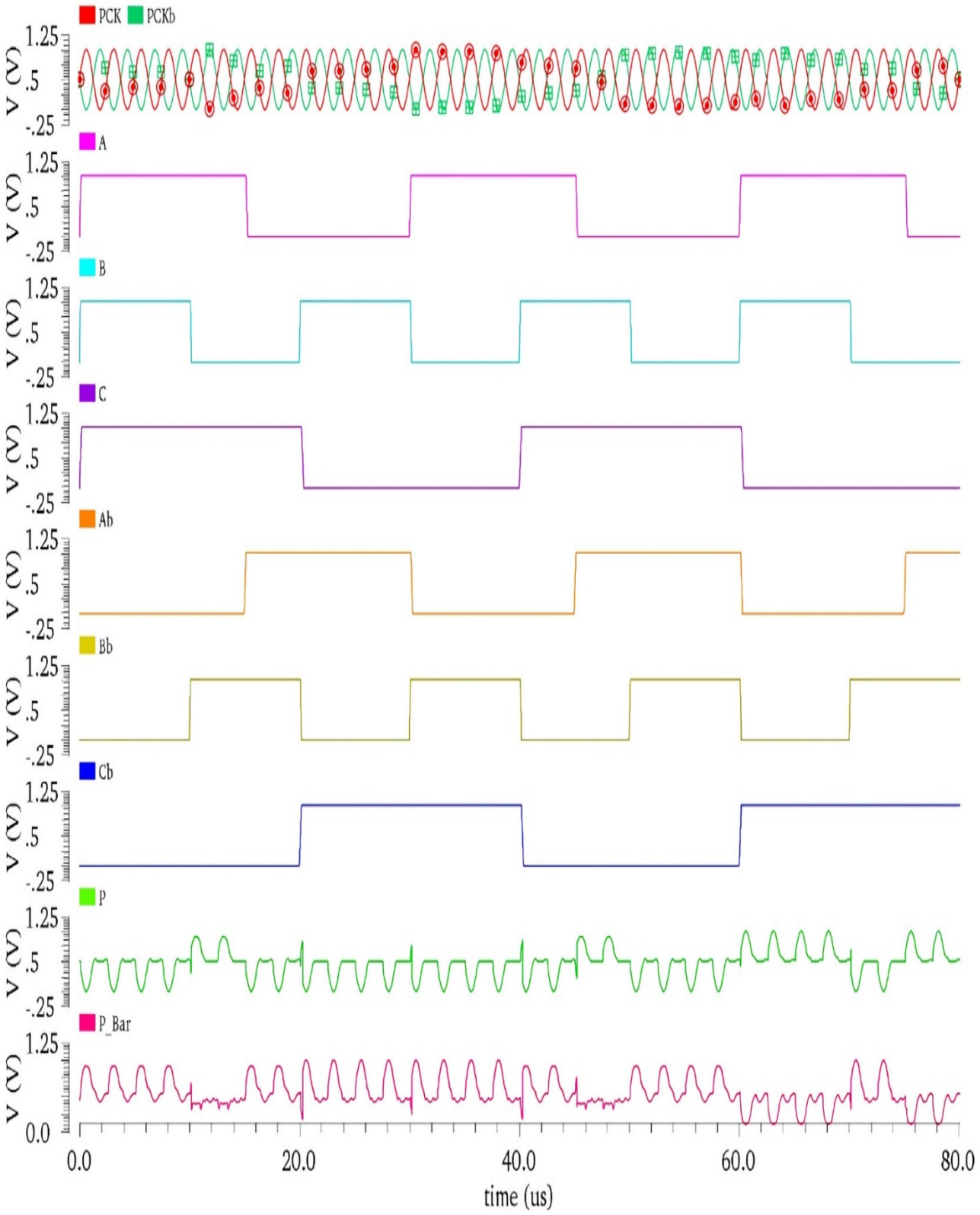

Fig.6.25: Waveform of an EPFAL Odd Parity Generator Circuit

6.6.2. The Parity Checker

A logical circuit is used to ensure that the transmission does not fail. Based on the parity created at the receiving end, this circuit may function as either an even or an odd parity watcher. Keeping the number of input bits equal is crucial for this circuit to work as an even parity checker. After a parity mistake has occurred, the "sum even" result will be low while the "sum odd" output will be large. With an odd number of input bits, this logic circuit can check for odd parity; nevertheless, when an error occurs, the "sum odd" output will be low and the "sum even" output will be high (Kumar & Amphawan, 2016).

6.6.2.1. Even Parity Checker

Assuming that the end of the sending also generates an even parity bit and three input messages, to guarantee that data is error-free, parity checker circuit accepts these four bits.

Table 6.3: Truth Table of Four Bit Received Even Parity Checker

4-Bit Message Received				Even Parity Bit Error Checker (CP)
A	**B**	**C**	**P**	**Y**
0	**0**	**0**	**0**	0
0	**0**	**0**	**1**	1
0	**0**	**1**	**0**	1
0	**0**	**1**	**1**	0
0	**1**	**0**	**0**	1
0	**1**	**0**	**1**	0
0	**1**	**1**	**0**	0
0	**1**	**1**	**1**	1
1	**0**	**0**	**0**	1
1	**0**	**0**	**1**	0
1	**0**	**1**	**0**	0
1	**0**	**1**	**1**	1
1	**1**	**0**	**0**	0
1	**1**	**0**	**1**	1
1	**1**	**1**	**0**	1
1	**1**	**1**	**1**	0

When a mistake happens, the message that is received has an unusual number of ones. Table 6.3 displays the truth table for the even parity checker; an error occurs when CP = 1, meaning that the four bits received include an odd number of 1s, and CP = 0 otherwise (Maji et al., 2020; Abdalla & Sharroush, 2019).

The logical expression is derived from the above truth table as:

$$CP = \overline{AB}\left(\overline{C}P + C\overline{P}\right) + \overline{A}B\left(\overline{CP} + CP\right) + AB\left(\overline{C}P + C\overline{P}\right) + A\overline{B}\left(\overline{CP} + CP\right)$$
$$= (A \oplus B) \oplus (C \oplus P) \qquad (6.21)$$

Fig. 6.26 illustrates that the logic statement for the even parity checker that follows it can be formulated by employing three XOR gates.

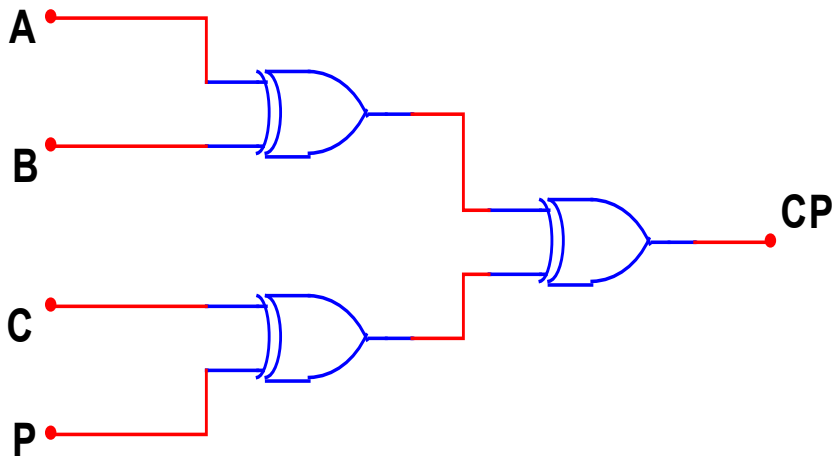

Fig.6.26: Logic diagram of Even Parity Checker

Even parity verification requires the utilization of an additional Ex-OR gate when the received message is five bits in length. Figure 6.27 exhibits the schematic framework for EPFAL-based even parity checker circuits, while Fig. 6.28 displays the simulation waveforms of EPFAL even parity checker circuits (Norouzi & Heikalabad, 2019).

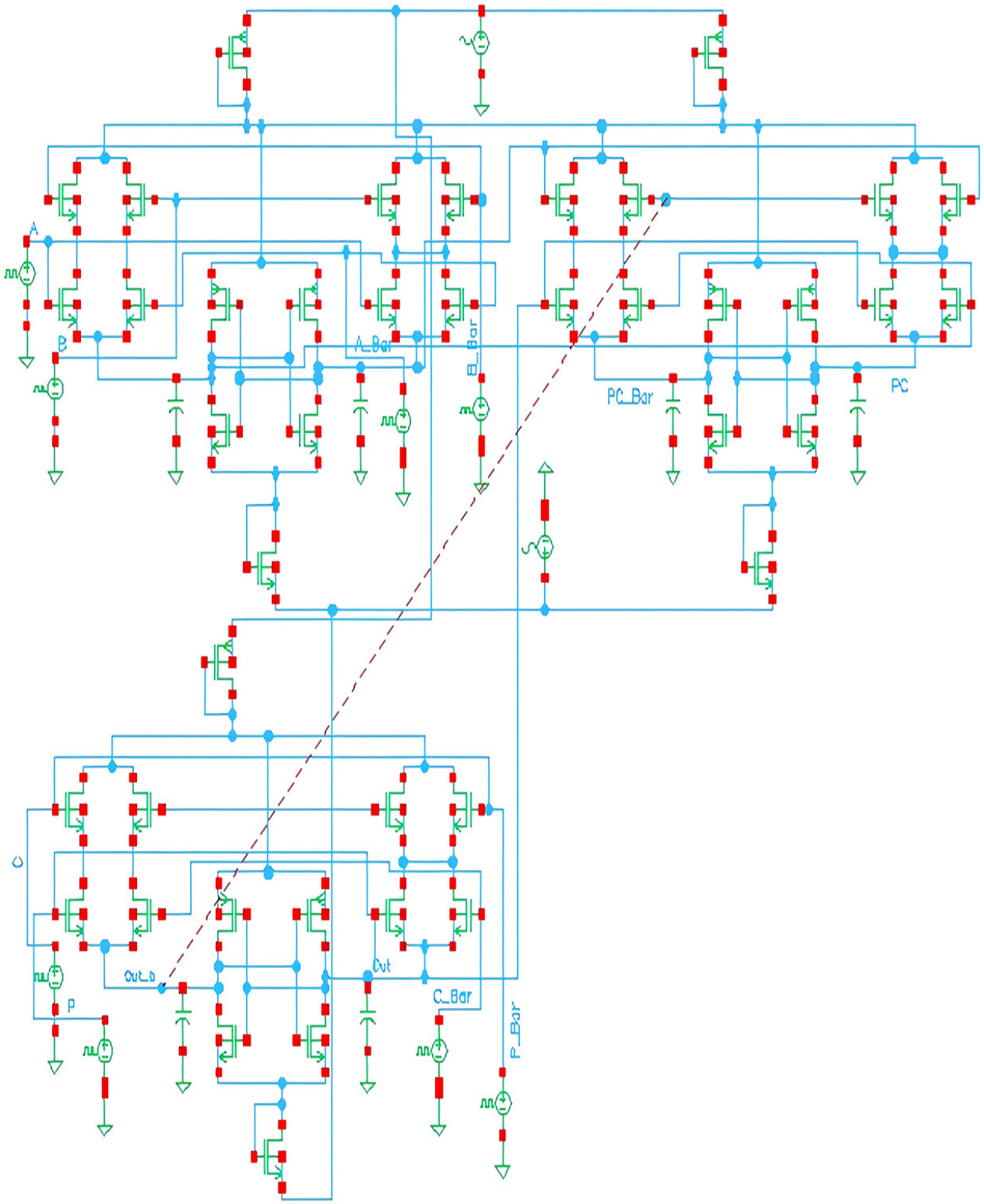

Fig.6.27: EPFAL Even Parity Checker Circuit

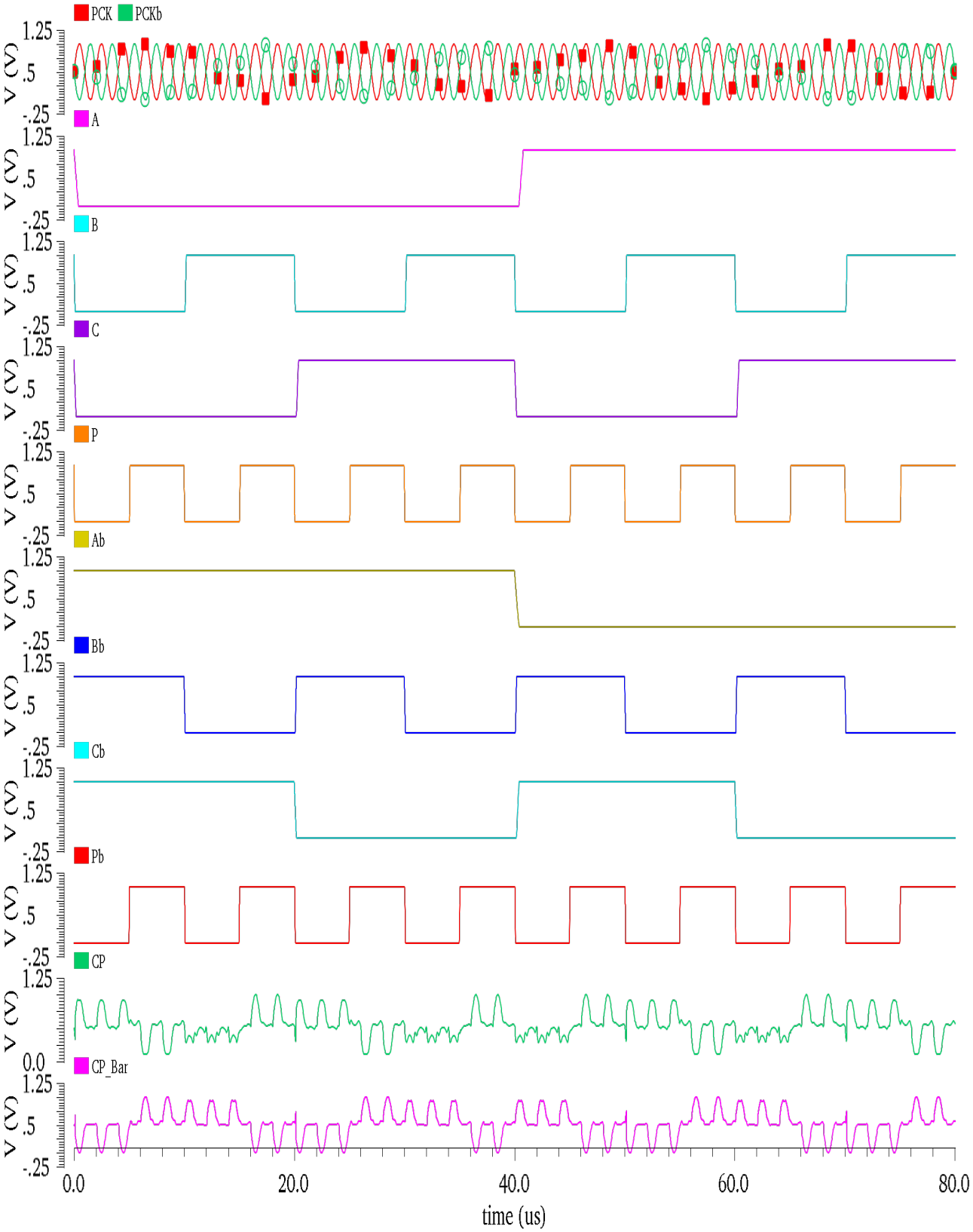

Fig.6.28: Waveform of EPFAL Even Parity Checker Circuit

6.6.2.2. Odd Parity Checker

Take into consideration the transmitting end of a three-bit message that contains an odd parity bit. After receiving these four bits, the data is checked for errors by the odd-parity checker circuit.

Table 6.4: Truth Table of Four Bit Received Odd Parity Checker

4-Bit Message Received				Odd Parity Bit Error Checker (CP)
A	**B**	**C**	**P**	**Y**
0	**0**	**0**	**0**	1
0	**0**	**0**	**1**	0
0	**0**	**1**	**0**	0
0	**0**	**1**	**1**	1
0	**1**	**0**	**0**	0
0	**1**	**0**	**1**	1
0	**1**	**1**	**0**	1
0	**1**	**1**	**1**	0
1	**0**	**0**	**0**	0
1	**0**	**0**	**1**	1
1	**0**	**1**	**0**	1
1	**0**	**1**	**1**	0
1	**1**	**0**	**0**	1
1	**1**	**0**	**1**	0
1	**1**	**1**	**0**	0
1	**1**	**1**	**1**	1

No mistake is indicated by the total number of ones in the data since the data is sent with odd parity at the sending end. To be sure, the error stands out when there are exactly even numbers of ones in the data. Below, in Table 6.4, you can see the truth table of the odd parity generator. According to many studies (Abdalla & Sharroush, 2019; Norouzi & Heikalabad, 2019; Lakshmi et al., 2020), CP = 1 when the received 4-bit message has an even number of 1s, indicating an error, and CP = 0 when the message consists of an odd number of 1s, signifying no mistakes.

After simplification, the final equation for the PEC is derived as,

$$PC = \left(AB + \overline{AB}\right) \odot \left(CP + \overline{CP}\right)$$
$$PC = (A \odot B) \odot (C \odot P) \tag{6.24}$$

Three XNOR gates can be used to create the equation for the odd parity checker, as illustrated in Fig. 6.29. In Figs. 6.30 and 6.31, the EPFAL odd parity checker circuits and associated waveforms are presented.

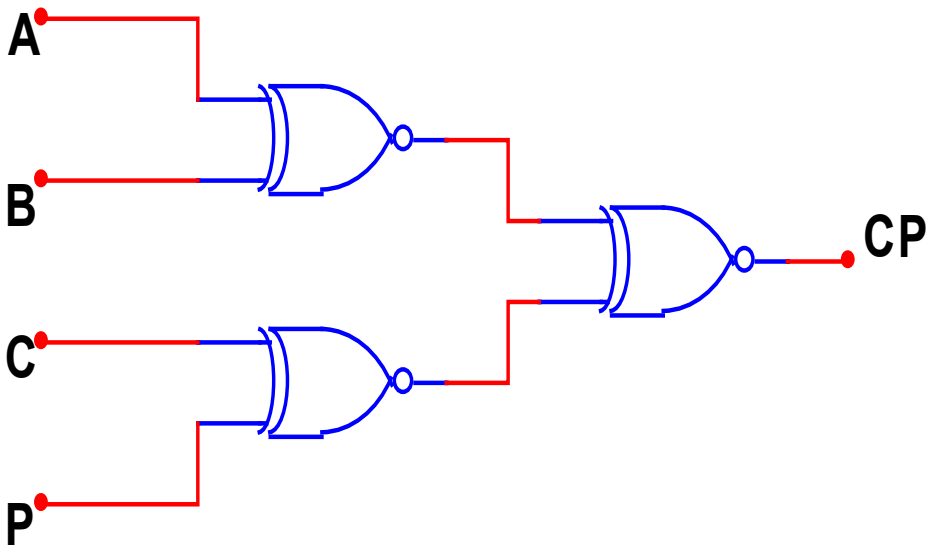

Fig.6.29: Logic diagram of Odd Parity Checker

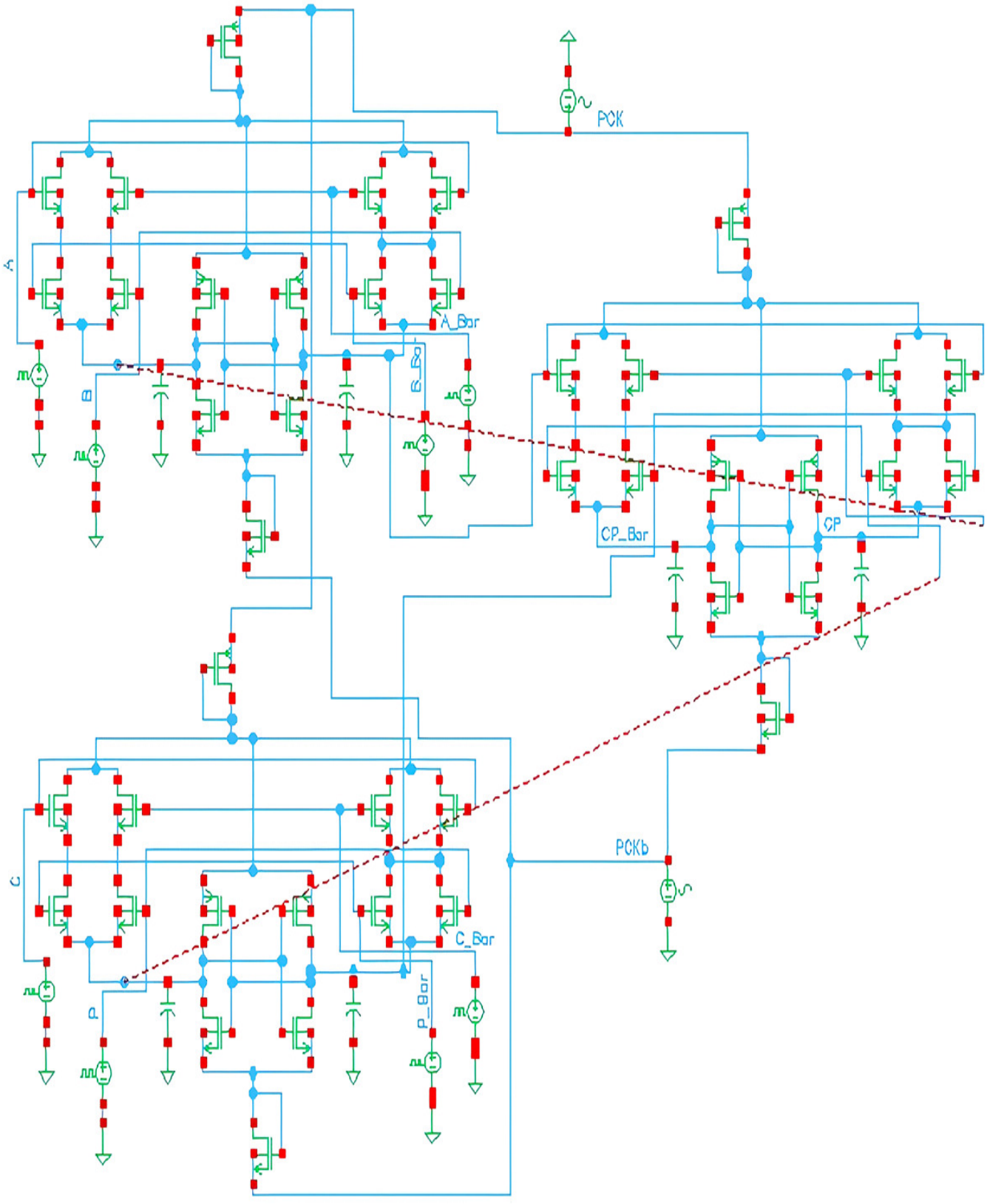

Fig.6.30: EPFAL Odd Parity Checker Circuit

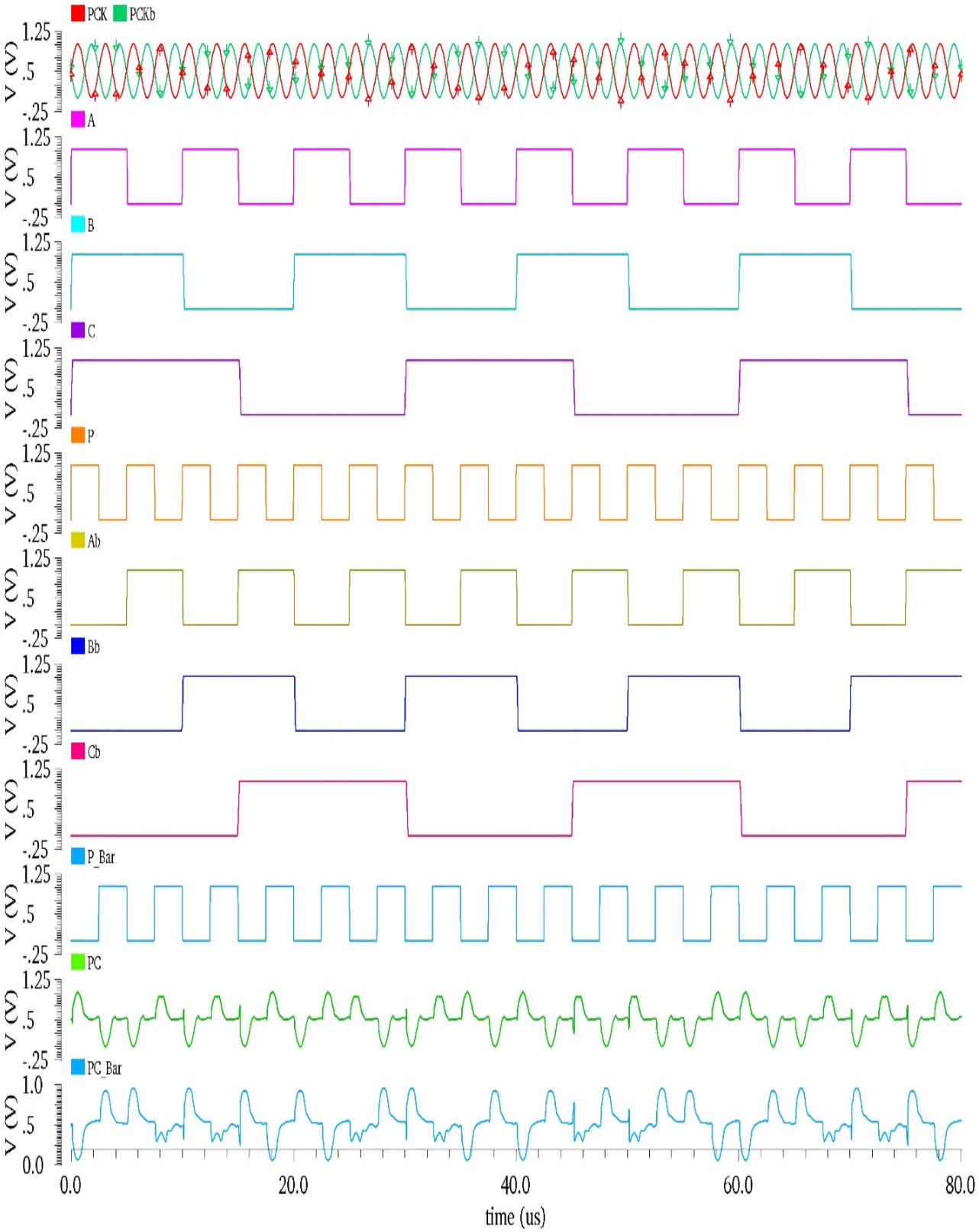

Fig.6.31: Waveform of an EPFAL Odd Parity Checker Circuit

6.7. Results and Discussion

The dynamic power consumption average at different frequencies of the proposed EPFAL circuit is compared to that of conventional CMOS and well-known reference adiabatic circuits such as ECRL, PFAL, 2N-2N2P, 2P-PFAL, IPGAL, CDCAL, DCPAL, and A-DCVSL. Comparative analyses are conducted at using the LP-PTM (Maji et al., 2020). The average power consumption of each circuit is computed using Cadence Virtuoso, an analog design environment (Fig. 6.11). The $45nm$ technology's design parameters employed are $L = 45nm$, $W_n = 400nm$, and $W_P = 600nm$, while the load capacitor is set at $10fF$ as specified in (Abdalla & Sharroush, 2019). The input voltage amplitudes and power supply values are: $V_{in} = V_{DD} = 1V$, and $V_\phi = \overline{V}_\phi = 0.5V$. The suggested EPFAL inverter circuit, CMOS, and a well-known reference adiabatic family are each shown together with their average power consumption at $50kHz$, $100kHz$, $200kHz$, $400kHz$, and $800kHz$, respectively, as shown in Table 6.5. With regard to Inverter/Buffer, NAND/AND, NOR/OR, and XNOR/XOR logic functions that were designed in a cross-couple, dual rail structure, simulations were carried out at 100 kHz operating frequency. Table 6.6 shows the average power consumption of typical CMOS, proposed EPFAL circuits, and all reference dual rail output circuits. Tables 6.5 and 6.6 validate that the suggested circuit, EPFAL, has superior presentation in power optimization.

Table 6.5: Comparison of 45nm_LP_PTM Inverter Circuits' Power Consumptions (nW) at Several Operational Frequencies Within Five Cycles of their Respective Inputs.

Logics/Freq.	50 kHz	100 kHz	200 kHz	400 kHz	800 kHz
ECRL	1.236	1.501	3.211	5.540	9.210
PFAL	1.175	1.432	3.015	5.470	8.071
2N-2N2P	0.994	1.302	2.671	4.830	7.791
2P-PFAL	0.976	1.289	2.421	4.721	7.173
IPGAL	1.094	1.362	2.358	4.619	6.319
DCPAL	1.121	1.492	3.394	5.928	8.192
CDCAL	1.022	1.231	2.750	3.859	5.911
A-DCVSL	0.832	1.112	2.294	3.271	5.053
EPFAL	0.571	0.939	1.391	2.887	4.978

Figure 6.32 depicts the typical average dynamic power consumption of even parity generators and checker circuits that were designed using conventional CMOS technology and a variety of adiabatic literature. These circuits were constructed with the help of the aforementioned technologies. Similarly, Fig. 6.33 illustrates the average dynamic power consumption of odd parity generators and checker circuits built using standard CMOS technology and several well-established adiabatic families. These circuits were built using a variety of adiabatic families. For the entirety of the procedure, evaluations were carried out utilizing a 45 nm LP_PTM node at an operating frequency of 100 kHz. Figures 6.32 and 6.33 exhibit the power-optimization efficacy of the proposed EPFAL circuit when associated to other design approaches.

Table 6.6: 45nm_LP_PTM; Comparison of Average Dynamic Power Consumption (nW) for Basic Gates Designed Using Conventional CMOS and Various Adiabatic Logic Techniques. Within Five Cycles (five periods) of Simulation time at 100 kHz Operating Frequency

Adiabatic Families/ Logics Design	Inverter/Buffer	NAND/AND	NOR/OR	XNOR/XOR
ECRL	1.501	2.098	2.182	3.456
PFAL	1.432	1.995	1.987	3.347
A-DCVSL	1.112	1.457	1.776	2.349
CDCAL	1.231	1.571	1.874	2.761
EPFAL	0.939	0.960	1.109	1.982
2N-2N2P	1.302	1.684	1.898	3.221
2P-PFAL	1.289	1.598	1.887	3.093
IPGAL	1.362	1.795	1.877	3.274
DEPAL	1.492	2.079	2.108	3.449

Table 6.7: 45nm_LP_PTM: Average Dynamic Power Consumption (in Nano Watts) for Basic Gates Designed Using Conventional CMOS Within 100µm Simulation Time at 100 kHz Operating Frequency

Logics Design	Inverter	AND	NAND	OR	NOR	XOR	XNOR
CMOS	2.00	3.587	2.447	3.33	2.691	7.671	8.234

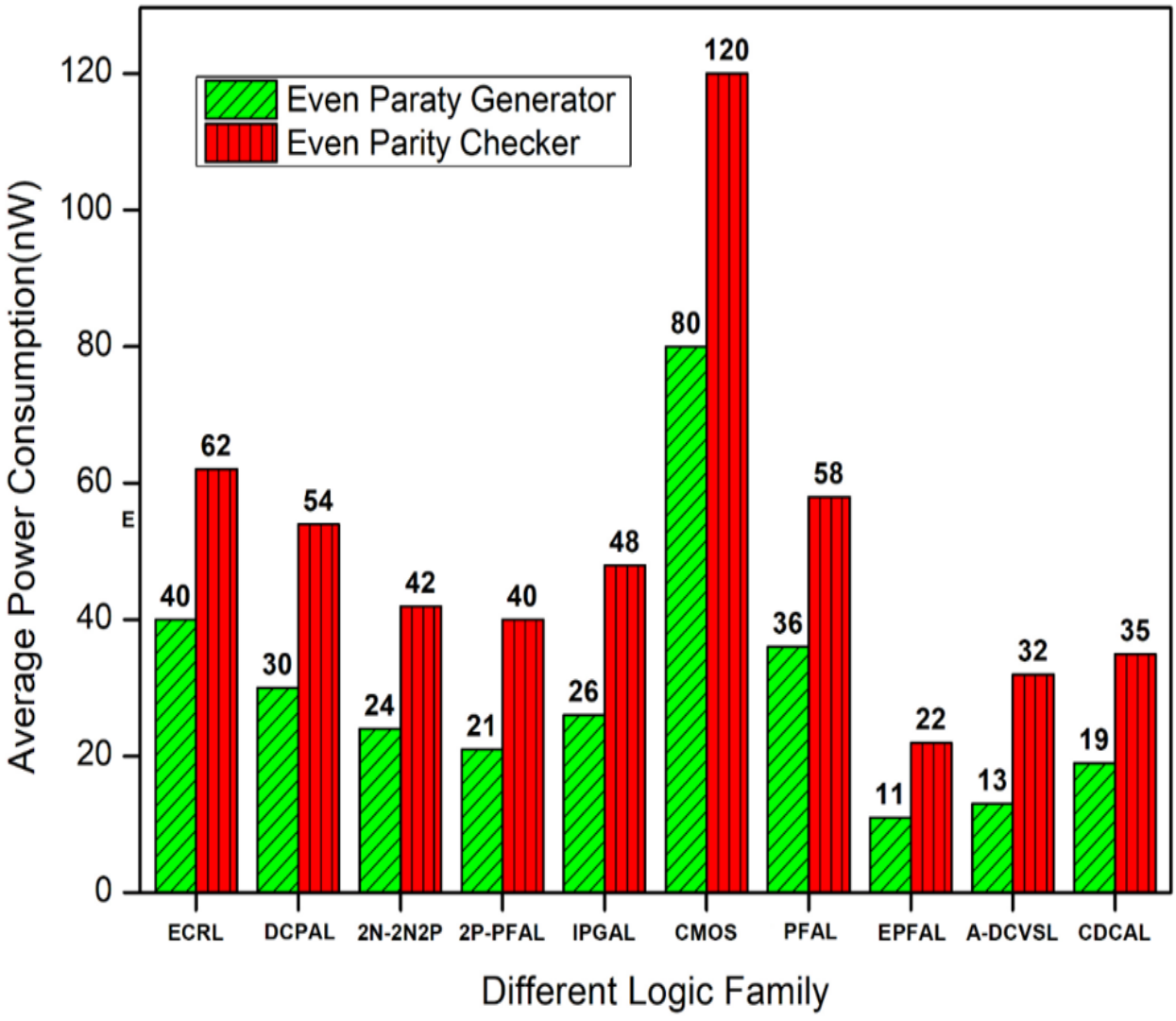

Fig.6.32: Average dynamic power consumption of Even Parity Generator and Checker Circuits designed using traditional CMOS approach and several adiabatic literatures

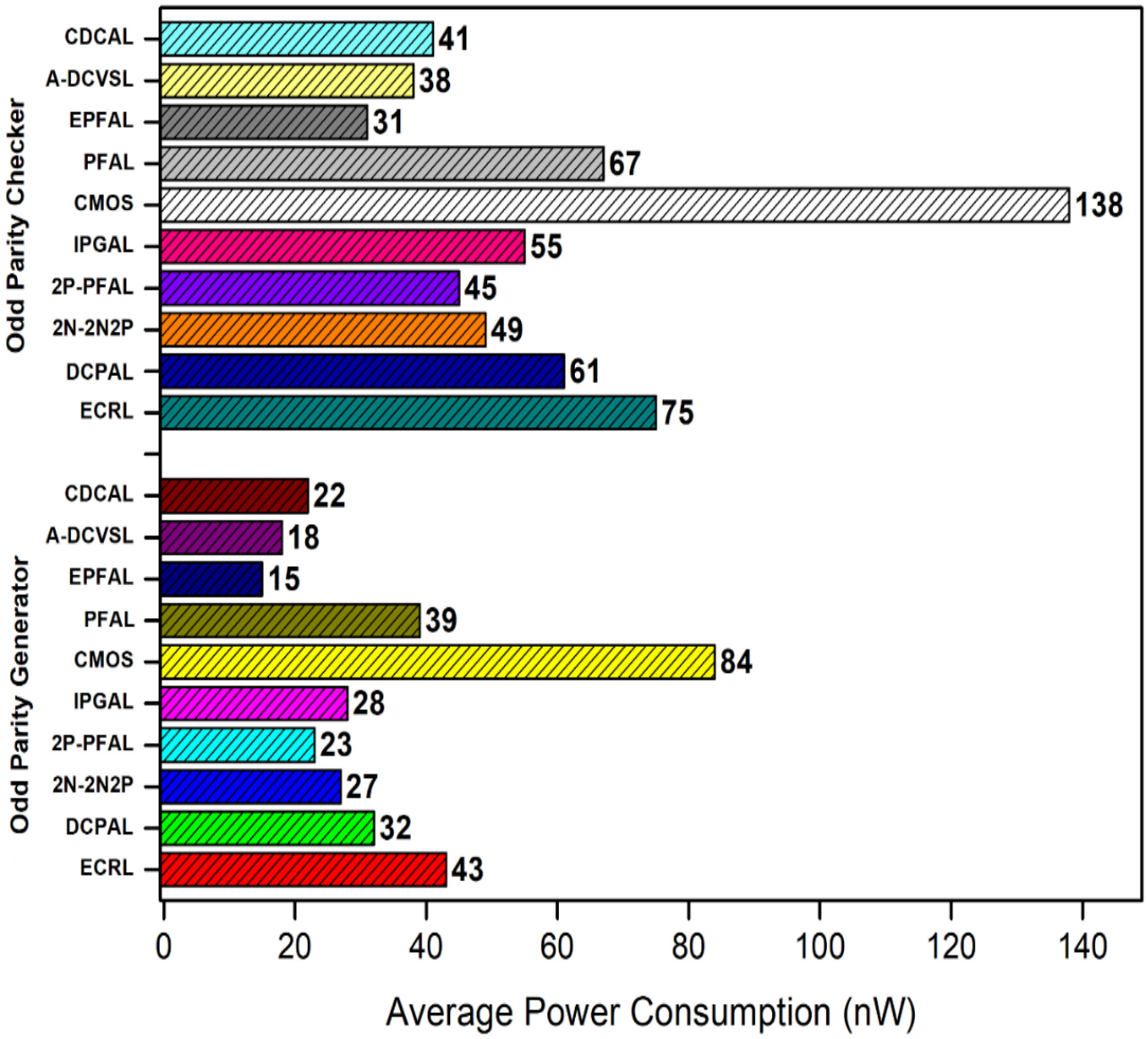

Fig.6.33: Average dynamic power consumption of Odd Parity Generator and Checker Circuits designed using traditional CMOS approach and several adiabatic families

6.8. Summary

In this chapter, we designed and analyzed two-phase sinusoidal power-clock-driven dual-rail encoded and sense amplifier-structured quasi-adiabatic circuits, and we offer a novel EPFAL system. In addition to the advantages of conventional PFAL, EPFAL offers ideal dynamic power consumption due to the use of a sinusoidal power supply with a split-level configuration. In addition, since there is no direct channel for leakage current from the power source to ground, the leakage power loss would be significantly reduced compared to those with a direct connection to ground. To

confirm the practicability of circuit, thorough analyses were performed at many operating frequencies using the $45nm$, LP_PTM file. It demonstrates that the EPFAL inverter saves 53.05%, 27.88%, 27.15%, 31.05%, 37.06%, 37.44%, 34.42%, 15.55%, and 23.72% of average power compared to the CMOS, 2N-2N2P, 2P-PFAL, IPGAL, DCPAL, ECRL, PFAL, A-DCVSL, and CDCAL circuits, respectively. When compared to traditional CMOS design methodologies, the suggested circuit EPFAL decreases dynamic energy usage in checker circuits by 81.66% and in even parity generators by 86.25%. Observation and analysis outcomes, as well as comparative performance assessment, demonstrate its superiority to CMOS. IDFAL offers superior power efficacy and optimization compared to CMOS and other adiabatic logic families. The suggested logic would thus be advantageous for upcoming low-power VLSI circuit applications.

CHAPTER-7

Power Efficient Fully Adiabatic Logic Circuit Design Approach: Application to Inverter and 8421 Code to Excess- 3 Code Converter

7.1. Introduction

The primary objective of VLSI designers is to improve power efficiency. A new power-efficient standard or fully adiabatic BCD 8421 code to XS-3 code converter is introduced in this chapter. The suggested design is contrasted with the conventional CMOS and two well-known families of fully adiabatic logic, namely ADCL and 2PASCL, both of which demonstrate ordinary power savings in the current body of adiabatic research. With a fixed channel length and width of 0.3µm and 0.75µm, respectively, the circuit employs 0.3µm CMOS technology, and the frequency range covered by the work is 100 MHz to 900 MHz. The results demonstrate that the suggested logic saves 54.54% power compared to CMOS logic, 28.57% power compared to ADCL, and 16.67% power compared to 2PASCL at 500 mm. Extensive assessments were conducted at low-frequency kHz ranges and high-frequency MHz ranges employing superior performance, smaller technology nodes, and larger numbers of the newest adiabatic logic design approaches to confirm the usefulness of the proposed circuit. The evaluations were conducted with the use of the most recent adiabatic design methodologies, including QSERL, 2PADCL, CCAL, 2PADL, DFAL, A-DCVSL, using the Barkley HP_PTM at 45 nm and 16 nm. Using Cadence Virtuoso, we looked at each fundamental gate's average power usage, circuit delays, and PDP.

In today's era, the widespread use of electronic gadgets such as mobile phones, laptops, pagers, and kindles, and the need to increase the devices' speed to achieve greater performance, compelled designers to seek an energy-efficient approach in the VLSI circuit design process. Therefore, decreasing power consumption in battery-powered equipment is a crucial objective of low-power VLSI circuit design. For a typical CMOS network, the power lost as a consequence of charging and discharging at the node of the output capacitor is estimated as $\alpha C_L V_{DD}^2 f$ (Bharti & Rakshit, 2018; Kumar & Bharathi, 2013; Takahashi & Mizunuma, 2000; Anuar *et al.,* 2010; Ye & Roy, 2001; Takahashi et al., 2006; Li *et al.,* 2013; Sasipriya & Bhaaskaran, 2008). Several techniques, including lowering the applied voltage (V_{DD}), decreasing the charging frequency (f), reducing switching

activity (α), and decreasing load capacitance (C_L), have been used to minimize power loss in standard CMOS circuits. It has significant drawbacks, such as the scaling down of the transistor threshold voltage (V_T), but it also causes a sharp rise in sub-threshold leakage current. Overall power consumptions in typical CMOS circuits are connected to dynamic $\left(P_{dyn}\right)$, short-circuit (P_{sc}), and leakage power (P_{leak}) (Kumar & Bharathi, 2013).

$$P_{tot} = P_{dyn} + P_{sc} + P_{leak} = C_L V_{DD} V f_{CLK} + I_{sc} V_{dd} + I_{leak} V_{dd} \quad (7.1)$$

To compensate for such a significant loss of power, a new technology known as adiabatic logic has been developed, which is quite feasible for minimizing the power squandered by digital CMOS circuits. Adiabatic is one of the thermodynamics' activities. The heat exchange with the environment is virtually zero, and hence the energy lost has been truncated (Takahashi & Mizunuma, 2000). The adiabatic logic process involves reclaiming the energy ($0.5C_L V^2$) that was held by a load capacitor throughout the first power clock cycle during the negative power clock cycle. Consequently, energy is reused and losses are minimized (Anuar et al., 2010; Takahashi & Mizunuma, 2000). See Fig. 7.1 for an illustration of the four steps that make up the adiabatic logic switching principle: wait (W), evaluation (E), hold (H), and recovery (R). It is recommended to use a power clock that is either sinusoidal or trapezoidal. While in the W phase, the circuit does nothing but wait for the cycle to begin again.

The duration of the hold phase determines how long the outputs are held constant at a high level of logic. Anuar et al. (2010) state that the last step, recovery, involves restoring and returning the energies accumulated at the nodes of the output to the source power clock. The study specifically investigated two well-known standard-adiabatic logic techniques, namely ADCL (Takahashi & Mizunuma, 2000) and 2PASCL (Anuar et al., 2010), using 0.3µm CMOS technologies. This choice was made because the proposed circuit shares a similar feedback structure with the 2PASCL and operates with a single power supply, similar to the ADCL. Furthermore, thorough evaluations were conducted to showcase the benefits of the proposed circuit using various predictive models (PTM).

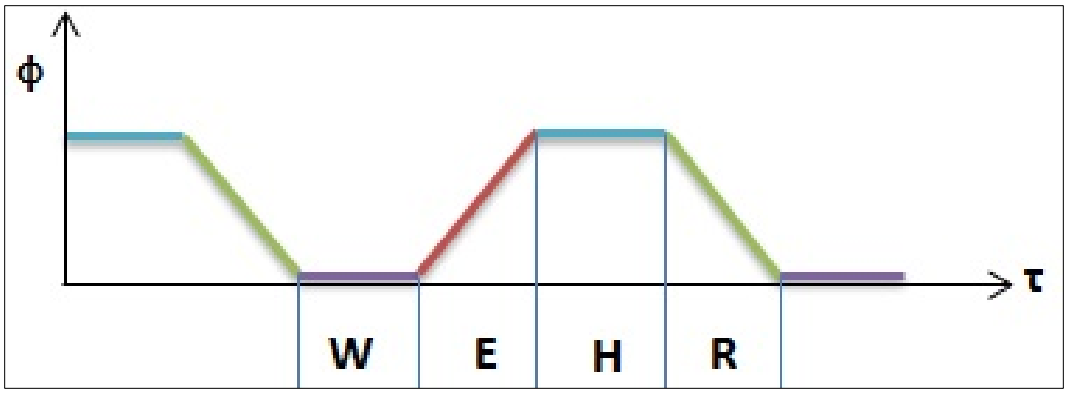

Fig.7.1: Phases of power supply in adiabatic technique

The results were then compared to those of trendy adiabatic literature, including QSERL (Ye & Roy, 2001), 2PADCL (Takahashi et al., 2006), CCAL (Li et al., 2013), 2PADL (Sasipriya & Bhaaskaran, 2018), DFAL (Upadhyay, 2013; Kumar & Kumar, 2022; Kumar & Kumar, 2020), and A-DSCVL (Gupta et al., 2022). The diagrams illustrating the basic inverter circuits may be found in Figs. 7.2–7.9.

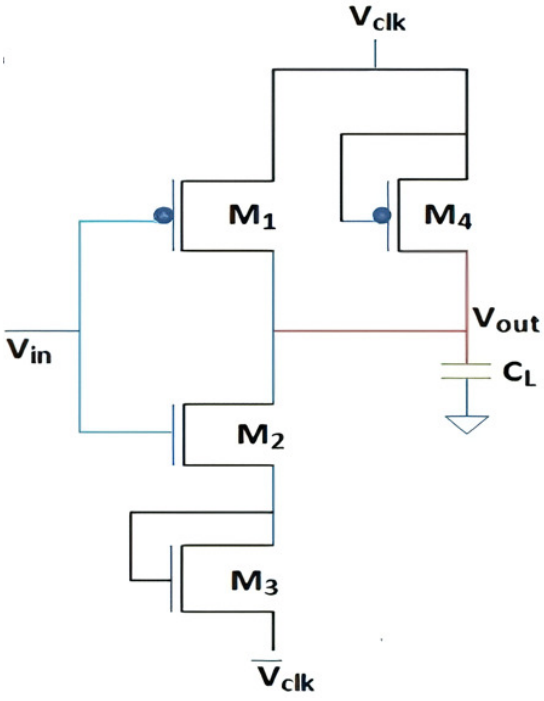

Fig.7.2: 2PASCL Basic Inverter

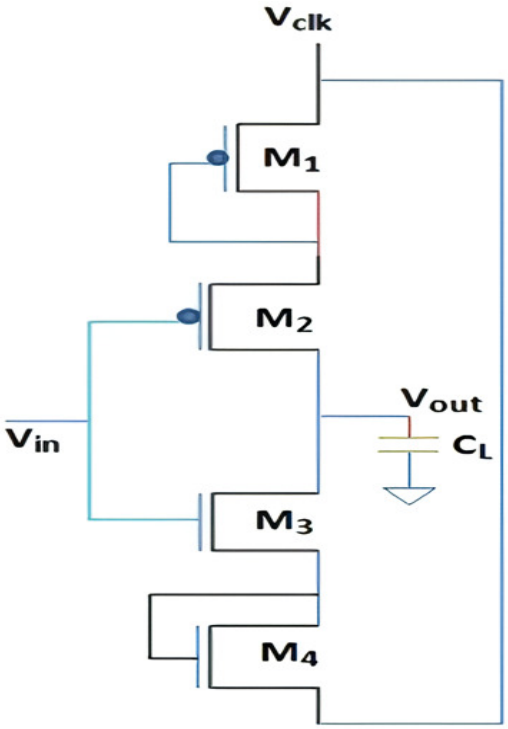

Fig.7.3: ADCL Basic Inverter

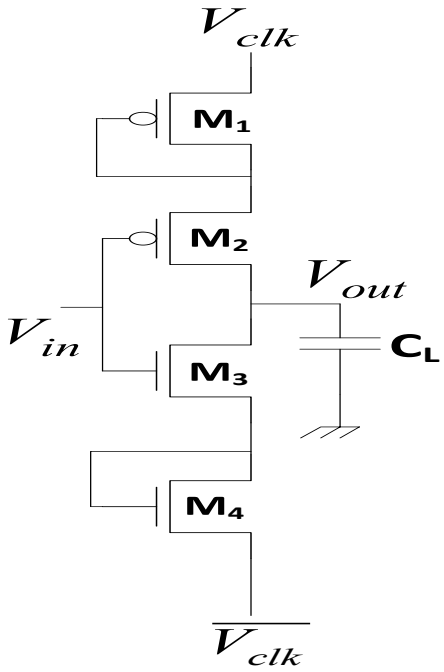

Fig.7.4: QSERL Basic Inverter

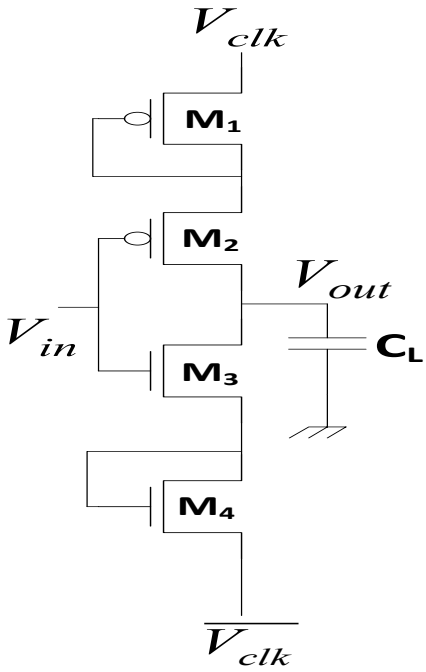

Fig.7.5: 2PADCL Basic Inverter

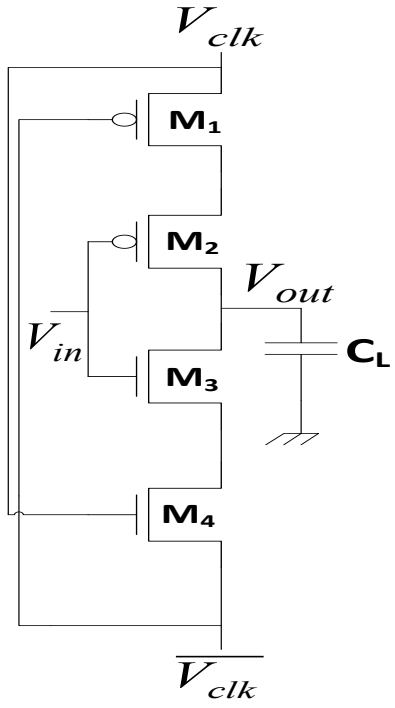

Fig.7.6: CCAL Basic Inverter

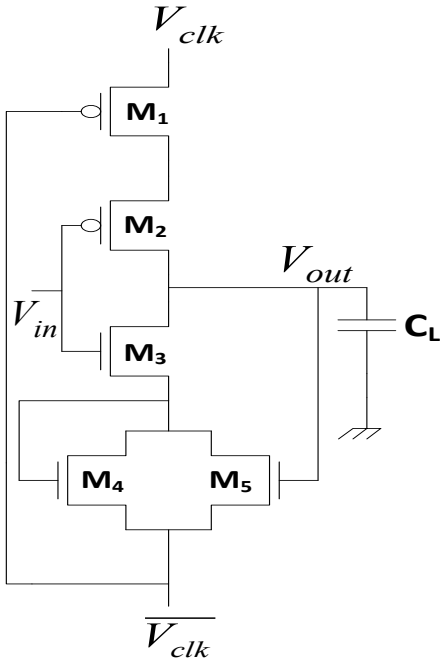

Fig.7.7: 2PADL Basic Inverter

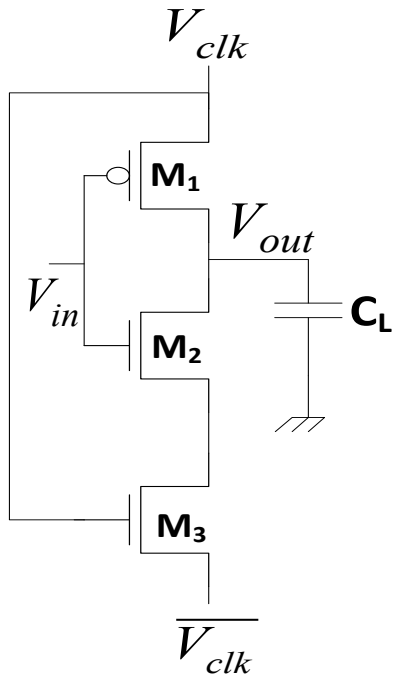

Fig.7.8: DFAL Basic Inverter

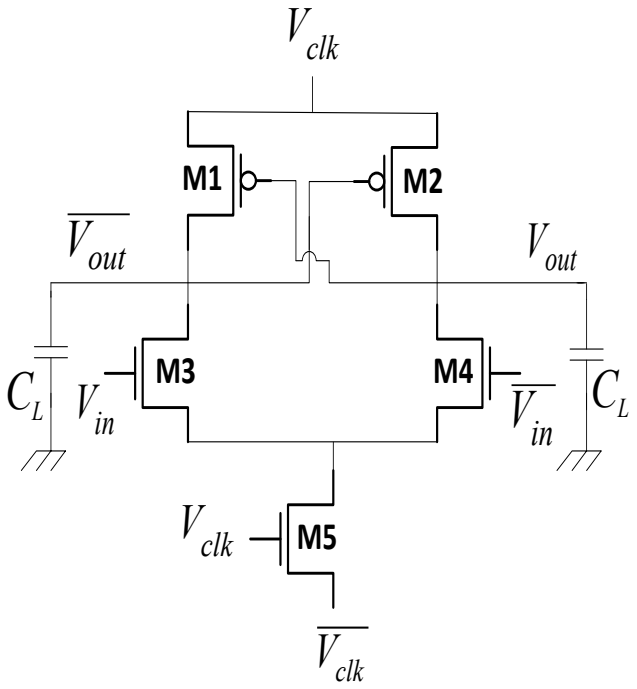

Fig.7.9: A-DSCVL Basic Inverter

The reference models, such as 2PASCL and ADCL, were thoroughly analyzed and compared with the proposed model in respect of power consumption and total gate area, or active area per chip. The work proves that the proposed model has less power dissipation and better performance. Previous work on adiabatic BCD to Excess-3 code converters included ECRL, PFAL, quantum dot cellular automata (QCA), and adiabatic logic array (ALA) (Moon & Jeong, 1996; Morrison et al., 2014; Kumar et al., 2017; AntoBennet et al., 2017).

7.2. Proposed Inverter Logic

In the proposed standard or fully adiabatic logic style, we have appended two more extra PMOS transistors in such a way that both of them are connected above and below the output node, as illustrated in Fig. 7.10. The circuit employs a single power clock. The addition and logical utilization of these two extra transistors in PMOS yield power minimization. The proposed circuit has a 3P-1N logic configuration. The circuit seems to be in a partial or quasi-adiabatic logic style, since ground is connected to MP2. However, as the energy is not lost during logic transitions and is theoretically fully recovered back to the power supply, the design has followed the standard or fully-adiabatic logic technique (D'heer et al., 2018; Morrison & Ranganathan, 2014; Avital et al., 2015). The

working of the circuit is almost similar to that of 2PASCL, as both circuits use one additional PMOS, configured as a diode across the power supply PCK and load capacitor. According to the proposed technique shown in Fig. 7.10, the PMOS transistor MP1 acts as an inverted diode with respect to the power supply.

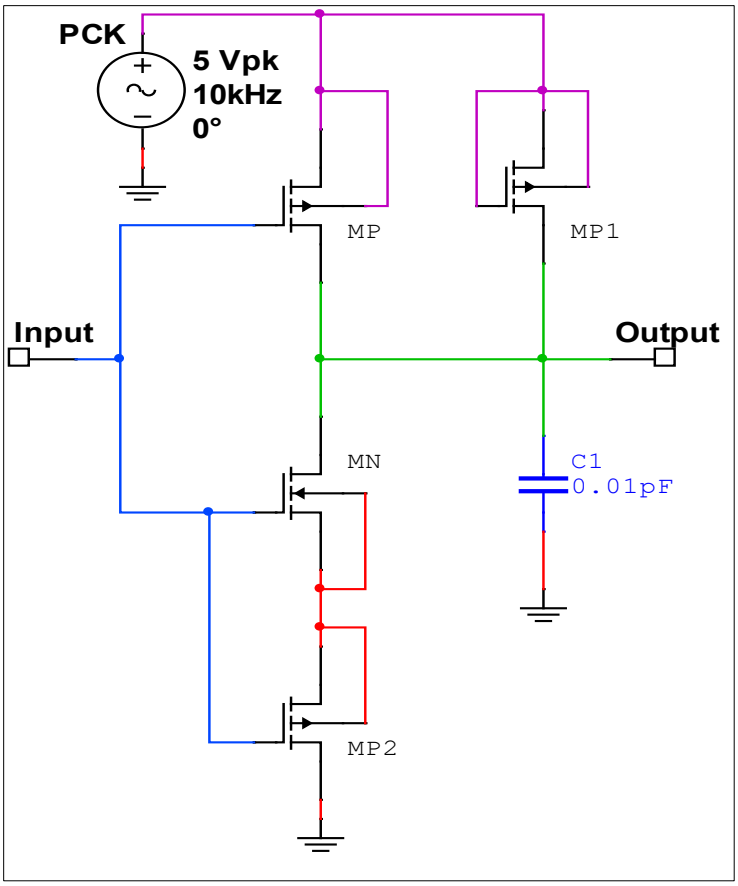

Fig.7.10: Basic Inverter circuit of proposed logic

When the input logic is low, the transistors MP and MP2 are ON, whereas the transistors MP1 and MN are in OFF states. The load capacitor is charged up to logic 1. When the input logic is high, the transistors MP and MP2 are OFF, whereas the transistor MN is ON. As transistor MP2 is open, the output capacitor voltage is not discharged to the ground through the NMOS transistor MN, since MN and MP2 are in series. The energy is therefore, in fact, recycled after being used by the circuit by sending it back to the supply PCK via the PMOS transistor MP1, as now it acts as a forward-biased diode. Hence, the power losses are minimized (Tenace et al., 2016; Yan & Chen, 2010; Maksimovic

et al., 2000). In Fig. 7.11, the basic proposed inverter simulation waveform is given. The transient analysis is carried out at a PCK value of 10 kHz and a voltage of 5Vp-p, respectively.

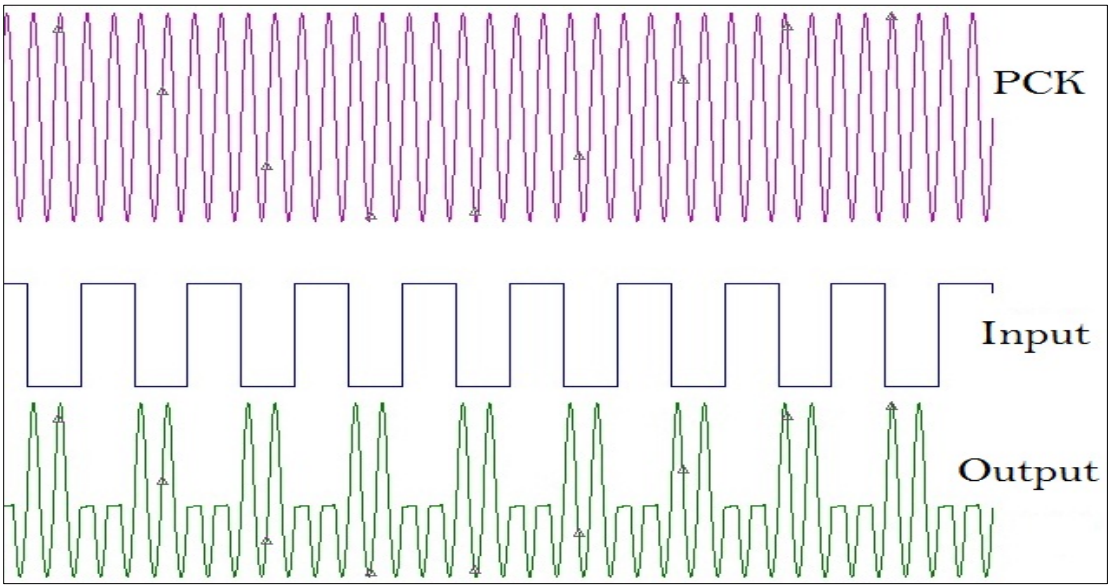

Fig.7.11: Basic Proposed Inverter Waveform

The dynamic energy consumption of the circuit can be estimated from Figs. 7.12 and 7.13. Figure 7.12 depicts the schematic of the proposed basic inverter circuit. According to Dickinson and Danker (1995) and Teichmann (2012), Fig. 7.13 shows the RC equivalent of the proposed circuit during charging the output load capacitor C_L, and Fig. 7.14 shows the RC equivalent of the circuit when discharging the output node, load capacitor C_L. When input V_{in} swings from logic one to zero, PMOS transistor M_1 conducts, and the associated ON-resistance of the transistor is indicated by R_{ON}. On the other hand, when the input V_{in} swings from zero to one, the reverse occurs, and the transistor M_1 is in cut-off and is represented by R_{Open}. As demonstrated in Figs. 7.12 and 7.13, the PMOS transistor M_2 functions as an inverted diode D_1 since its source and drain are shorted.

This arrangement makes use of complementary and 180degrees out of phase sinusoidal power supply $V\phi$ and $\overline{V\phi}$. The energy loss resulting from the threshold voltage is estimated as (Ye & Roy, 1996).

$$E_p = \frac{1}{2} C_L \left|V_{tp}\right|^2 \tag{7.2}$$

Considering all initial conditions of the circuit are zero. Let the amount of charge ejected from the source $V\phi$ be Q, therefore (Takahashi & Mizunuma, 2000; Dickinson & Danker, 1995; Ye & Roy, 1996).

$$Q = C_L V_P \tag{7.3}$$

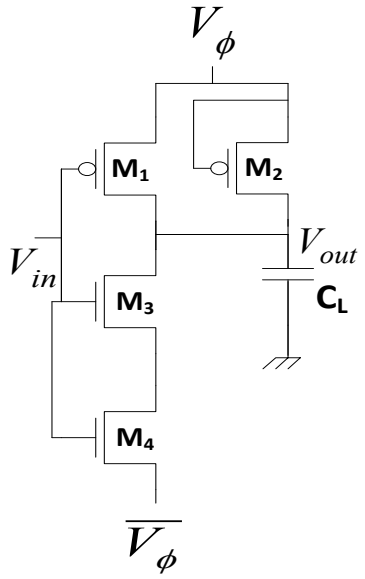

Fig.7.12: schematic of the proposed basic inverter.

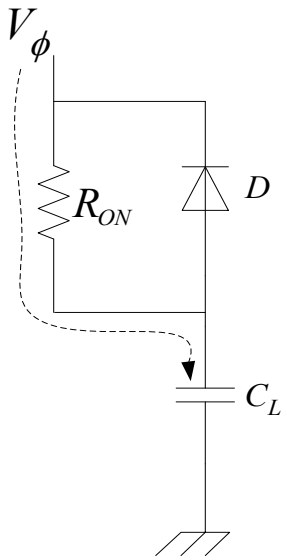

Fig.7.13: RC equivalent of the proposed Inverter.

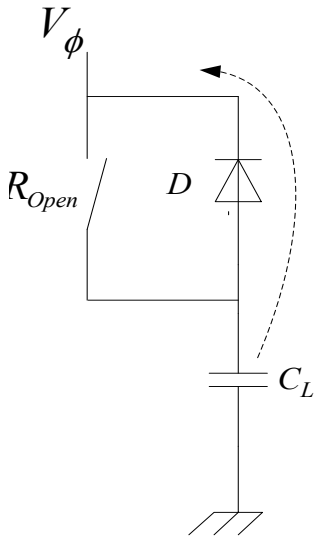

Fig.7.14: RC equivalent of the circuit when discharging.

Where, V_P is the peak voltage of the source $V\phi$, and C_L is the capacitance of the load capacitor.

During charging, the energy dissipated in the ON-resistance R is calculated as (Takahashi & Mizunuma, 2000).

$$E_{Chrg} = I^2 R_{On} T = \left(\frac{Q}{T}\right)^2 R_{On} T \tag{7.4}$$

$$= \left(\frac{C_L V_P}{T}\right)^2 R_{On} T = \frac{{C_L}^2 {V_P}^2}{T^2} R_{On} T = \left(\frac{C_L R_{On}}{T}\right) C_L {V_P}^2 \tag{7.5}$$

At the discharging time, the energy lost due to the threshold voltage of the diode is approximated according to Ye & Roy (2001).

$$E_D = C_L V_d (V_P - V_d) \tag{7.6}$$

During the recovery time, the energy stored in the load capacitor is returned to the power supply through diode D. Therefore,

$$E_{dis-Chrg} = E_D = C_L V_d (V_P - V_d) \tag{7.7}$$

The circuit has only a PMOS threshold voltage energy loss during the charging process, since the NMOS is not in the recovery path, hence the circuit suffered from the energy loss resulting from the threshold voltage of a PMOS transistor M_1 only. It is estimated as (Ye & Roy, 1996).

$$E_p = \frac{1}{2} C_L |V_{tp}|^2 \tag{7.8}$$

The threshold voltage of a PMOS transistor is denoted as V_{tp}. So, the overall energy use is estimated as a result of the following equations: (Bharti & Rakshit, 2018; Takahashi & Mizunuma, 2000; Anuar et al., 2010).

$$E_{Total} = E_{Chrg} + E_{dis-Chrg} + E_p \tag{7.9}$$

$$E_{Total} = \left(\frac{C_L R_{On}}{T}\right) C_L {V_P}^2 + C_L V_d (V_P - V_d) + \frac{1}{2} C_L |V_{tp}|^2 \tag{7.10}$$

7.3. Average Power Consumption Analyses with Predictive Technologies

This section compares the suggested design to the reference adiabatic circuits given in Section 7.1, in terms of average power consumption, circuit delays, PDP, energy consumption, and EDP.

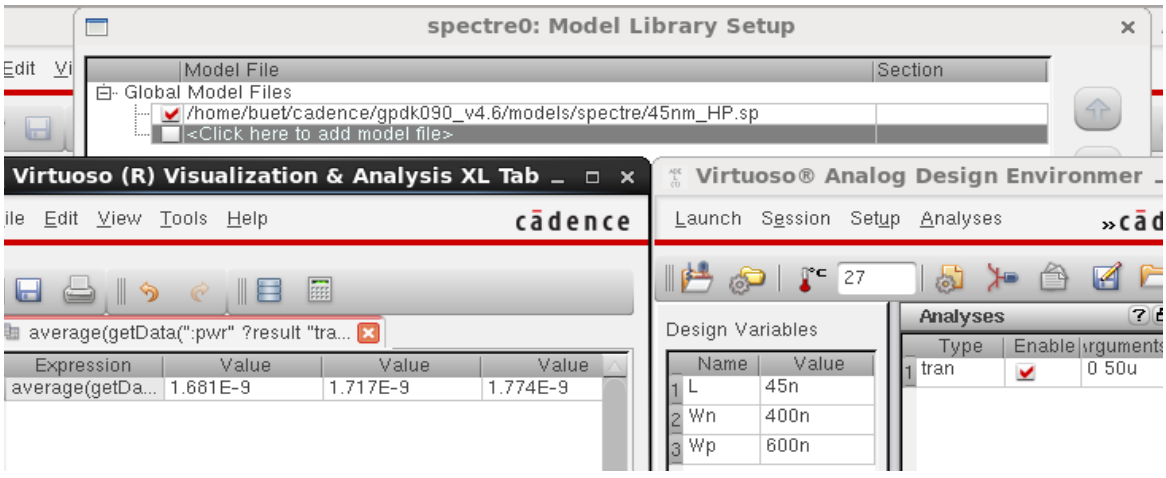

Fig.7.15: Average Power Calculation of Proposed Circuit using 45nm-HP_PTM at Various Frequencies

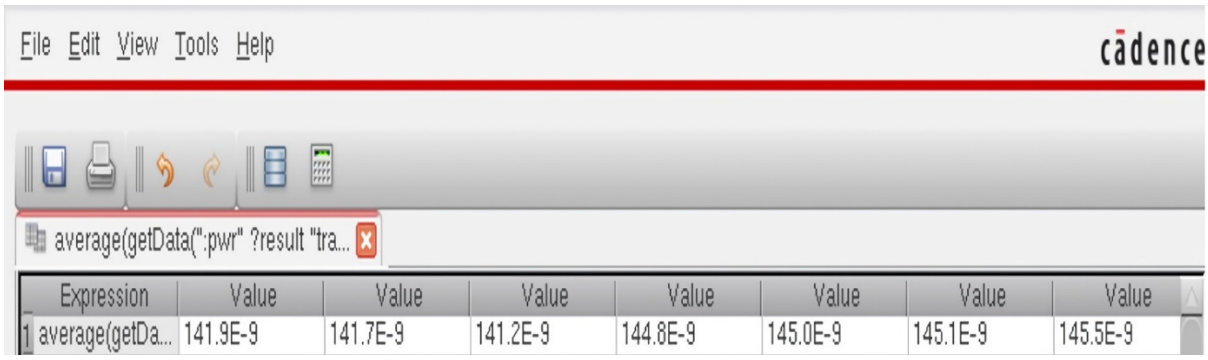

Fig.7.16: Average Power Calculation of CMOS Circuit using 45nm HP_PTM at Various Frequencies

Table 7.1: Comparison of 45nm_HP_PTM Inverter Circuits' Power Consumptions at Several Operating Frequencies Within Five Clock Periods or Cycle Times of Their Respective Input

45nm_HP_PTM: Average Power Consumption in (nW)							
Logics/Freq.	**20 kHz**	**50 kHz**	**100 kHz**	**200 kHz**	**400 kHz**	**500 kHz**	**800 kHz**
CMOS	141.9	141.7	141.2	144.8	145.0	145.1	145.5
ADCL	58.02	59.43	62.90	64.87	70.15	72.43	81.32
2PASCL	20.41	21.91	22.30	25.71	31.49	33.10	39.92
QSERL	22.41	23.42	24.71	27.13	34.22	37.27	41.15
2PADCL	43.58	43.96	44.76	49.41	55.24	57.76	61.39
CCAL	2.051	2.277	3.138	3.713	4.997	5.854	8.329
2PADL	1.822	1.973	2.216	3.027	4.127	5.293	7.294
DFAL	2.073	2.916	3.957	4.786	5.858	6.012	9.438
A-DCVSL	3.112	3.543	4.011	4.991	6.337	7.881	10.61
Proposed	1.681	1.717	1.774	2.251	2.892	3.316	5.257

In Mozaffari et al. (2017), the Berkeley (HP-PTM) was compared at 45 nm and 16 nm, respectively. The average power consumption of each circuit is calculated using Cadence Virtuoso, an analog design environment, as shown in Figs. 7.15 and 7.16. The average power consumption of the proposed circuit with 45 nm HP_PTM at various frequencies is shown in Fig. 7.15. Figure 7.16 also depicts the average power consumption of standard CMOS with 45 nm HP_PTM at various frequencies.

Table 7.2: Performance Evaluation of Basic Gates on 16nm HP_ PTM Using Standard CMOS and Referenced Adiabatic Logics at 100 MHz Frequency, Within 50nm Simulation Time

16nm_HP_PTM						
Circuit Design	**Logic Gates**	**AVG. Power (nW)**	**Delays (ns)**	**PDP (fJ)**	**Energy (fJ)**	**EDP (E-24J)**
CMOS	OR	690.5	0.031405	0.021685	27.62	0.867406
	AND	739.1	0.03055	0.022582	29.564	0.90318
ADCL	OR	366.1	1.20688	0.441839	14.644	17.67355
	AND	366.4	1.78331	0.653405	14.656	26.13619
2PASCL	OR	122.9	0.52634	0.064687	4.916	2.587487
	AND	149.6	0.65926	0.098625	5.984	3.945012
QSERL	OR	170.3	0.20248	0.034482	6.812	1.379294
	AND	151.5	0.41896	0.063472	6.063	2.538898
2PADCL	OR	268.7	0.57786	0.155271	10.748	6.210839
	AND	279.2	0.40878	0.114131	11.168	1.274619
CCAL	OR	73.45	0.49805	0.036578	2.938	1.463139
	AND	80.55	0.49805	0.040118	3.222	1.604733
2PADL	OR	60.11	0.55812	0.033549	2.4044	1.341956
	AND	56.27	0.55011	0.030955	2.2508	1.238199
DFAL	OR	75.01	0.49861	0.037401	3.0004	1.496029
	AND	88.56	0.274625	0.024321	3.5424	0.972832
A-DCVSL	OR	92.25	0.66875	0.061692	3.6912	0.227644
	AND	86.73	0.574785	0.049851	3.4692	1.994044
Proposed	OR	50.06	0.622652	0.031170	2.0024	1.246798
	AND	51.02	0.55361	0.028245	2.0408	1.129807

The design parameters are such that, for 45nm technology, $L = 45nm$, $W_n = 400nm$, and $W_p = 600nm$, whereas, for 16nm technology $L = 16nm$, $W_n = 150nm$, and $W_p = 255nm$. Load capacitor is fixed at $10fF$ for both 45nm and 16 nm technologies, in 45nm_HP_PTM, $V_{in} = V_{DD} =$

$1V$, and $V_\phi = \overline{V_\phi} = 0.5V$whereas, in 16nm_HP_PTM, $V_{in} = V_{DD} = 0.7V$ and $V_\phi = \overline{V_\phi} = 0.35V$ as parameters presented in (Bhusan & Ketchen, 2014).

Table 7.1 shows the average power consumption of the inverter circuit of CMOS, the proposed circuit, and the reference adiabatic family at $20\ kHz$,$40\ kHz$,$50\ kHz$,$100\ kHz$,$200\ kHz$, $400\ kHz$, $500\ kHz$ and $800\ kHz$, respectively, using a 45nm HP_PTM. Table 7.2 illustrates the average power consumption, circuit delays, PDP, energy consumption, and EDP of CMOS, proposed circuits, and all reference circuits with respect to AND logic and OR logic functions using 16nm HP_PTM at a particular fixed frequency, say 100 MHz. The suggested circuit has improved performance in all scenarios, as shown by Tables 7.1 and 7.2.

7.4. BCD To Excess-3 Converter Circuit Based on Proposed Logic

The manner of coding in BCD requires at least four bits for each decimal number. For example, a decimal (27)10 will be equivalent to (0010 0111)2. The code is also known as 8-4-2-1 codes since 8, 4, 2, and 1 represent the BCD codes, which are of four bits. The block diagram and truth table of the code are shown in Fig.7.17 and Table 7.3, respectively.

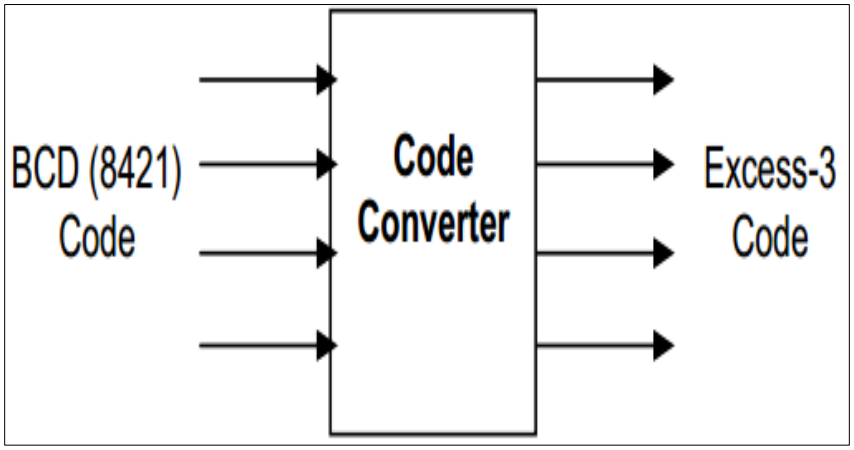

Fig.7.17: Block diagram of BCD to excess-3 code converter

On the other hand, the XS-3 code is derived from the BCD code by precisely appending binary three, i.e., $(0011)_2$, to each BCD number. The XS-3 code is a non-weighted code and is extremely important for arithmetic operations because, by virtue of this coding technique, the problem encountered by BCD can be rectified. The XS-3 coding technique is more advantageous than the

BCD method, as the former involves the nines' complement, which is extremely important for subtraction purposes. Both the inputs and outputs are four bits in total; the logic expressions of the conversion formulas employ NAND-gates, NOT-gates, XOR-gates, and XNOR-gates (Kumar & Bharathi, 2013; Morrison et al., 2014; D'heer et al., 2018).

*Table 7.3: **Truth Table of the BCD to Excess-3 Code***

Decimal	BCD (8421) Code				Excess-3 Code			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

From Table I the SOP of the output logics can be given as,

$$E_0 = \overline{B_0}$$
$$E_1 = B_1 \oplus B_0$$
$$E_2 = B_2 \oplus (B_1 + B_0)$$
$$E_3 = B_3 + B_2(B_1 + B_0) \quad (7.11)$$

The power-efficient circuit recommended for converting BCD (8421) code to Excess-3 code is seen in Fig.7.18. Figure 7.19 displays the outcome of the circuit simulation.

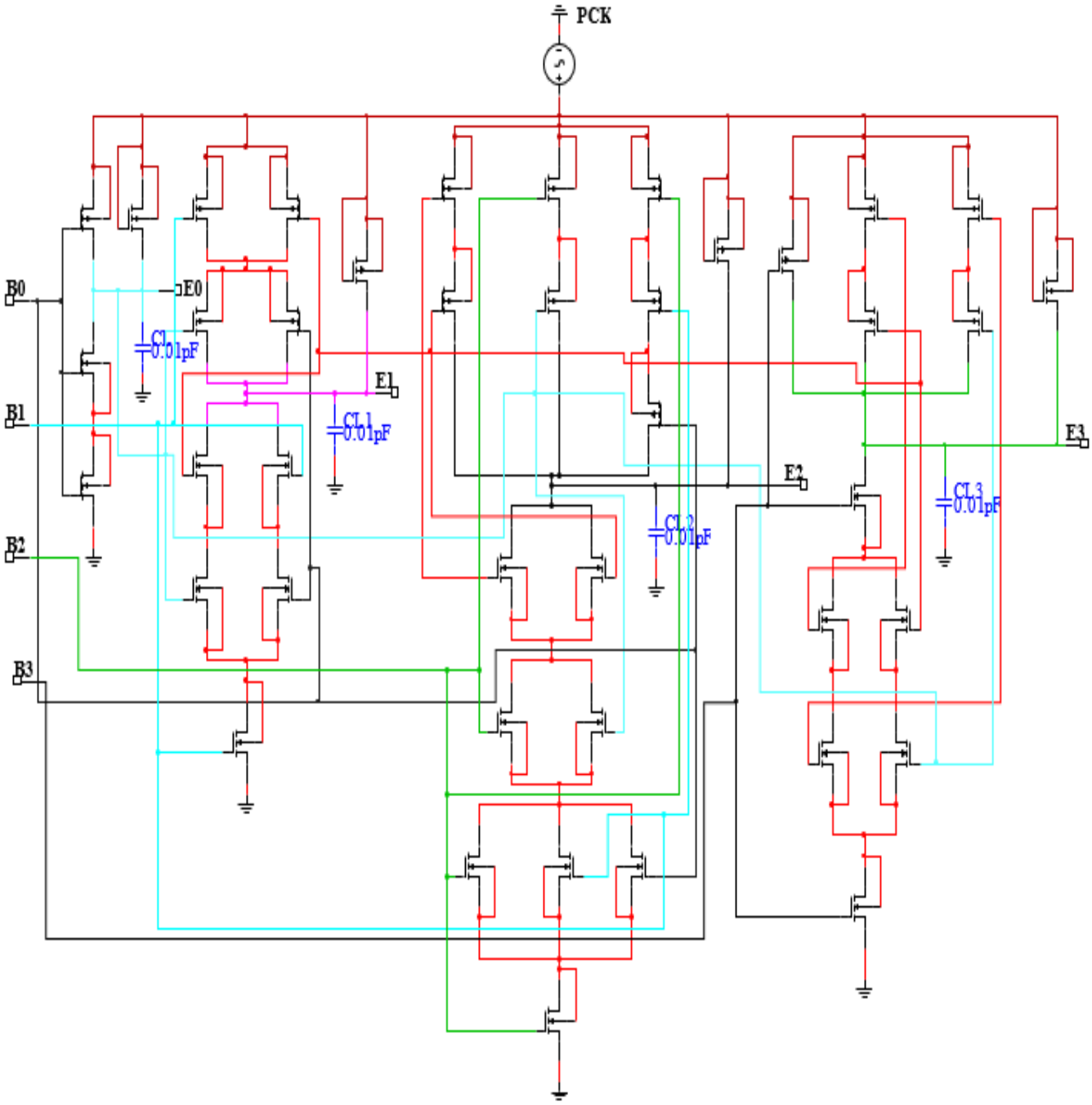

Fig.7.18: Recommended BCD to Excess-3 code converter circuit

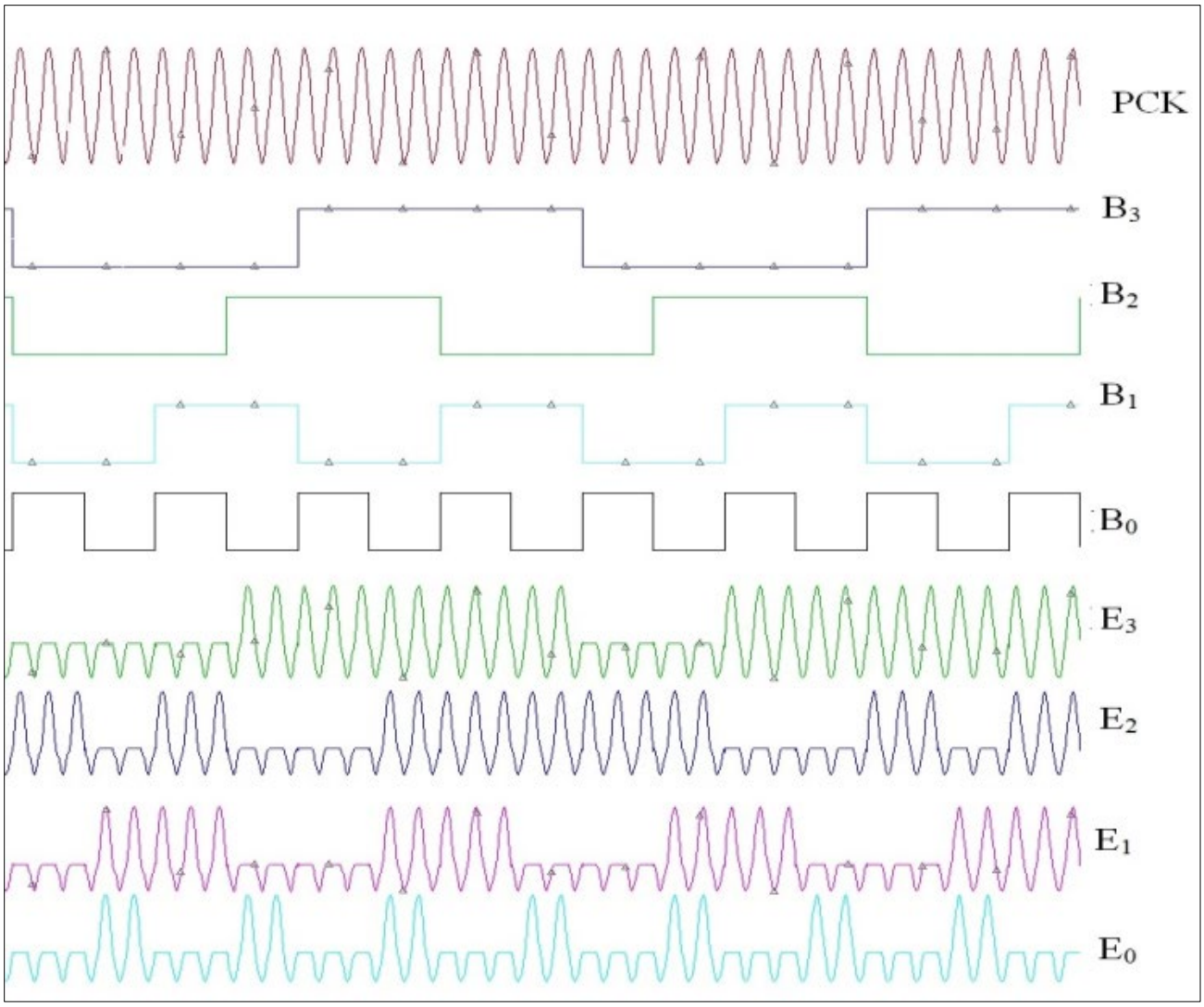

Fig.7.19: Inputs and outputs waveforms

7.5. Results and Discussion

At various frequencies, the deep analyses of the proposed standard adiabatic inverter circuit have been carried out based on different circuit parameters as shown in Figs. 7.20 -7.22. In Fig. 7.20, the output load capacitor current at different transition frequencies is depicted. The capacitor value is fixed at $0.01pf$. From the graph, it shows that the output load current is linear with respect to the operating frequencies. The RC equivalent of the proposed circuit is depicted in Fig. 7.13 in Section 7.2. During charging, the circuit behaves as a simple RC circuit, with the reactance of the capacitor indicated as $X_C = \frac{1}{\omega c} = \frac{1}{2\pi f c}$. The reactance X_C is inversely proportional to both capacitance and

operating frequency as $X_C \propto \frac{1}{c}$ and $X_C \propto \frac{1}{f}$. In the analysis, the capacitor value is maintained constant and fixed at $0.01pf$, although the frequency is varied. When the frequency of the supply voltage is high, the reactance value of the capacitor is low, and the capacitor works as a good conductor.

Figure 7.20 illustrates the relation between the load capacitor current and frequency of the supplied voltage. Here, we saw that a low frequency corresponds to a high reactance. Since the rate of voltage change accelerates with time, the charging current grows as the frequency rises. If the frequency is infinite, the reactance is zero, and the reactance value is infinity when the frequency is zero. As a result, the suggested adiabatic logic circuit precisely follows the features of a simple RC circuit with sinusoidal input supply voltage during charging. This demonstrates the concept of an RC-comparable circuit for the suggested circuit.

Figure 7.21 shows the output phase angle in degrees. Since the output load is capacitive, the load current leads the load voltage by 90 degrees. From the graph, the phase angle tends to rise from the 100 kHz frequency. Since the capacitor takes a certain amount of time to charge up, the current leads the voltage by a phase angle ϕ. The phase angle (ϕ) is given as,

$$\phi = \tan^{-1}\left(\frac{1}{\omega RC_L}\right) = \tan^{-1}\left(\frac{1}{2\pi fRC_L}\right) \tag{7.12}$$

The capacitor dominates the series RC circuit's impedance at low frequencies, causing the voltage to be 90 degrees behind the current. This clearly shows that the proposed adiabatic circuit's charging current leads the voltage by 90 degrees while charging at a low frequency. However, as the frequency rises, the phase difference reduces until, at a very high frequency, the impedance approaches R and the phase difference is zero. Thus, the circuit somehow behaves as a high-pass filter circuit with a phase shift that starts at 90 degrees. Figures 7.20 and 7.21 make it evident that the suggested circuit functions as a pure RC circuit with a sinusoidal voltage source when it is charging. Figure 7.22 also shows the power dissipation of a proposed inverter circuit at various load capacitors with respect to different operating frequencies. The load capacitor is allowed to increase from zero to 500 fF at a rate of 125 fF. It is clear that at a given frequency, the power consumption of the circuit increases with an increase in load capacitance.

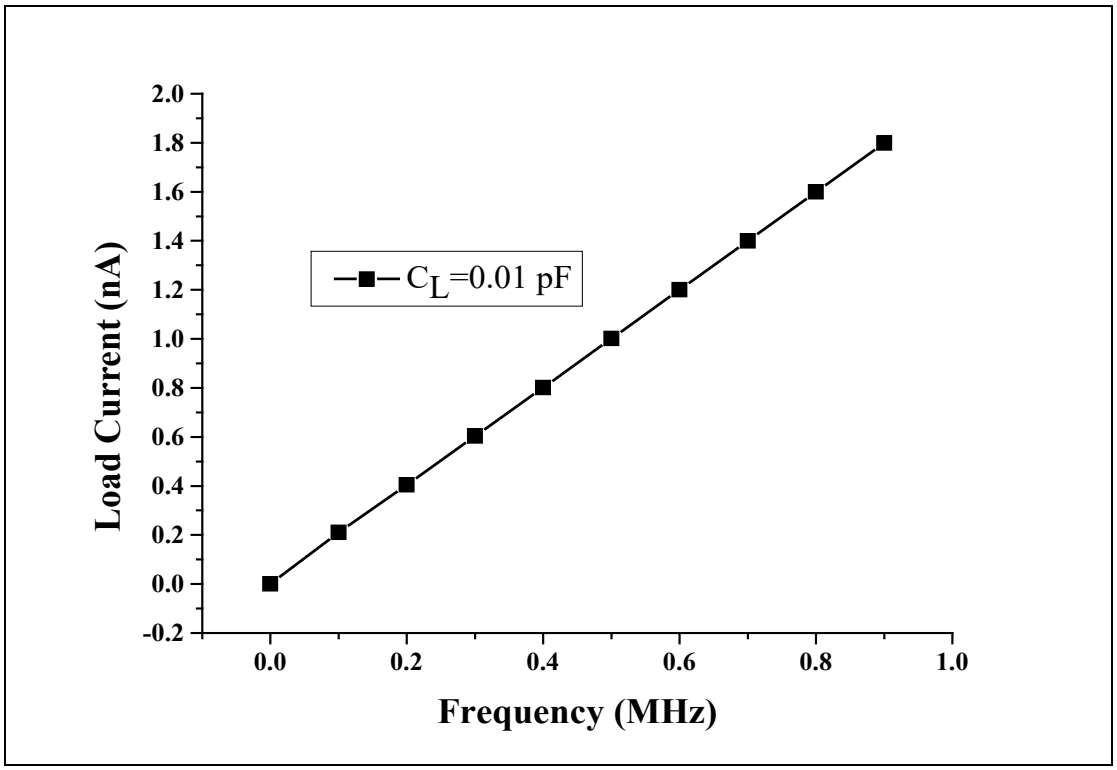

Fig.7.20: Load capacitor current vs. operating frequency

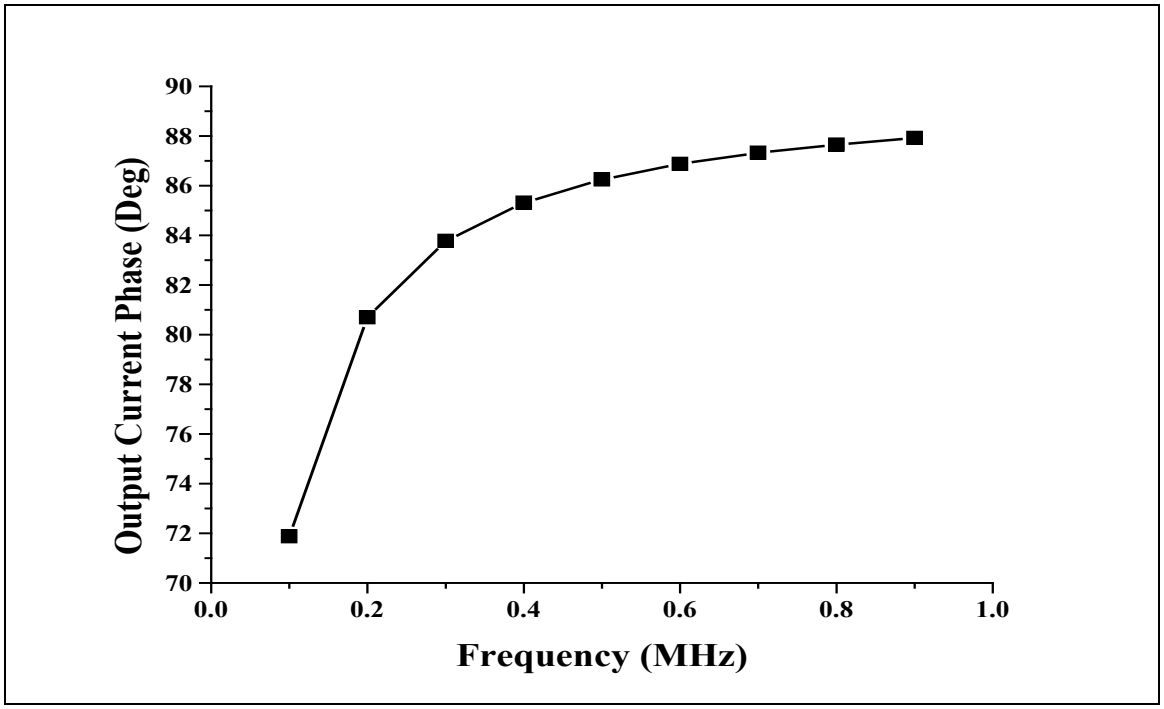

Fig.7.21: Output current phase vs. operating frequency

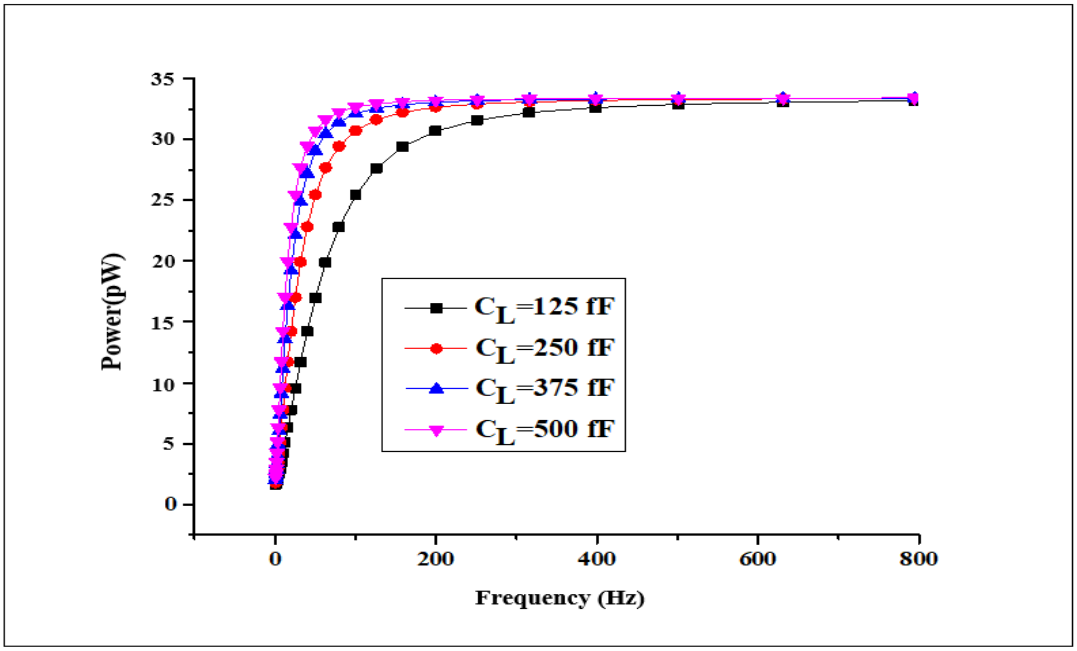

Fig.7.22: Power consumption vs. load capacitor

Fig. 7.23 depicts the power analysis of the proposed inverter circuit between 100 MHz and 900 MHz operating frequencies. From the graph, it is clear that the proposed circuit has better performance and consumes the least power when compared against CMOS and other adiabatic logic devices like ADCL and 2PASCL.

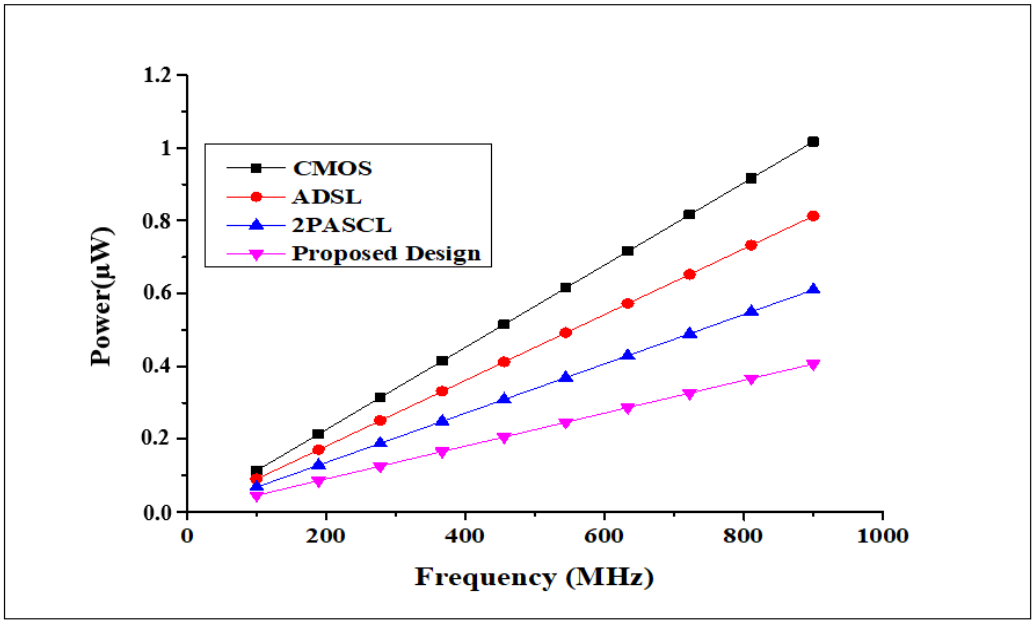

Fig.7.23: Power consumption vs. lower operating frequency (up to 900MHz)

The analysis is further extended to high frequency, as shown in Fig. 7.24. The range of analysis is between 1 GHz and 10 GHz. Even at higher frequencies, the performance of the proposed inverter circuit shows better results than the counterpart CMOS and other adiabatic literature such as ADCL and 2PASCL, which are the most popular in power optimization among the existing adiabatic logic families. However, as seen from Figs. 7.23 and 7.24 at all frequencies, the new design technique has better performance against other design styles in terms of power loss reduction and optimization (Takahashi & Mizunuma, 2000; Anuar et al., 2010). In addition to that, the new design method has another advantage when compared to other design techniques in terms of operating speed. In Fig. 7.25, the input and output waveforms of inverter circuits for ADCL, 2PASCL, and the proposed design are given. The work is performed at a 0.01 fF load capacitor and a 5-volt power clock.

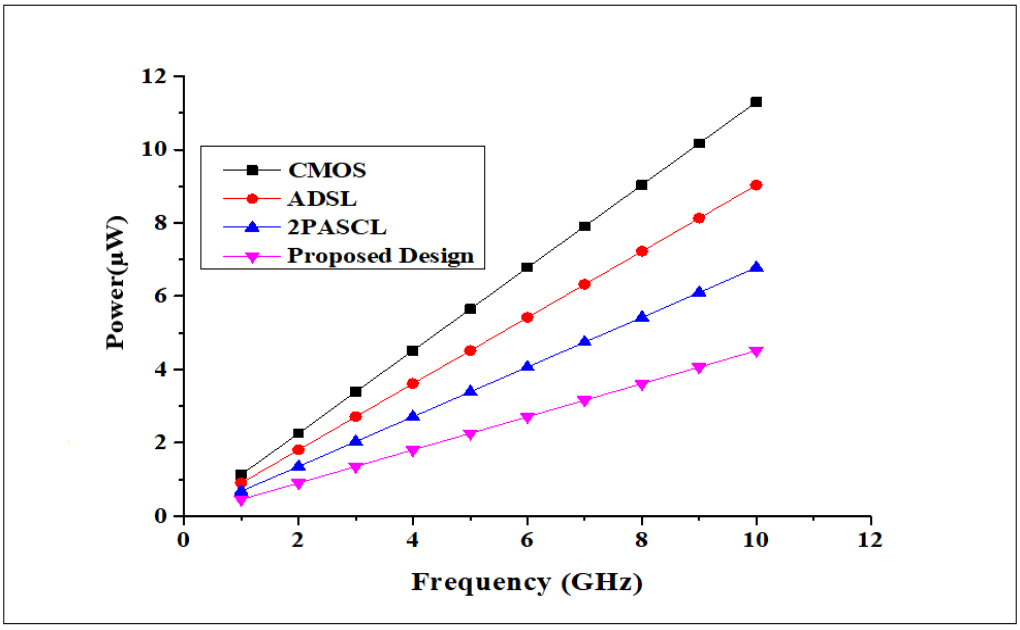

Fig.7.24: Power consumption vs. higher operating frequency (up to 10GHz)

Figure 7.25 displays the results of a transient investigation; both the input and power supply are sinusoidal or alternating in nature. As a result, the outputs become sinusoidal. The rise time for each particular design technique, such as ADCL, 2PASCL, and proposed logic, is calculated at a given rise range, as shown in Fig. 7.25. As per the simulation results, the rise times for ADCL and 2PASCL are 0.05969s and 0.05966s, respectively, whereas the proposed circuit has a rise time of 0.04555s. The amplitude of the output voltages may not be the same at a particular time due to the effect of the load capacitor and different design techniques for each literature. From this

investigation, it is clear that the proposed circuit has a quicker response time and is faster than the others. Therefore, the proposed circuit is not only superior in power optimization but also improves the speed of operation of the circuit (Chong et al., 2005; Huang & Ercegovac, 2005; Chen & Chu, 2007).

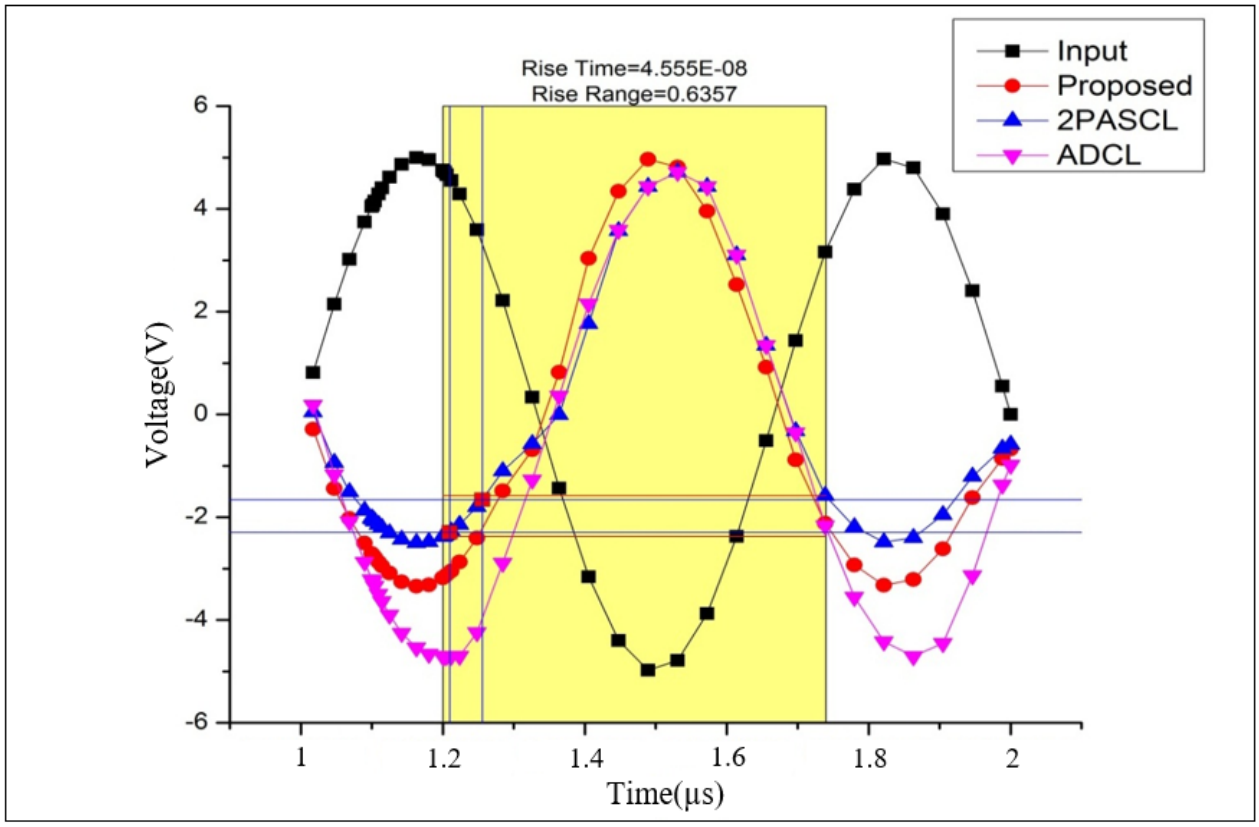

Fig.7.25: Input and output waveforms of inverter for ADCL, 2PASCL and the proposed design

The power consumption for 0.3µm CMOS technology is evaluated with the help of NI Multisim. The simulation frequency is set between 100 MHz and 900 MHz. All the output node capacitor values are kept at 0.01 pf. The aspect ratio (W/L) is the same for both PMOS and NMOS, such that channel length L = 0.3µm and channel width W = 0.75µm. The magnitudes of the power clock and the input logic are kept at 5V each, i.e., V_{PCLK} = 5V and V_{in} = 5V. The graphical power analysis result of the proposed circuit for BCD (8421) code to Excess-3 code converter circuit is shown in Fig. 7.26 along with references employed—2PASCL, ADCL, and typical CMOS. Hence, the power losses have been evaluated at a particular frequency. Measurements of power have been taken at intermediate and high frequencies, i.e., at 100 MHz and 900 MHz (Kim et al., 2003; Alioto &

Palumbo, 2001; Houri et al., 2015; Chang et al., 2010; Kim et al., 2003; Maksimovic et al., 2000; Gong et al., 2008).

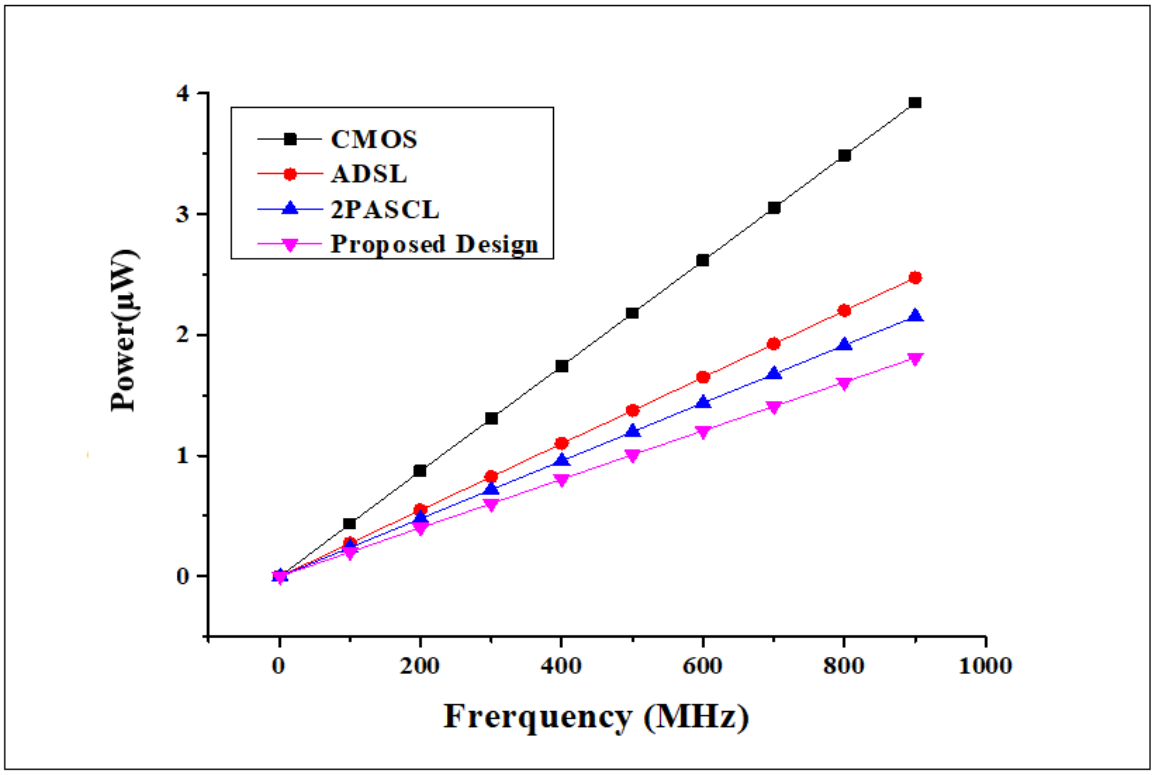

Fig.7.26: Power analysis of BCD to Excess-3 code converter circuit

Table 7.4 depicts the comparison table of different parameters (transistor count, area, and total power consumption for 500 MHz and 900 MHz) for CMOS, ADCL, 2PASCL, and the proposed logic. From the results, it is clear that the proposed circuit has better performance and consumes the least power when compared against CMOS, ADCL, and 2PACL logics. Table 7.5 illustrates the comparison table of power saving percentages at 500 MHz with respect to CMOS, ADCL, and 2PACL logic for BCD to Excess-3 code converter. It clearly demonstrates the advantages of the proposed adiabatic logic technique. Chip area, or the area of occupancy of a device or substrate, is greatly affected by the gate area or effective area, which is related to the product of channel length L and channel width W. For any logic function, the design based on adiabatic logic techniques has a higher a higher transistor count than a traditional CMOS design, as adiabatic circuits require extra transistors for energy recovery. The schematic topologies and energy recovery techniques of various adiabatic logic families determine the number of transistors. The total effective area, which affects

the whole chip size, grows in direct proportion to the number of transistors used in a logic circuit *(total effective area/gate area for each substrate=WxLxTransistorCount)*—a factor that is crucial to designers (Ren et al., 2018).

Table 7.4: Evaluation of Different Logic Designs for a BCD to Excess-3 Code Conversion Circuit

Parameters	CMOS Logic	ADCL Logic	2PASCL Logic	Proposed Logic
Transistor count	30	38	38	38
Total Effective Area per chip (μm^2)	6.75	8.55	8.55	8.55
Total power consumption (µW) [at 500 MHz]	2.2	1.4	1.2	1
Total power consumption (µW) [at 900 MHz]	3.9	2.6	2.2	1.8

Table 7.5: Power Saving in Percentage for Proposed Logic At 500 MHz with respect to CMOS, ADCL and 2PASCL for BCD to Excess-3 Code Converter

CMOS	ADCL	2PASCL
54.54%	28.57%	16.67%

In Fig. 7.27, the average dynamic power loss of conventional CMOS, and all the referenced adiabatic families at 100MHz operating frequency using a 16nm HP_PTM is illustrated. The simulation parameters are the same as discussed in Section 3. Figure 7.27 reveals the efficacy of the proposed circuit in power optimization when compared to other design methodologies. Table 7.6 shows that at low-frequency and small technology nodes, power consumption is considerably reduced, and power savings for the proposed circuit are increased when compared to other design techniques.

Table 7.6: Power Saving in Percentage for Proposed Logic Using Berkeley 16nm_HP_PTM at 100 MHz for BCD to Excess-3 Code Converter

CMOS	QSERL	2PADCL	A-DCVSL	DFAL	2PADL	ADCL	CCAL	2PASCL
74.72%	39.32%	40.61%	14.67%	10.71%	51.64%	51.64%	5.66%	36.06%

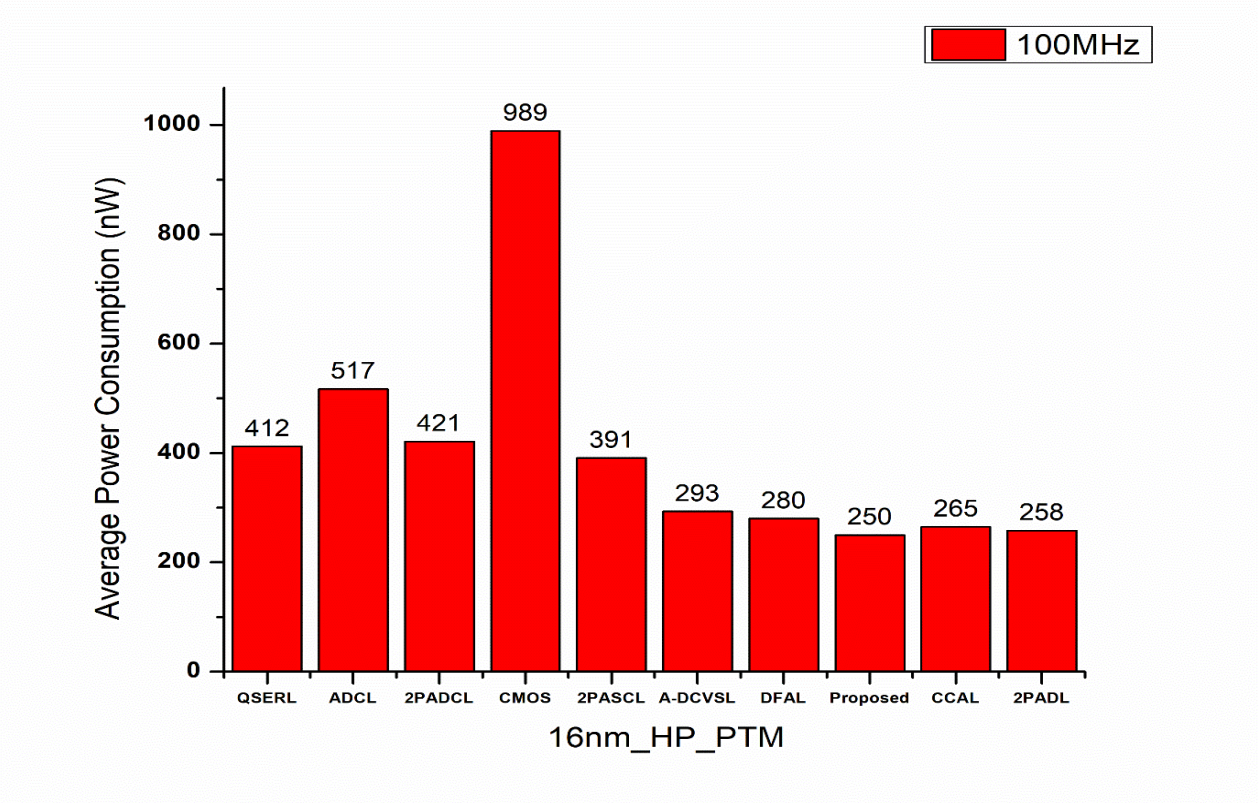

Fig.7.27. Average Power Consumption of BCD to Excess-3 code converter circuit using 16nm_HP_PTM, within 5 clock cycles at 100 MHz

7.6. Summary

The proposed adiabatic logic for the BCD to Excess-3 code converter is aimed at minimizing its power dissipation. Simulations and analyses were performed using 0.3 µm CMOS with NI-Multisim. The simulation results were also validated for numerous adiabatic logic design techniques: ADCL, 2PASCL, QSREL, 2PADCL, CCAL, 2PADL, DFAL, A-DCVSL, and the proposed circuit using high performance predictive technology nodes such as 16nm HP_PTM and 45nm HP_PTM. The circuit diagram, simulated input and output waveforms, and power analyses have been clearly shown. From the power analyses and observation tables, one can notice that the proposed logic circuit has better power utilization at low, medium, and high frequencies. Moreover, the proposed circuit has spectacular percentage power savings against referenced circuits at 0.3 µm CMOS technology and 16 nm HP_PTM, respectively. Furthermore, the suggested logic exhibits faster performance when contrasted with other design methodologies. Consequently, the proposed logic would be advantageous for the building of low-power VLSI circuits in the future.

CHAPTER-8

Conclusion and Future Scope

8.1. Conclusion

The present thesis, titled "Investigation of Adiabatic and Quasi-Adiabatic Logic Techniques for Digital CMOS Circuits," encompasses a comprehensive examination of adiabatic logic circuits. The investigation commences with an exploration of fundamental design methodologies and an intensive study of existing literature. The objectives outlined in the synopsis were successfully accomplished, as evidenced by the thorough examination of multiple adiabatic logic and quasi-adiabatic logic circuits in chapters 3–7. Furthermore, novel design techniques for standard adiabatic logic, quasi-adiabatic logic, cross-couple type, single-phase power supply, and split-level dual power supply with 180-degree phase shift were introduced. The strategies developed in this study demonstrated superior power optimization capabilities and reduced circuit propagation delay in comparison to the most recent design techniques available in the literature.

In this work, the IDFAL circuit, which is an upgraded form of diode-free adiabatic logic, has been introduced. It uses two control transistors to minimize output node floating and reduce leakage current and power. The circuit also has a parallel additional transistor across the pull-down network, reducing discharging resistance and dynamic power consumption. The IDFAL circuit saves an average power of 92.6%, 95.5%, 96.2%, and 96.5% against CMOS at various high-performance predictive technology nodes. It also achieves power savings of 83.17%, 57.42%, 49.88%, 23.95%, 10.37%, and 5.39% when creating an SR flip-flop and a 1-bit comparator. The IDFAL is ideal for creating complex circuits involving sequential and combinational circuits. The work also presented adiabatic switching ideas, which were subsequently used in a 16-bit ALU architecture that made use of MOSFET and FinFET technology. In terms of power savings, the method achieves a result of 95.22%, 21.34%, 20.75%, 15.66%, and 8.69% when using MOSFET technology for CMOS, QSERL, ADCL, and 2PASCL; and 39.47%, 34.65%, 8.73%, and 4.16% when using FinFET technology. Power consumption was assessed using SPICE and NI Multisim-14.1 with 32nm node technologies. The proposed adiabatic technique, which is standard or fully adiabatic, shows better performance in terms of power utilization.

Later the work proposes and discusses a new family of adiabatic logic referred to as EPFAL. Utilizing quasi-adiabatic circuits based around sense amplifiers and dual-rail encoding, this family of logic is constructed. A two-phase sinusoidal power-clock source powers it, allowing for optimal dynamic power consumption and minimizing leakage power consumption. When compared to other logic families, the EPFAL circuit achieves considerable power savings. EPFAL offers ideal dynamic power usage and reduced leakage power loss compared to conventional PFAL. The proposed EPFAL inverter saves 53.05%, 27.88%, 27.15%, 31.05%, 37.06%, 37.44%, 34.42%, 15.55%, and 23.72% of average power compared to CMOS, 2N-2N2P, 2P-PFAL, IPGAL, DCPAL, ECRL, PFAL, A-DCVSL, and CDCAL circuits. Comparative performance assessment demonstrates EPFAL's superiority to CMOS and IDFAL, making it advantageous for upcoming low-power VLSI circuit applications. The proposed BCD-to-Excess-3 code converter, with an emphasis on reducing power consumption, is also detailed in this work. A number of adiabatic logic design methods were used to do simulations and power evaluations. In comparison to the cited circuits, the suggested circuit showed considerable power savings and improved power usage at low, medium, and high frequencies. It also demonstrated higher speed, making it beneficial for future low-power VLSI circuit implementations.

It is imperative to acknowledge that adiabatic logic is not universally applicable and may not be the optimal choice for all digital circuit applications. In situations where the major focus is on power efficiency, this technology demonstrates exceptional performance. The benefits of decreased power usage outweigh any potential drawbacks, such as heightened circuit complexity. The efficacy of adiabatic logic for a specific use must be determined by the designers through a comprehensive assessment of their specific needs and constraints.

8.2. Future Scope

The future of adiabatic logic design can be improved by enhancing design tools, improving noise margin and robustness, exploring compatibility with quantum computing and neuromorphic computing, developing more efficient adiabatic charging and discharging schemes, and exploring its application in low-power and energy-harvesting systems. By addressing these challenges and exploring new frontiers, adiabatic logic can continue to evolve and offer innovative solutions in digital CMOS circuit design. By addressing these difficulties and investigating novel domains,

adiabatic logic may persist in providing inventive resolutions in the realm of digital CMOS circuit design.

Some prospective future directions for the research are outlined below.

- **Adiabatic CMOS Logic with Micro-Electro-Mechanical Systems (MEMS) Resonators:**

For CMOS digital logic to work as intended, a quasi-trapezoidal power-clock voltage waveform originating from a resonant element with a high-quality factor (Q) must be used. Particularly noteworthy are the increased frequencies and Q factors shown by MEMS resonators, which are finding increasing use in communication system-on-chip (SoC) applications, including the amplification and filtering of RF signals.

- **Adiabatic Power Reduction in Spacecraft:**

Power supplies like computers, solar panels, and cooling systems are very heavy and expensive to send into orbit; therefore, spaceships must reduce their adiabatic power use. This becomes particularly critical when these components contribute significantly to the total spacecraft weight.

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List of Publications

Journal Publications

1. R. H. Vanlalchaka, R. Maity, and N. P. Maity, "A power efficient fully adiabatic logic circuit design approach: Application to inverter and 8421 to excess-3 code converter," *Engineering Research Express* ***(IOP)***, vol. 5, no. 1, p. 015058, 2023, doi: 10.1088/2631-8695/acae1b.

2. R. H. Vanlalchaka, R. Maity, and N. P. Maity, "A low power design using FinFET based adiabatic switching principle: Application to 16-bit arithmetic logic unit," *Ain Shams Engineering Journal* ***(Elsevier)***, vol. 14, no. 4, p. 101948, 2023, doi: 10.1016/j.asej.2022.101948.

3. R. H. Vanlalchaka, R. Maity, and N. P. Maity, "Energy-efficient circuits with improved diode-free adiabatic logic design methodology," *Ain Shams Engineering Journal* ***(Elsevier)***, vol. 14, no. 8, p. 102049, 2023, doi: 10.1016/j.asej.2022.102049.

4. R. H. Vanlalchaka, R. Maity, L. Khiangte, D. Rosangliana, and N. P. Maity, "A novel adiabatic logic technique for low-power circuit applications," *Microsystem Technologies* ***(Springer),*** pp. 1-20, 2025.

5. R. H. Vanlalchaka, R. Maity, R. L. Ralte, L. R. M. Punte, P. C. Rohmingliana, R. Lalawmpuii, and N. P. Maity, "Architectural design of sequential circuit based on improved diode-free adiabatic logic," *Analog Integrated Circuits and Signal Processing* ***(Springer),*** accepted for publication, July 2025.

Conference Publications

1. R. H. Vanlalchaka and N. P. Maity, "Power efficient 8421 code to excess-3 code converter," in *Proceedings of the International Conference on Recent Trends in Electronics & Computer Science (ICRTECS)*, March 18-19, 2019.

2. R. H. Vanlalchaka and N. P. Maity, "Efficient low-power circuits with enhanced positive feedback adiabatic logic (EPFAL)," in *Proceedings of the 10th International Conference on Microelectronics, Circuits & Systems (Micro-2023)*, July 1-3, 2023.

3. R. H. Vanlalchaka and N. P. Maity, "New combinational circuit approach using improved diode free adiabatic logic families," in *Proceedings of the 6th International Conference on Energy Systems, Drives and Automations (ESDA2023)*, Kolkata, India, Dec. 30-31, 2023, p. 16.

Granted Patent – Intellectual Property Contribution (Government of India)

Patent Title: “An Ultra-Low Power VLSI Circuit Design Technique”

Patent No.: 564217

Application No.: 202131003952

Inventors: Niladri Pratap Maity, Reginald H. Vanlalchaka, Reshmi Maity

Filed on: 29 Jan 2021

Granted on: 28 Mar 2025

Issuing Authority: The Patent Office, Government of India

Patent Duration: 20 years (from 29 Jan 2021)

क्रम सं/Sl. No :033138402

INTELLECTUAL PROPERTY INDIA
PATENTS | DESIGNS | TRADE MARKS
GEOGRAPHICAL INDICATIONS

सत्यमेव जयते

पेटेंट कार्यालय,भारत सरकार
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(पेटेंट नियमावली का नियम 74)

The Patent Office, Government Of India
Patent Certificate
(Rule 74 of The Patents Rules)

पेटेंट सं. / Patent No. : 564217

आवेदन सं. / Application No. : 202131003952

फाइल करने की तारीख / Date of Filing : 29/01/2021

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प्रमाणित किया जाता है कि पेटेंटी को, उपरोक्त आवेदन में यथाप्रकटित *AN ULTRA-LOW POWER VLSI CIRCUIT DESIGN TECHNIQUE* नामक आविष्कार के लिए, पेटेंट अधिनियम, 1970 के उपबंधों के अनुसार आज तारीख जनवरी 2021 के उन्नतीसवें दिन से बीस वर्ष की अवधि के लिए पेटेंट अनुदत्त किया गया है।

It is hereby certified that a patent has been granted to the patentee for an invention entitled *AN ULTRA-LOW POWER VLSI CIRCUIT DESIGN TECHNIQUE* as disclosed in the above mentioned application for the term of 20 years from the 29th day of January 2021 in accordance with the provisions of the Patents Act,1970.

अनुदान की तारीख : 28/03/2025
Date of Grant :

पेटेंट नियंत्रक
Controller of Patents

टिप्पणी - इस पेटेंट के नवीकरण के लिए फीस, यदि इसे बनाए रखा जाना है, जनवरी 2023 के उन्तीसवें दिन को और उसके पश्चात प्रत्येक वर्ष में उसी दिन देय होगी।

Note. - The fees for renewal of this patent, if it is to be maintained, will fall / has fallen due on 29th day of January 2023 and on the same day in every year thereafter.

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Date of Admission	**:**	**03.08.2018**
Approval of Research Proposal:		
1. DRC	**:**	**24.01.2019**
2. BOS	**:**	**23.04.2019**
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ABSTRACT

INVESTIGATION OF ADIABATIC AND QUASI-ADIABATIC LOGIC TECHNIQUES FOR DIGITAL CMOS CIRCUITS

AN ABSTRACT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSHOPHY

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SCHOOL OF ENGINEERING AND TECHNOLOGY

JULY 2025

INVESTIGATION OF ADIABATIC AND QUASI-ADIABATIC LOGIC TECHNIQUES FOR DIGITAL CMOS CIRCUITS

BY

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Submitted
In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Electronics & Communication Engineering of Mizoram University, Aizawl

Introduction

The semiconductor industry has experienced extraordinary progress, beginning with the invention of the transistor and advancing to the development of Very Large Scale Integration (VLSI) technology. The transition from Small Scale Integration (SSI) to Medium Scale Integration (MSI), Large Scale Integration (LSI), and eventually VLSI has facilitated the incorporation of an increasing number of transistors on a single chip. This evolution has enabled the creation of electronic devices that are more compact, powerful, and energy-efficient. In alignment with Moore's Law, modern integrated circuits (ICs) now house billions of transistors, significantly enhancing processing capabilities. However, as the number of transistors continues to increase, power density becomes a critical design challenge. While technological advancements in manufacturing have enabled the scaling of transistors, the high power density in these compact ICs restricts designers, particularly for low-power applications, from fully utilizing these capabilities. The significance of low-power design is increasingly paramount, particularly as advancements in battery technology have not kept pace with the demands of modern electronic devices. The rising prevalence of high-speed systems, including microprocessors, has led to elevated power consumption, increased reliability concerns, and thermal management challenges. For portable and high-performance systems, where power dissipation is directly linked to clock frequency, minimizing power consumption is essential. A variety of strategies, ranging from device-level optimizations to algorithmic techniques, have been employed to manage power usage effectively. While improvements in transistor density and switching speed have bolstered system performance, they have also exacerbated power and energy dissipation, leading to higher costs in cooling and packaging solutions. As high-end microprocessors are projected to consume even more power in the future, it is crucial to develop innovative solutions that address these challenges in a sustainable and cost-effective manner.

Adiabatic logic represents an innovative approach in digital circuit design, offering a promising solution to the challenges of power dissipation and energy efficiency in

modern electronics. This paradigm shifts from conventional digital logic, which is energy-intensive, towards a design philosophy that emphasizes energy conservation. By mimicking the thermodynamic principle of adiabatic processes—where a system does not lose or gain energy—adiabatic logic circuits achieve significant reductions in power consumption and heat generation. These circuits are particularly well-suited for applications requiring high energy efficiency, such as mobile devices, Internet of Things (IoT) systems, and other portable electronics. The principle of reversible computation underpins this technology, recovering energy that would otherwise be lost as heat in traditional circuits. Through specialized clocking schemes, advanced energy storage techniques, and novel circuit architectures, adiabatic logic holds the potential to revolutionize low-power design. Given the limitations of conventional low-power design methodologies across various hierarchical levels—such as system, algorithm, architecture, circuit, and device—adiabatic logic presents a compelling alternative. This thesis focuses on the development of energy-efficient digital circuits based on adiabatic switching principles, offering new insights into the design of low-power systems.

Objectives

- To investigate digital CMOS circuits based on adiabatic and quasi-adiabatic logic techniques
- To design new adiabatic logic techniques aimed at reducing power consumption when compared against the current existing literature.
- To minimize the weight and area per chip.
- To improve speed of operations and reduce delay of signal propagations.

Adiabatic logics such as ADCL, 2PASCL, QSERL, along with quasi-adiabatic logics like CAL, PAL, and PSAL, have been extensively investigated in the context of digital CMOS circuit design. In an effort to address both dynamic and leakage power consumption, several novel adiabatic logic design techniques have been proposed. These

include a single-phase fully adiabatic technique, which has been applied in novel FinFET arithmetic logic unit (ALU) designs, and a 3P-1N adiabatic logic based on 2PASCL, utilized for designing an 8421 Code to Excess-3 Code Converter. Additionally, a novel improved diode-free adiabatic logic (IDFAL) and Enhanced Positive Feedback Adiabatic Logic (EPFAL) have been introduced. Comparative analysis with existing literature demonstrates that these proposed logics yield significant improvements, including a smaller Total Effective Area per chip (μm^2), reduced transistor count, and superior power efficiency in FinFET 16-bit ALUs and 8421 Code converter circuits. Furthermore, the IDFAL technique exhibits reduced circuit delay, enhanced power delay product (PDP), and improved energy delay product (EDP), establishing it as a more efficient alternative in low-power circuit design.

Summary

The present thesis, titled "Investigation of Adiabatic and Quasi-Adiabatic Logic Techniques for Digital CMOS Circuits," provides a comprehensive analysis of adiabatic logic circuits, beginning with an exploration of foundational design methodologies and a critical review of existing research. The objectives set forth in the research have been successfully achieved, as demonstrated by the in-depth analysis of various adiabatic and quasi-adiabatic logic circuits. Throughout the study, novel design techniques were introduced, including standard adiabatic logic, quasi-adiabatic logic, cross-coupled configurations, single-phase power supply systems, and split-level dual power supply mechanisms with 180-degree phase shifts. These innovative approaches have shown significant improvements in power optimization and reduction of circuit propagation delay when compared to the latest techniques documented in the existing literature. The organization of this thesis reflects the structured approach to addressing these advancements and their practical implications.

Chapter 1 provides a detailed discussion on the evolution of semiconductor technology, beginning with the introduction of Small Scale Integration (SSI), Medium Scale Integration (MSI), and Large Scale Integration (LSI), leading to the current

advancements in Very Large Scale Integration (VLSI). The chapter emphasizes the growing demand for low-power devices and thoroughly explores the power consumption challenges in digital Complementary Metal-Oxide-Semiconductor (CMOS) designs, focusing on dynamic and static power consumption. Furthermore, various techniques currently available for low-power design methodologies are analyzed, and the inherent limitations of these methods are discussed.

Chapter 2 presents a comprehensive review of existing adiabatic logic design techniques, following a chronological order of their development. This chapter includes a detailed explanation of quasi-adiabatic design techniques, particularly those with cross-coupled structures, supported by diagrams to enhance understanding. Analytical descriptions of adiabatic switching technology are provided, elucidating the benefits of adopting adiabatic logic for achieving low-power digital CMOS architecture.

Chapter 3 introduces an improved diode-free adiabatic logic (IDFAL) technique, which eliminates the need for diodes by employing a two-phase complementary sinusoidal power supply. The chapter explains how the circuit's operation is sustained using the principle of adiabatic switching. Extensive simulations and analyses are conducted to evaluate the performance of IDFAL across several CMOS technology nodes. The results demonstrate a 91.59% reduction in the power delay product (PDP) for the IDFAL inverter circuit compared to its conventional CMOS counterpart using a 16 nm High Performance Predictive Technology Model (HP_PTM).

Chapter 4 investigates the performance of the IDFAL circuit in comparison to traditional CMOS logic and other alternative design approaches. The chapter describes the IDFAL circuit's use of a split-level sinusoidal power source and a dual-phase timing mechanism. Various sequential and combinational logic circuits, including SR, D, and T flip-flops, are evaluated at the 45 nm scale using IDFAL. The findings highlight that the IDFAL circuit achieves the lowest energy delay product (EDP) and PDP compared to existing adiabatic designs, as confirmed by simulations performed with Cadence Virtuoso and Spectre simulators.

Chapter 5 explores the single-phase diabatic logic technique, an innovative logic design approach introduced in this chapter. A comprehensive blueprint of a 16-bit arithmetic logic unit (ALU) is presented, incorporating both MOSFET and FinFET fabrication technologies and utilizing adiabatic switching principles. The analyses indicate significant power savings for MOSFET technology—67.14%, 39.47%, 34.65%, 8.73%, and 4.16%—and even higher savings for FinFET technology—95.22%, 21.34%, 20.75%, 15.66%, and 8.69%.

Chapter 6 focuses on the development of Enhanced Positive Feedback Adiabatic Logic (EPFAL), a low-power adiabatic logic technique based on sense-amplifier-structured quasi-adiabatic circuits and dual-rail encoded architectures. EPFAL leverages two-phase sinusoidal power-clock sources and is affected by factors such as charge recovery, adiabatic and non-adiabatic losses, unclaimed charge, charge sharing, and drift effects. This chapter presents the design and evaluation of odd and even parity generators and checker circuits based on EPFAL, demonstrating power savings of 77.53% and 82.14%, respectively, when compared to traditional CMOS architectures.

Chapter 7 introduces a fully adiabatic binary-coded-decimal (BCD) to Excess-3 (XS-3) code converter prototype. This design showcases significantly reduced power consumption compared to standard CMOS logic and other prominent fully adiabatic logic families. The proposed logic achieves remarkable power savings at 500 MHz, surpassing conventional CMOS implementations, highlighting the potential of BCD in modern VLSI design for achieving energy efficiency.

Chapter 8 provides a comprehensive conclusion to the research, summarizing all major findings and their broader implications. A critical analysis of the advantages and disadvantages of adiabatic logic is conducted, and potential solutions to the limitations of adiabatic switching are explored. The chapter also outlines future directions for research in this domain, proposing areas for further investigation to advance the development of low-power design techniques.