MODELING AND PERFORMANCE ANALYSIS OF GAN BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT)

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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MODELING AND PERFORMANCE ANALYSIS OF GAN BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT)

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Submitted

In partial fulfillment of the requirement of the Degree of Doctor of Philosophy in Electronics & Communication Engineering of Mizoram University, Aizawl

CERTIFICATE

This is to certify that the thesis entitled "Modeling and Performance Analysis of GaN Based High Electron Mobility Transistor (HEMT)" submitted to Mizoram University for the award of the degree of Doctor of Philosophy Electronics and Communication Engineering by PICHINGLA KHAREI, Ph.D. Registration no. MZU/Ph.D./1456 of 26.07.2019, is a Ph.D. scholar in the Department of Electronics and Communication Engineering, under our guidance and supervision and has not been previously submitted for the award of any degree in any Indian or foreign University. She has fulfilled all criteria prescribed by the UGC (Minimum Standard and Procedure governing Ph.D. Regulations). She has fulfilled the mandatory publication (Publication enclosed) and completed Ph.D. course work. It is also certified that the scholar has been admitted in the Department through an entrance test, followed by an interview as per UGC Regulation of 2016.

Date: (Dr. Achinta Baidya)

Place: Aizawl Supervisor

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DECLARATION

MIZORAM UNIVERSITY

APRIL, 2026

I **PICHINGLA KHAREI**, hereby declare that the subject matter of this thesis is the record of work done by me, that the contents of this thesis did not form the basis for the award of any previous degree to me or, to the best of my knowledge, to anybody else, and that the thesis has not been submitted by me for any research degree in any other University/Institute.

This thesis is being submitted to the Mizoram University for the **Degree of Doctor of Philosophy in Electronics and Communication Engineering.**

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(Pichingla Kharei)

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CHAPTER 1

Introduction

1.1 Semiconductor Technology and Industry Evolution Overview

The first transistor, developed in 1947 by the Bell Labs team of Shockley, Bardeen, and Brattain, offered a smaller, more reliable, and energy-efficient alternative to bulky vacuum tubes, while enhancing signal amplification and control [1]. Initially, it was developed for telecommunications, but it quickly expanded into various applications, such as radios, televisions, and eventually computers. Its invention not only revolutionised computer science but also significantly impacted modern life. The inventors of the first transistor were honoured with the Nobel Prize in Physics, with Shockley often called the father of the transistor [2]. The first practical transistor was the point-contact device, which evolved into Shockley's bipolar junction transistor (BJT) in 1948 and later to the field-effect transistor (FET) in the 1950s, marking the start of widespread adoption of the transistor [3]. By 1960, transistors had replaced vacuum tubes as smaller, cheaper, and more reliable alternatives. The need for compact systems and the growing use of transistors in computers led to the independent invention of the integrated circuit (IC) by Jack Kilby in 1958 and by Robert Noyce and Jean Hoerni in 1959. Soon after, Atalla and Kahng introduced the metal-oxide semiconductor field-effect transistor (MOSFET) in 1959 [4], which became the dominant technology thanks to its scalability and low power consumption [5]. The constant miniaturisation of transistors, as predicted by Moore's Law [6], has led to the rapid growth in computational strength, driving the digital transformation and showcasing the transistor's enduring role as a backbone of advancements in science and industry. Although the semiconductor industry primarily relies on silicon (Si), advanced radio frequency (RF) transmitters require enhanced performance. This need has spurred the development of microwave and mm-wave transistors using materials like selenium germanide (SeGe), gallium arsenide (GaAs), silicon carbide (SiC), and gallium nitride (GaN). These materials

offer superior physical properties for high-frequency and high-power applications. Fig. 1.1 compares these key material properties [7, 8].

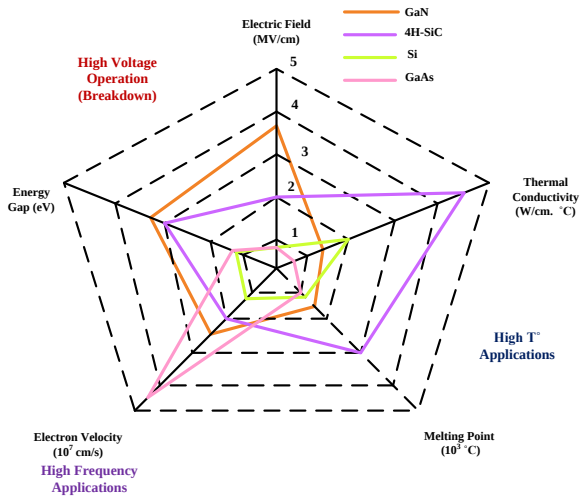


Fig. 1.1. Evaluation of semiconductor properties for use in high-power and high-frequency applications [8].

Transistors requiring high breakdown voltage (V_{br}) necessitate materials with a high critical electric field, making wide-bandgap options such as 4H-SiC and GaN ideal choices. High-power devices also require strong thermal conductivity, where SiC excels. For high-frequency operation, materials with high electron velocities, such as GaAs, SiC, and GaN, are most suitable. Alternative materials also offer unique benefits for power-frequency applications, as depicted in Fig. 1.2 [9]. While Si is outperformed by other materials, advanced Si-based devices like laterally-diffused metal-oxide semiconductor (LDMOS) transistors have improved performance, operating below 3 GHz and handling 10-100 W in power switching [10]. Meanwhile, 4H-SiC is used in advanced metal–semiconductor field-effect transistors (MESFETs), enabling high-performance power switches characterized by low on-resistance (R_{on}) and greater power capability [11].

For power amplifiers (PAs) in mobile handsets, silicon-germanium (SiGe) p-MOSFETs with 2-3 V operation, 1-2 W power, and high frequency are appealing because they are compatible with Si complementary metal-oxide-semiconductor (CMOS) technology. However, as frequency and linearity demands rise, GaAs devices such as high electron mobility transistors (HEMTs) and heterojunction

bipolar transistors (HBTs) [12] have become standard for applications up to 5 W. For high-power (above 10 W) and mm-wave frequency applications such as radar systems, satellite communications, and cellular base stations, GaN HEMTs fabricated on SiC or Si substrates represents the leading technology [13].

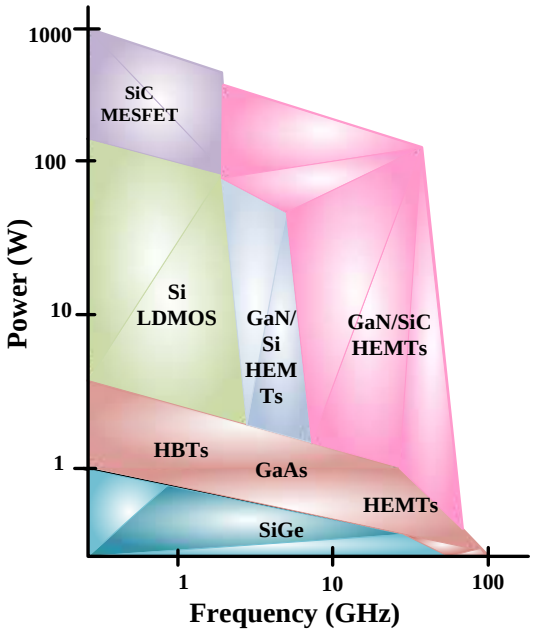


Fig. 1.2. Power-frequency range diagram for various semiconductor device technologies [9].

The aluminium gallium nitride/ gallium nitride (AlGaN/GaN) heterostructure's wide bandgap provides high V_{br}, allowing high drain voltages, reducing voltage conversion needs, and enhancing power efficiency, which is crucial for PAs [8]. The creation of HEMTs in the 1980s represented a paradigm shift in transistor technology, particularly for high-frequency and high-power applications [14]. HEMTs, also referred to as heterostructure FETs (HFETs), utilize the principle of modulation doping in heterojunctions, where two semiconductor materials with different band gaps, such as GaAs and aluminium gallium arsenide (AlGaAs), are combined. This design generates a two-dimensional electron gas (2DEG) at the interface, confining electrons in a narrow region with minimal impurity scattering [14-15]. A schematic diagram of AlGaAs/GaAs HEMT is given in Fig. 1.3. As a result, HEMTs exhibit exceptionally high electron mobility, enabling superior high-frequency performance and low noise characteristics compared to conventional

MOSFETs and BJTs [14]. The pioneering work on HEMTs by Takashi Mimura and his team laid the foundation for their widespread adoption in RF and microwave applications, including satellite communications, radar systems, and wireless networks [16].

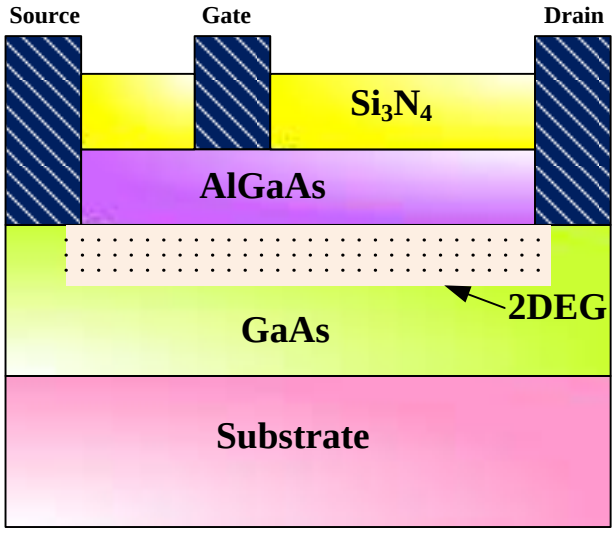


Fig. 1.3. Schematics of AlGaAs/GaAs HEMT.

In the mid-1980s, two key advancements significantly enhanced GaAs-based HEMTs for communication and radar applications. Ketterson *et al.* introduced the pseudomorphic HEMT (pHEMT) [17], which employed an AlGaAs/InGaAs/GaAs quantum well structure to improve electron transport and scalability. In heterojunction design, the ideal scenario involves two materials with perfectly matched lattice constants (atomic spacing). However, minor mismatches (such as in AlGaAs/GaAs systems) often lead to crystal defects. A pHEMT deliberately violates this rule by incorporating an ultrathin layer of one material—so thin that its lattice stretches to match the other material. This approach enables transistors with larger bandgap differences, resulting in superior performance [18]. The pHEMT is a high-frequency transistor featuring a thin, strained indium gallium arsenide (InGaAs) channel on a GaAs substrate, offering exceptional electron mobility. The term "pseudomorphic" indicates that the InGaAs layer, though slightly lattice-mismatched with GaAs, remains defect-free due to its minimal thickness. This design delivers high-speed operation with low noise, making pHEMTs ideal for satellite

communications and radar systems, where they outperform conventional HEMTs. Compared to standard HEMTs, pHEMTs provide better electron confinement and higher gain at microwave frequencies. However, their indium content is typically limited to 20-25% to avoid strain relaxation, which caps their performance at extremely high frequencies. Despite this, pHEMTs remain a cost-effective solution for RF applications below 100 GHz. Another breakthrough was planar doping [19], which incorporated thinned barriers to improve V_{br}, transconductance (g_m), and aspect ratio. These innovations allowed pHEMTs to achieve 0.1 μm gate lengths and record-setting noise/power efficiency at high frequencies. For larger lattice mismatches, an alternative approach involves inserting a buffer layer—a technique used in metamorphic HEMTs (mHEMTs), an evolution of pHEMTs. For instance, indium aluminium arsenide/indium gallium arsenide (InAlAs/InGaAs) HEMTs with high indium arsenide (InAs) content have been grown metamorphically on GaAs substrates [20]. mHEMTs surpass pHEMTs by utilizing a buffer layer to accommodate greater lattice mismatches between the substrate (e.g., GaAs) and the active layer (e.g., high-indium InGaAs). This adaptation enables the integration of materials with vastly different lattice constants, further boosting electron mobility and high-frequency performance [21]. mHEMTs retain the advantages of pHEMTs while offering better manufacturability, including compatibility with larger wafers, improved reproducibility, and seamless integration into GaAs fabrication processes. Fig. 1.4 illustrates the structures of pHEMT and mHEMT devices.

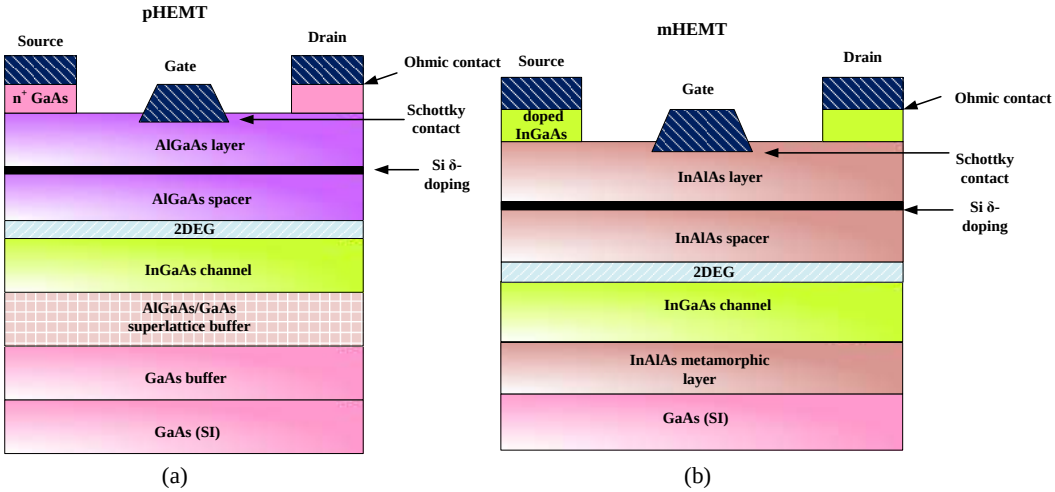


Fig. 1.4. Schematics of (a) pHEMT and (b) mHEMT devices.

Alongside advancements in GaAs HEMT technology, modulation doping and HEMTs were successfully implemented in various other material systems, including AlGaN/GaN [22], InAlAs/InGaAs [23], and aluminium antimonide/indium arsenide (AlSb/InAs) [24]. InAlAs/InGaAs HEMTs on indium phosphide (InP) substrates excel in noise and frequency performance. Fig. 1.5 shows the band-gap energy as a function of lattice constant for the III–V semiconductors. Increasing InAs in InGaAs enhances electron transport and carrier confinement, enabling ultra-scaled devices with outstanding low-noise and high-frequency characteristics. These HEMTs are the first transistors to achieve cut-off frequency (f_T) and maximum frequency (f_{max}) values over 640 GHz simultaneously at just 0.5 V [25], showcasing their low-power potential.

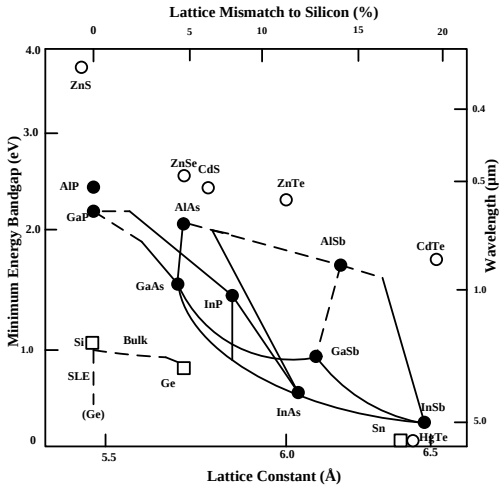


Fig. 1.5. Correlation between lattice constant and minimum band-gap energy in III–V semiconductors.

The transition from GaAs-based HEMTs to those utilising wider bandgap materials, such as GaN, further revolutionised the field. GaN-based HEMTs, with their high V_{br}, thermal stability, and electron saturation velocity, have become the cornerstone of modern high-power and high-frequency electronics. The AlGaN/GaN HEMT has emerged as one of the most impactful device structures in modern technology. The AlGaN/GaN heterostructure, in particular, has demonstrated remarkable performance in power amplifiers, RF transmitters, and energy-efficient switching applications**.** AlGaN/GaN HEMTs are gaining prominence for applications in high-voltage

switching and power conversion. This advantage arises from the remarkable features of GaN-based wide bandgap materials, such as high two-dimensional electron gas (2DEG) density, strong breakdown field, high saturation velocity, superior electron mobility, wide bandgap, and excellent thermal conductivity. AlGaN/GaN HEMTs are prepared for implementation in a wide range of applications, such as cable TV amplifiers, radar systems, satellite communications, and various military systems [8]. Besides, the combination of advanced epitaxial growth techniques, such as metal-organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE), has facilitated precise control over the material properties and HEMT performance characteristics [26]. Recent advancements in HEMT technology target key challenges such as current collapse, gate leakage, self-heating, and thermal management, all of which directly affect device reliability and longevity. Current collapse occurs due to electron trapping in AlGaN, GaN bulk, or unpassivated surface states, which decreases output power at high frequencies. The gate experiences electron tunnelling which results in leakage that degrades both RF and noise performance characteristics. High power densities creates self-heating effects which further accelerates performance degradation. Thermal management plays a crucial role in maintaining temperature stability for extended device operation. Innovations in device architecture, including the use of field plates (FPs) and passivation layers, have significantly improved the performance and robustness of HEMTs [27]. Furthermore, the exploration of novel materials, such as indium aluminium nitride (InAlN) [28-30], indium gallium nitride (InGaN) [31], and indium aluminium gallium nitride (InAlGaN) [32-33] has opened new avenues for enhancing the efficiency and frequency response of HEMTs. As the demand for faster, more efficient, and compact electronic systems continues to grow, HEMTs are poised to play a pivotal role in shaping the future of semiconductor technology, bridging the gap between traditional Si-based devices and next-generation compound semiconductor solutions.

1.2 Motivation

The thesis finds its basis in the growing demand for advanced energy-efficient electronic devices that operate efficiently in modern applications, such as

power electronics, RF communication, and high-speed computing. HEMTs built from III-Nitride materials have established themselves as a promising technology due to their outstanding electron mobility, together with high V_{br} and strong thermal stability. These unique properties of HEMTs make them ideal for use in high-power and high-frequency applications, where traditional Si-based devices face limitations. However, despite their advantages, HEMTs still face several challenges that hinder their widespread adoption and optimal performance. The essential obstacles include designing FP structures that regulate electric fields and boost V_{br}, and selecting passivation materials that minimize surface trap formation to boost device reliability. Investigation of alternative barrier materials to enhance device performance, and designing Normally-Off HEMTs, which serve as crucial components for safe power switching applications. This thesis focuses on studying HEMT design and materials, along with modeling, to overcome these challenges effectively. This research investigates new FP structures and passivation materials alongside multi-barrier materials and Normally-Off HEMT configurations to develop improved next-generation HEMTs that deliver better performance, reliability, and efficiency. Furthermore, the analytical modeling of HEMTs provides a deeper understanding of the underlying physics, enabling better device design and optimization. The primary reason for conducting this research stems from HEMTs capability to revolutionize power electronics and RF systems towards sustainable advanced technological solutions for various industrial applications including renewable energy and telecommunications. The thesis aims to enhance present HEMT technology through innovation while making practical contributions to real-world applications.

1.3 Research Objective

i. To study and analyse different HEMT structures and explore the possibilities of improvement.
ii. Analytical modeling of threshold voltage, drain current, and other parameters for the proposed HEMT structure.
iii. To analyse the critical characteristics of the proposed HEMT structure for high-speed operation.
iv. To study different materials for improving the characteristics of HEMT.

v. To validate the proposed device with technology computer-aided design (TCAD) simulation.

1.4 Organization of the Thesis

The research work presented in the thesis is organized and structured in the form of eight chapters, which are briefly described as follows:

i. **Chapter 1** provides an overview of the research, including the background and significance of HEMTs, the motivation behind the study, the objectives of the thesis, and the organization of the thesis.

ii. **Chapter 2** presents a comprehensive review of the existing literature on HEMTs. It covers the III-Nitride crystal structure, the working principle of HEMTs, the structure of HEMTs (including Normally-On and Normally-Off HEMTs), key challenges in HEMT technology, and state-of-the-art advancements. It also discusses analytical modeling work related to HEMTs.

iii. **Chapter 3** investigate different existing FP structures and explores possibility of novel FP structure in HEMT to further improve the electrical characteristics.

iv. **Chapter 4** investigates the role of passivation layers in HEMTs, multiple passivation layer and their optimization for better device reliability and overall electrical performance.

v. **Chapter 5** examines the use of single and multi-materials barrier in HEMTs, highlighting their effects on DC and RF characteristics.

vi. **Chapter 6** explores the Normally-Off AlGaN/GaN HEMT with novel double-deck FP, analysing various FP configurations and optimized design parameters for enhanced performance.

vii. **Chapter 7** analyses the DC characteristics of AlGaN/GaN HEMTs using an analytical model, incorporating polarization effects, carrier transport mechanisms, and parameter variations in barrier thickness, aluminium mole fraction, and doping density.

viii. **Chapter 8** summarizes the key findings of the thesis, discusses their implications, and outlines potential directions for future research in the field of HEMTs.

CHAPTER 2

Literature Review

2.1 Introduction

For over half a century, Si has been the backbone of the microelectronics industry. Si-based power MOSFETs have dominated the power electronics and power delivery sectors [34]. Various Si-based devices, including BJTs, insulated gate bipolar transistors (IGBTs), vertical FETs, and laterally diffused MOSFETs (LDMOS), have been widely employed in high-power switching circuits, which are essential in power conversion systems [35]. However, despite continuous improvements, the performance of Si-based power devices has plateaued due to material limitations, while the industry's demand for efficiency and cost-effectiveness continues to rise. To address these limitations, researchers and manufacturers have explored alternative materials, particularly wide bandgap semiconductors like GaN and SiC. However, SiC devices cannot form a heterojunction, resulting in lower electron mobility. This limitation restricts their effectiveness in high-frequency applications. GaN stands as a dominant material for RF and power electronics because of its wide bandgap (3.4 eV), alongside high breakdown voltage (V_{br}), and superior carrier saturation velocity [36, 37]. The outstanding material characteristics of GaN, together with its hetero-structure design, enable GaN-based devices to function efficiently throughout a wide frequency range, from a few hundred MHz up to 100 GHz [38]. Among its most impactful applications are GaN HEMTs, which have transformed fields such as high-power electronics, RF communications, and microwave technologies due to their superior performance in terms of V_{br}, efficiency, and operating frequency. GaN HEMTs are based on the concept of a high electron mobility channel formed at the interface of two materials with differing band gaps, such as AlGaN and GaN. This 2DEG at the heterojunction interface provides the basis for the transistor's high electron mobility, enabling high-speed and high-power operation. These devices have evolved from their early theoretical concepts in the late 1980s and early 1990s into commercially

viable solutions for modern power and RF applications. In 1938, Juza successfully synthesised GaN, as well as indium nitride (InN) and copper nitride (Cu_3N) [39]. However, the production of high-quality GaN epitaxial layers was only achieved much later, in the late 1960s. The potential of GaN as a semiconductor material was recognised in the 1970s, with Maruska and Tietjen (1969) laying the groundwork for future GaN-based device research by demonstrating the growth of GaN crystals using hydride vapour phase epitaxy (HVPE) [40]. HVPE is one of the oldest epitaxial growth techniques, developed in the 1950s–1960s for the synthesis of III-V semiconductors such as GaAs. The process involves the reaction of metal chlorides with hydride gases at high temperatures to deposit high-purity crystalline layers [41]. In 1972, J.I. Pankove *et al.* successfully fabricated a GaN-based blue light detector [42]. Although the device demonstrated blue luminescence at room temperature, its power efficiency remained low. Extensive research was conducted in laboratories across the world [43-45] to improve the understanding and growth morphology of GaN for light-emitting diode (LED) development. In 1986, Amano *et al.* achieved a breakthrough by producing high-quality GaN films using metal-organic Vapour Phase Epitaxy (MOVPE) [46]. This work, along with contributions from Akasaki and Nakamura, eventually led to the invention of the blue LED—a milestone that earned them the Nobel Prize [47]. MOVPE, also known as MOCVD, is a key epitaxial growth technique widely used for depositing high-performance semiconductor thin films. MOCVD enables the deposition of crystalline layers by precisely coating atomic layers onto a substrate. The process involves introducing highly purified gases into a cold-wall reactor under controlled thermal and compositional gradients. Under optimal conditions, surface reactions facilitate crystal growth. The gases utilised in this process include metal-organic precursors and hydrides, which undergo pyrolysis. The resulting decomposed atoms then adhere to the substrate surface, forming the desired crystalline structure [48]. In the 1980s, advancements in growth techniques such as MOCVD and MBE revitalised research toward the commercialisation of GaN [49-50]. MBE is an epitaxial growth method performed under ultra-high vacuum (UHV) conditions, offering atomic-scale precision in depositing thin semiconductor layers. Introduced in the late 1960s, this technique [51] employs effusion cells to project molecular or atomic beams onto a heated

substrate, facilitating highly controlled layer-by-layer deposition with precise composition, doping, and sharp interfaces. Unlike MOCVD, MBE operates at lower temperatures, typically around 700°C. However, its growth rate for GaN is relatively slow (0.5–1 μm/hr), making the process more costly compared to MOCVD. Due to its ability to produce high-quality films, MBE is primarily utilised in research settings for proof-of-concept studies [52]. Mimura *et al.* first demonstrated the concept of HEMT in 1980 with AlGaAs/GaAs, and the concept was later applied to GaN-based materials in the 1990s [14]. Khan *et al.* unveiled the first AlGaN/GaN HEMT in 1993 to demonstrate its suitability for high-power applications [24]. The study presented GaN HEMTs as a future technology, which led to Eudyna releasing their first commercial GaN HEMT RF transistor in 2006 [53]. The initial breakthrough led multiple companies to create their own GaN HEMT products, which targeted RF applications. Throughout the 2000s, research focused on improving the performance and durability of these transistors. Since then, GaN microelectronics has seen substantial progress, with the global market for GaN semiconductor devices reaching USD 21.1 billion in 2023 and projected to expand to USD 28.3 billion by 2028, growing at a compound annual growth rate (CAGR) of 6.1% over this period [54].

2.2 III-Nitride Crystal Structure

III-nitrides, along with materials like SiC and diamond, are characterized by their wide bandgaps and short atomic bond lengths [55]. The short bond length signifies a strong bonding energy between atoms, which is greater than that of Si-Si bonds, resulting in materials that are highly stable and chemically inert. GaN can crystallize in wurtzite, zinc-blende, or rock-salt structures, with the wurtzite structure being the most prevalent due to its easier growth process and higher stability. The wurtzite structure is characterized by lattice parameters a (hexagon side length) and c (unit cell height). Additionally, the u-parameter is given by the ratio $u = b/c$, where b represents the length of the bond [56]. Zinc-blende differs from wurtzite primarily in their second-nearest-neighbour bond angles. In wurtzite, atoms in layers one and three align vertically (ABABAB stacking along ⟨0001⟩), creating Mirror symmetry along the c-axis, with the third layer rotated 60° in zinc-blende, resulting

in ABCABC stacking along ⟨111⟩. Here, A, B, and C represent anion-cation bond positions (Fig. 2.1). At room temperature, wurtzite GaN has lattice constants of a = 3.189 Å and c = 5.185 Å, as widely reported [40]. The wurtzite structure displays polarity along the c-axis, resulting in the creation of two unique surfaces: the Ga-face (0001) and the N-face (000-1).

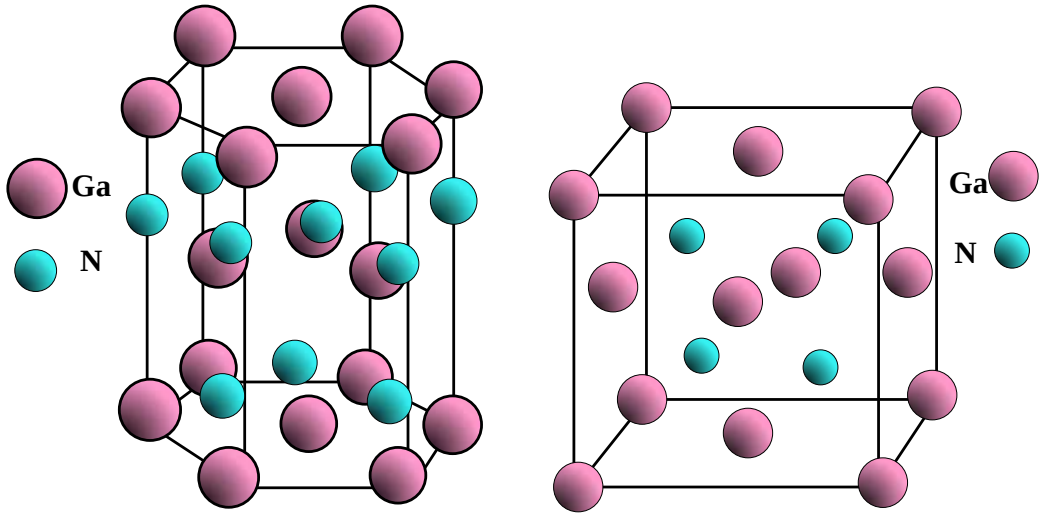


Fig. 2.1. (a) Wurtzite and (b) zinc-blende GaN crystal structures.

This polarity strongly influences GaN growth, etching, and electronic properties [57], originating from the non-centrosymmetric wurtzite lattice, where unidirectional Ga-N bonds along the c-axis generate a built-in **spontaneous polarisation (P_{SP})** field. The polarity affects various aspects of GaN, including epitaxial growth, surface reactivity, and electronic properties. For instance, the Ga-face is typically smoother and more chemically stable, making it preferable for device fabrication, while the N-face is more reactive and prone to defects [58]. Additionally, the polarisation fields in GaN-based heterostructures, such as AlGaN/GaN, induce high sheet carrier concentrations (n_s) at interfaces, which are crucial for HEMTs [8]. Understanding and controlling GaN polarity is therefore essential for optimizing the performance of GaN-based devices. In general, Ga-facing crystals are more durable compared to N-facing ones, which are highly sensitive. The material on the N-polar face can be readily etched with developer solutions, while etching the Ga-polar face demands high-energy plasma sources. Although most research in electronics has concentrated

on Ga-polar materials, N-polar devices have also been investigated and have shown encouraging performance traits [59]. These N-facing materials hold potential for sensory applications, the development of enhancement-mode transistors, and highly scaled transistors.

A fundamental aspect of GaN HEMTs is the role of polarisation effects, which are intrinsic to III-nitride materials and play a critical role in the creation and operation of the 2DEG at the heterojunction interface. These polarisation effects, arising from both spontaneous and piezoelectric mechanisms, are central to the device's performance and have significant implications for its design, operation, and reliability. An unstrained GaN crystal's inherent polarisation field is known as P_{SP}. Due to the crystal's lack of symmetry, the bond formed between two atoms is not strictly covalent, which is why this polarisation field arises. Surface charges of opposite polarity build up across both ends of the crystal as a result of the electron being displaced towards one of the atoms in the crystal link [60]. Reported P_{SP} values are -0.029, -0.032, -0.074, and -0.081 C/m² for GaN, InN, zinc oxide (ZnO**)**, and aluminum nitride (AlN), respectively [61]. For AlGaN alloys, P_{SP} scales linearly with Al composition (n), interpolated between GaN and AlN values. Additionally, when heterostructures such as AlGaN/GaN are grown epitaxially, material lattice mismatch induces mechanical strain, leading to **piezoelectric polarisation (**P_{PZ}**)**. AlGaN on GaN undergoes tensile strain since its lattice constant is smaller. Fig. 2.2 depicts the three possible cases of polarisation-induced charges at the heterojunction in Ga-polar AlGaN/GaN structures. In Fig. 2.2(a), a thick AlGaN layer grown on a relaxed GaN buffer results in both layers remaining relaxed, leaving only P_{SP} vectors pointing toward the substrate. Since the P_{SP} AlGaN exceeds that of GaN, a net positive interfacial charge forms at the heterojunction. Fig. 2.2(b) shows the case where a thin AlGaN layer is deposited on GaN, introducing tensile strain that generates both P_{SP} and P_{PZ}. Here, the aligned polarisation vectors create a stronger positive charge at the interface compared to Fig. 2.2(a), as the piezoelectric component enhances the total polarisation. Finally, Fig. 2.2(c) illustrates the scenario where a thin GaN layer is grown on a relaxed AlGaN buffer, subjecting the GaN layer to compressive strain and altering the polarisation behaviour accordingly.

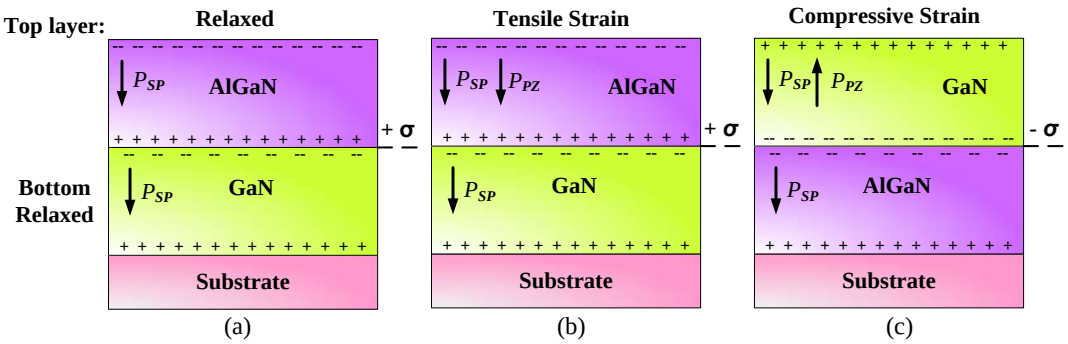


Fig. 2.2. Polarisation vectors (P_{SP} and P_{PZ}) and interface charges in Ga-polar AlGaN/GaN heterostructures under varying growth conditions of the top layer: (a) relaxed AlGaN, (b) tensile-strained AlGaN, and (c) compressively strained GaN, with the bottom layer remaining relaxed in all cases.

This will result in anti-parallel P_{SP} and P_{PZ} vectors, creating a net negative interfacial charge. In tensile-stressed Ga-polar AlGaN/GaN heterojunctions (Fig. 2.2(b)), a strong positive polarisation charge ($+\sigma$) forms at the interface. Free electrons from surface donor states [61] compensate this charge. High densities of these free electrons form a conductive restricted layer known as a 2DEG. Without doping, polarisation-induced 2DEG can reach concentrations over 10^{13} cm^{-2}, leading to high electron mobility >1000 cm^2 $V^{-1}S^{-1}$ because of decreased impurity scattering [62], which can be used to create high-frequency devices. Wurtzite GaN heterostructures leverage polarisation effects, giving them a key advantage over AlGaAs/GaAs systems where the 2DEG relies on doping-induced carrier injection. The strain in the material, both in amplitude and orientation, is correlated with the P_{PZ}. The polarisation increases with strain; compressive strain produces a polarisation that is opposite to that of tensile strain.

According to the approach outlined by Rashmi *et al.* [63], the P_{PZ} can be expressed as:

$$P_{PZ}(AlGaN) = 2\left(\frac{a(0)-a(n)}{a(n)}\right)\left(e_{31}(n) - e_{33}(n)\frac{c_{13}(n)}{c_{33}(n)}\right) \tag{2.1}$$

The parameters c_{13} and c_{33} represent the elastic constants, e_{31}, and e_{33} denote the piezoelectric coefficients. Additionally, $a(n)$ corresponds to the lattice constant of the

strained layer, while *a(0)* denotes the hexagonal edge of the relaxed HCP cell. Owing to its substantial thickness, generally around 1–3 μm, the GaN buffer layer achieves complete relaxation. As a result, there are no P_{PZ} present. Since the P_{SP} and P_{PZ} constants for AlGaN are greater [64], AlGaN, whether strained or unstrained, has larger polarisation than GaN.

Overall net polarisation charge σ is given as [63]

$$|\sigma(n)| = |P_{SP}\ (AlGaN) - P_{SP}\ (GaN) - P_{PZ}\ (AlGaN)| \quad (2.2)$$

$P_{SP}\,(AlGaN)$ and $P_{SP}\,(GaN)$ can be expressed as [63, 65-66],

$$P_{SP}\ (AlGaN) = -0.052n - 0.029 \quad (2.3)$$

$$P_{SP}\ (GaN) = -0.029 \quad (2.4)$$

2.3 Working Principle of HEMT

HEMT is a device that consists of a two-layer heterostructure, where a material with a wide bandgap is grown on top of a material with a narrow bandgap. The heterojunction induces strain, causing P_{PZ} that generates a high-density 2DEG. Due to the differing lattice constants of AlGaN and GaN, depositing a thin layer of AlGaN on GaN introduces mechanical strain within the AlGaN layer, as illustrated in Fig. 2.3. This mechanical strain arises from the material's elastic properties. The alignment of AlGaN with GaN produces biaxial strain, affecting both the x and y directions in the AlGaN layer. This strain increases AlGaN's lattice constant, enabling atomic alignment with GaN and forming the heterojunction [67].

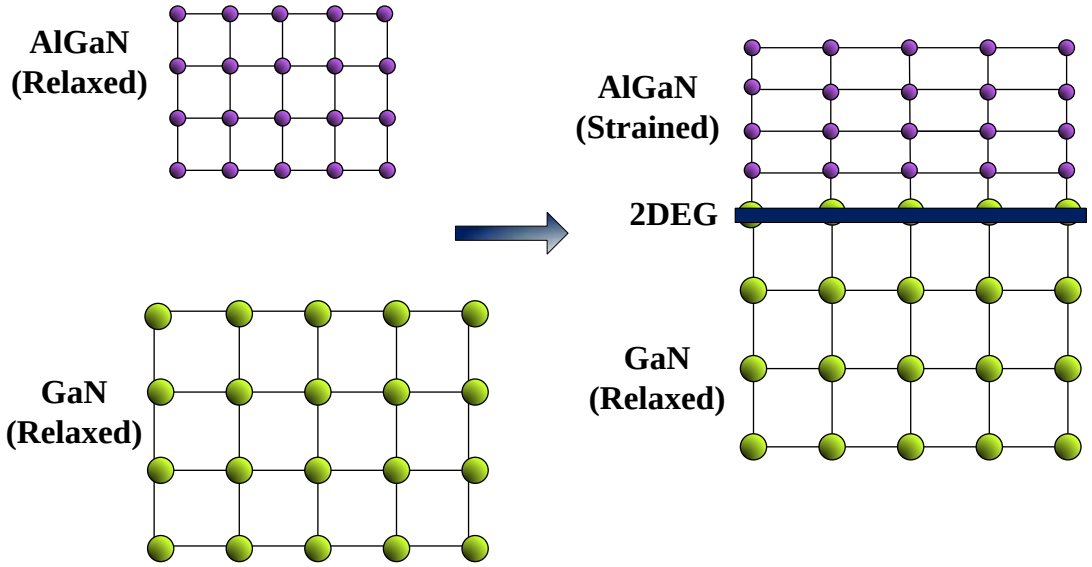


Fig. 2.3. Demonstration of strain development in AlGaN when creating 2DEG on GaN.

The creation of a quantum well at the AlGaN/GaN interface is driven by the discontinuity in polarisation, specifically the P_{PZ} and P_{SP} [68]. Fig. 2.4(a). shows the energy band diagram of the HEMT device prior to heterojunction formation. Band bending, which is essential for creating a 2DEG, occurs at the heterojunction interface when the wide and narrow bandgap materials come into contact (Fig. 2.4(b)). At the GaN-AlGaN heterojunction, electrons from donor impurities in the wider bandgap material transfer into the lower-energy GaN conduction band. These electrons become confined by the potential barrier formed at the heterointerface**.** Variation in three key parameters such as work function (φ), electron affinity (χ), and bandgap (E_G), facilitates electron transfer between the materials. This charge redistribution persists until the system reaches equilibrium through fermi level alignment. Fig. 2.4(c) shows the quantum potential well at the heterojunction, which confines free electrons. Electrons within the quantum well are spatially separated from their parent donor ions, significantly enhancing carrier mobility. This confinement gives rise to 2DEG, which serves as the fundamental operating principle of HEMTs. The energy barrier at the heterojunction is characterized by the conduction band offset (ΔE_c), while the gate contact's Schottky barrier height is

denoted by $\emptyset_b$. Additionally, ΔE_F represents the Fermi level offset from the GaN conduction band edge, and q corresponds to the elementary charge (1.6×10^{-19} C). The 2DEG formed at the heterointerface can be controlled by applying a gate voltage (V_G), which bends the energy bands. Strong polarisation effects in III-nitrides (with wurtzite structure) generate large electric fields, increasing carrier concentration and enhancing 2DEG confinement. As a result, AlGaN/GaN HEMTs can achieve high 2DEG n_s of up to 10^{13} atoms/cm² without intentional doping [69]. Doping can reduce electron mobility due to scattering, but placing the current-carrying region below the AlGaN barrier minimizes surface scattering in these devices. The 2DEG in standard AlGaN/GaN HEMT with 15% Al content demonstrates a n_s of 6×10^{12} cm^{-2}, which can be boosted to 2×10^{13} cm^{-2} by increasing the Al content to 31%. For a 100% Al binary AlN barrier, the n_s can reach a maximum of 6×10^{13} cm^{-2} [70]. Consequently, devices utilizing an AlN barrier can deliver up to three times the power output of conventional AlGaN/GaN HEMTs. The 2DEG serves as a high-current-density channel, with electron concentration influenced by conduction band offset, barrier layer doping, and polarisation effects. Operational issues in AlGaN/GaN HEMTs, such as current collapse, I-V "kinks", and instability, arise when electrons become trapped in AlGaN, GaN bulk, or unpassivated surface states.

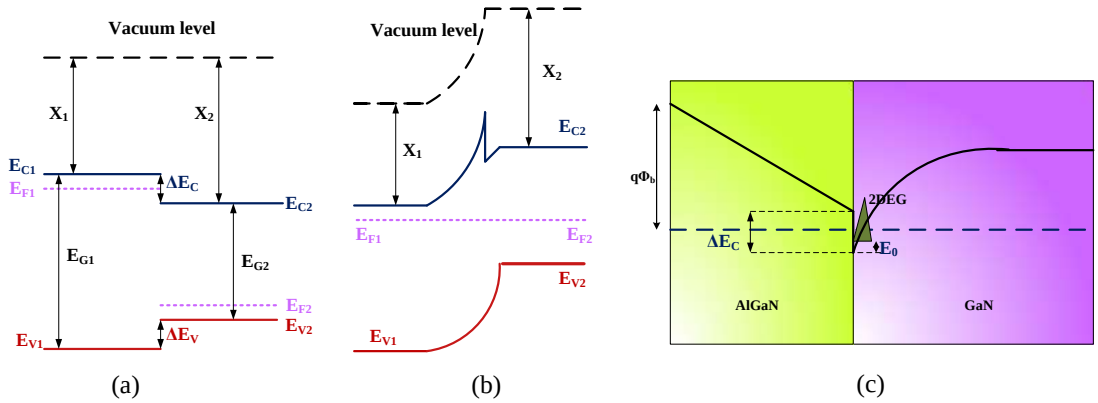


Fig. 2.4. Energy band diagram of an AlGaN/GaN HEMT, showing: (a) The initial band gap discontinuity prior to heterojunction formation, (b) subsequent band bending resulting from heterojunction creation, and (c) the eventual formation of a 2DEG at the interface.

2.4 HEMT Structure

Fig. 2.5 presents a schematic cross-section of a conventional AlGaN/GaN HEMT. The GaN channel layer, with a bandgap of 3.4 eV, has a lower bandgap energy compared to the AlGaN barrier layer (4 eV for $Al_{0.25}Ga_{0.75}N$). This bandgap difference facilitates the formation of a 2DEG at the heterointerface. To achieve strain relaxation, a thick GaN buffer layer is typically employed. Additionally, a high-resistivity buffer layer is essential to improve electron confinement and minimize vertical leakage currents. In GaN HEMT heterostructures, carbon (C) and iron (Fe) are the most commonly used acceptor dopants for the buffer layer [71]. The $Al_nGa_{1-n}N$ barrier layer, typically 20-30 nm thick, has an *n* value of 20-30%. In a HEMT structure, the AlGaN barrier layer is typically deposited above the GaN channel layer and serves mainly to control both the mobility and electron density in the 2DEG channel. Because AlGaN has a wider bandgap than GaN, it significantly influences the 2DEG carrier concentration, which increases with the bandgap difference. By adjusting the composition of Al in the AlGaN layer, key properties such as E_G and polarisation effects can be tuned. For example, higher Al content raises the potential barrier, reducing gate leakage current but often at the expense of lower electron mobility. The most commonly used barrier layers are AlGaN [72] and AlN [73]. AlN, offering high 2DEG density (~2×10^{13} cm^{-2}) with just 3 nm thickness [74], faces challenges like high contact resistance, leakage currents, and surface sensitivity, limiting its use [75].

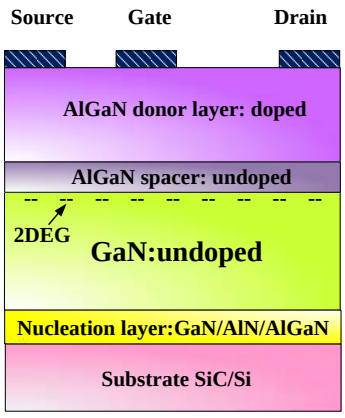


Fig. 2.5. A cross-sectional view of a doped AlGaN/GaN HEMT, showcasing the 2DEG formed at the AlGaN/GaN heterojunction.

The AlGaN spacer layer separates the doped AlGaN barrier from the channel (heterojunction), reducing impurity scattering and ensuring high electron mobility [76]. Increasing its thickness distances dopants from the channel, minimizing scattering and improving electron mobility. The AlGaN layer is n-doped (10^{17}–10^{19} cm^{-3}) to supply electrons for the 2DEG. Higher doping boosts channel electron density but reduces mobility and increases leakage current. However, AlGaN/GaN HEMTs often don't require doping, as polarisation charges alone can generate a 2DEG density of 10^{13} atoms/cm^2 at the heterointerface [77]. Doping contributes less than 10% to 2DEG formation due to GaN's strong polarisation effects. Doped AlGaN/GaN HEMTs show better DC performance than un-doped ones, but excessive doping levels in the AlGaN barrier layer led to increased scattering, potentially degrading RF performance [78]. The thickness of the barrier layer (d_{AlGaN}) and n also critically affect RF small-signal gain. GaN-based HEMTs are typically grown on thick substrates like sapphire, silicon, or silicon carbide, as native GaN substrates are costly and hard to produce. An intermediate/nucleation layer is often added to mitigate lattice and thermal mismatch between GaN epilayers and foreign substrate. For GaN growth on sapphire, the two-step method can produce crack-free epitaxial films [45]. This process begins with the deposition of a thin AlN nucleation layer at 500–600°C, followed by high-temperature GaN growth at approximately 1000°C. The higher temperature forms polycrystalline nano-islands in the AlN layer, serving as the nucleation base for GaN growth. When using SiC substrates, a thin AlN interlayer is typically introduced to reduce lattice mismatch and mitigate stress in the GaN buffer layer. For GaN growth on silicon substrates, an AlN nucleation layer is often used to block Ga diffusion, usually followed by GaN/AlN superlattices to introduce compressive stress and balance the tensile strain in nitrides grown on silicon. The Schottky barrier height is increased, and leakage current is reduced by introducing a thin GaN cap layer on top of the AlGaN barrier [79]. This GaN layer also helps prevent AlGaN surface oxidation and improves electrical contact formation [80]. AlGaN/GaN HEMTs typically feature three terminals: a Schottky gate contact and Ohmic source and drain contacts. These devices utilize Ohmic and Schottky contacts for biasing and current output. In standard configurations, the source and drain employ Ohmic contacts, which are linear and non-rectifying, to

facilitate current flow. The gate, on the other hand, uses a Schottky contact, which is non-linear and rectifying, to control the device operation.

At low drain-source voltages (V_D), the drain current (I_D) is nearly linear. As a depletion-mode device, the AlGaN/GaN HEMT requires a strong negative V_G to turn off, achieved via the Schottky gate. A negative V_G depletes electrons in the 2DEG channel, increasing resistance. When the V_G reaches the threshold voltage or pinch-off voltage (V_{th}), the channel electrons deplete, closing the channel and reducing I_D to zero, known as device pinch-off. The Schottky gate in GaN HEMTs serves two key roles: (i) depleting the channel and (ii) suppressing unwanted leakage currents between source and drain terminals (like in MESFETs). Ohmic contacts for source/drain electrodes commonly employ Ti/Al or Ti/Au metallization stacks, whereas the Schottky gate typically utilizes Ni/Au or Pt/Au bilayers [81].

2.4.1 Normally-On HEMT

GaN HEMTs have proven crucial for high-power and high-frequency applications owing to their remarkable material properties, which feature a wide bandgap, high V_{br}, and exceptional electron mobility. The structural design of GaN HEMTs plays a critical role in determining their performance, reliability, and application suitability. The most common classification of GaN HEMTs is based on their operational mode, namely Normally-On (depletion-mode) and Normally-Off (enhancement-mode) devices. Normally-On HEMTs are characterized by the presence of a conductive channel in the absence of V_G, making them safer for power switching applications. A negative V_G is required to deplete the channel and switch the device off. While offering high-speed performance, their Normally-On nature can pose challenges in power applications where a default-off state is preferred for safety reasons [82]. To mitigate high electric fields between the drain and gate under elevated V_D, the gate is typically placed nearer to the source. This layout improves the HEMT's lateral V_{br} and reduces self-heating effects. Fig. 2.6(a) and (b) illustrate the cross-sectional structure of an AlGaN/GaN HEMT, demonstrating its On-state and Off-state operation. Owing to polarisation-induced effects, the GaN HEMT functions as a Normally-On (depletion-mode) device [83]. Under negative gate bias,

the 2DEG channel depletes proportionally with applied voltage. The V_{th} corresponds to the bias required to completely deplete the channel, cutting off current flow and switching the device off. Conversely, increasing the gate bias above V_{th} enhances the 2DEG electron density, allowing current conduction between source and drain under an applied bias. For Schottky gates, a critical threshold of around +1 V exists—beyond this point, the gate starts conducting and loses control over 2DEG concentration. The devices studied in this thesis are Normally-On (depletion-mode), meaning a 2DEG forms even at zero V_G. V_G controls 2DEG density, switching between On ($V_G > V_{th}$) and Off ($V_G < V_{th}$) states. In Off-state ($V_G < V_{th}$), the 2DEG depletes, blocking the current flow.

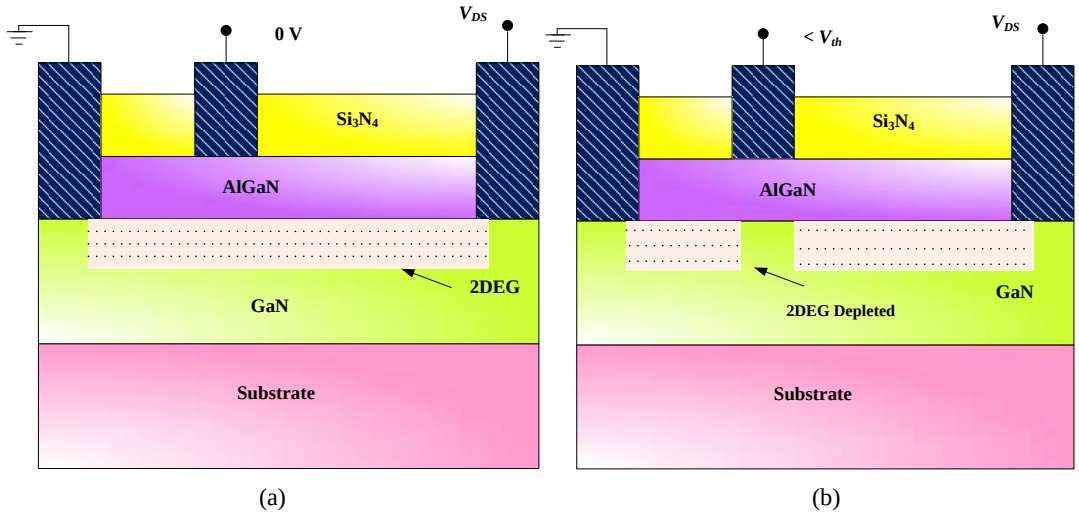


Fig. 2.6. Illustration of an AlGaN/GaN HEMT operation principle and biasing (a) On-state and (b) Off-state.

Optimizing GaN-based RF and power devices requires considerations beyond just mitigating self-heating effects and current collapse phenomena. Power GaN devices face challenges like their inherent Normally-On behaviour, which is preferred in RF but problematic for power applications. Achieving Normally-Off (enhancement-mode) operation is crucial for power devices, offering safe operation by cutting off high voltage without gate activation.

2.4.2 Normally-Off HEMT

Normally-Off (enhancement-mode) behaviour improves performance by cutting leakage current, simplifying circuits, boosting stability, and enhancing efficiency. Enhancement-mode devices don't need extra power to turn off, which is its key advantages. In a Normally-Off GaN HEMT, zero V_G creates a depletion region via a p-type layer in the AlGaN barrier. A positive V_G forms a conductive channel, enabling current flow; removing it depletes the channel, turning the device off. Methods to achieve enhancement-mode include p-type layers above GaN HEMTs [84-85], deep gate recessing [86], gate oxide modifications [87-88], and plasma-treated buried layers in AlGaN layer HEMTs [89-90]. A p-doped GaN layer is incorporated under the gate [91], as depicted in Fig. 2.7(a) to achieve enhancement-mode operation in AlGaN/GaN HEMTs. This setup, known as a gate-injection transistor (GIT), uses the p-doped GaN layer to raise the potential barrier, creating a diode-like depletion layer without V_G. By thinning the AlGaN layer, the 2DEG charges under the gate can be fully depleted, enabling Normally-Off operation. To further improve device performance, **gate-recessed HEMTs** (Fig. 2.7(b)) have been introduced, where the gate region is etched to reduce the distance between the gate and the channel, resulting in enhanced gate control and reduced leakage current [92]. Similarly, metal-insulator-semiconductor HEMT (MISHEMT) incorporate an insulating layer between the gate and the AlGaN layer, significantly reducing gate leakage and improving device reliability, particularly in power electronics and RF amplifiers [87-88]. The choice of insulator material and its interface quality with the semiconductor are critical factors influencing device performance. Recent studies have explored the use of ultra-wide bandgap materials, such as β-Ga_2O_3 substrates, to further improve the performance of MISHEMTs in high-power and high-frequency applications [94]. R. Chu *et al.* from HRL Laboratories [90] also utilized halide-based plasma treatment to achieve enhancement-mode operation**.** The fluorine plasma treatment generates trapped negative charges, depleting the 2DEG under the gate and resulting in a positive V_{th}. There is significant potential for advancing both RF GaN and power GaN devices. While issues like self-heating and current collapse are well-known, the Normally-On

behaviour of power devices and the pursuit of Normally-Off operation, particularly in power applications, remain critical challenges. Various techniques, from fluoride-based methods to innovative gate structures, have been pursued to enhance device performance and efficiency. These diverse GaN HEMT structures cater to a wide range of applications, from RF and power electronics to high-speed digital systems, each offering unique advantages in terms of performance, reliability, and efficiency. The choice of structure depends on the specific requirements of the application, such as power handling, frequency range, and thermal management.

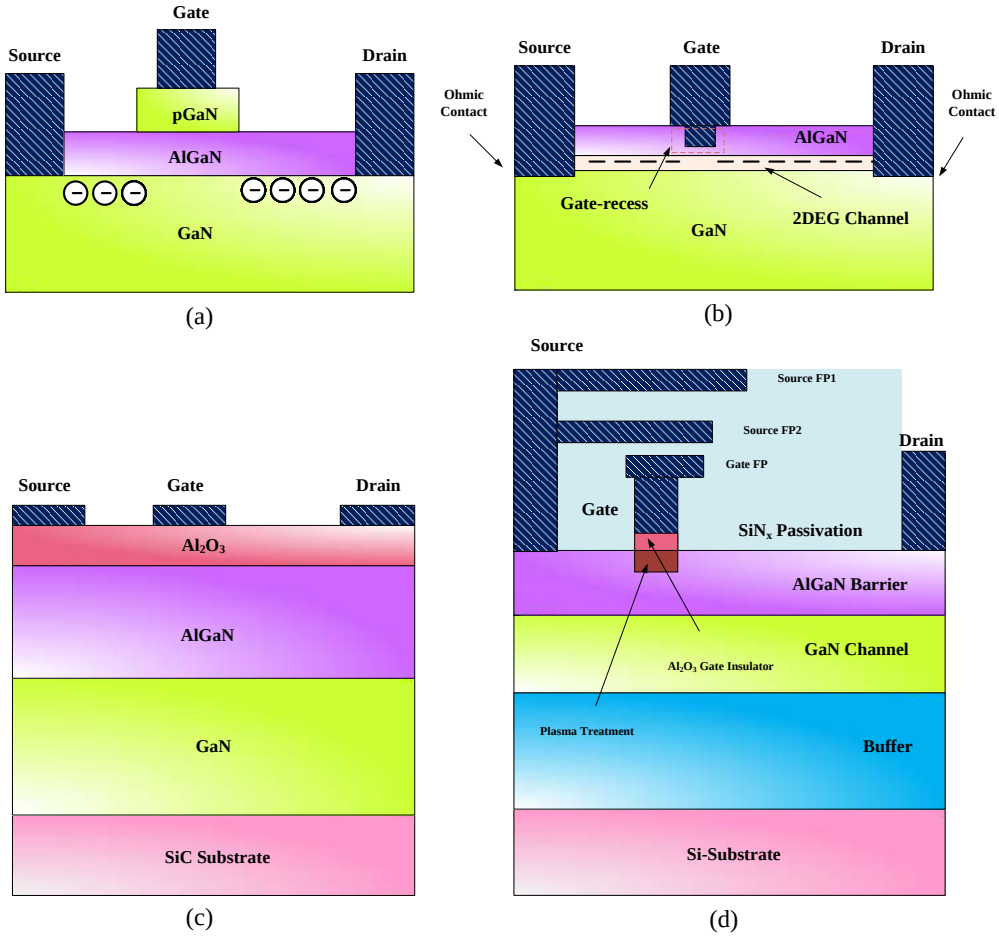


Fig. 2.7. Cross sectional structure of (a) GaN-GIT [91], (b) recessed-gate structure [93], (c) MIS-HEMT [87], and (d) plasma implanted gate [90].

2.5 Key Challenges

GaN HEMTs are promising for high-frequency, high-power applications due to their excellent material properties. However, challenges such as self-heating,

current collapse, gate and drain lag, peak electric field distribution, gate leakage, gate-edge degradation and inverse piezoelectric effect still limit their reliability and broader adoption.

2.5.1 Self-heating

The self-heating effect in GaN-based HEMTs emerges as a vital problem because of their high-power density and intense lateral electric fields inside the device. A significant electric field forms at the gate's edge on the drain side when high drain bias is applied thus causing localized heating in the lattice structure. The self-heating effect occurs because of this phenomenon which raises channel temperatures thus decreasing I_D and damaging device performance over time. High temperatures beyond a certain threshold will permanently damage [95] the device and shorten its operational lifespan [96]. Self-heating in GaN-HEMTs creates several performance challenges, such as gate degradation along with reduced electron mobility and current reduction, and potential damage to the chip-package interface [97]. The main cause of this problem arises from multi-layer device structures with poor thermal conductivity, which restrict heat flow from the active region to the substrate [98]. The design phase must include proper thermal management solutions to enhance device reliability. Various material and structural solutions have been studied to reduce self-heating, with the most common approach being the substitution of low-thermal-conductivity substrates like Si or sapphire with high-thermal-conductivity SiC or diamond [99], which enable improved heat dissipation [100]. Diamond substrates, with thermal conductivities reaching up to 2000 W/m·K [101], significantly improve heat dissipation. Another approach involves integrating Cu-filled trenches or vias in SiC substrates [102], which enhances thermal regulation. Modifying the AlGaN barrier and the use of a back-barrier layer help reduce thermal resistance [103]. The development of micro-trench structures together with advanced engineered substrates, including Qromis Substrate Technology (QST) [104], serves to enhance thermal management and helps in reducing self-heating. These strategies collectively contribute to reducing self-heating, thereby improving the reliability and performance of GaN-based HEMTs.

2.5.2 Current Collapse

Current collapse is a significant parasitic effect observed in GaN HEMTs, leading to a notable reduction in output power at high frequencies. This phenomenon, also referred to as DC/RF dispersion [105], current slump [106], or current compression [107]. It reduces the dynamic saturation drain current (I_{dss}) relative to DC values, leading to higher access resistance. Furthermore, current collapse contributes to increased high-frequency distortion and diminished efficiency. The primary cause of current collapse is the presence of traps within the device, which can be located in the buffer layer, barrier layer, or at the surface. Surface traps are particularly responsible for the majority of the observed dispersion effects, while bulk traps in the buffer region also contribute to the phenomenon. The mechanism behind current collapse is often explained using the virtual gate model [103]. When a negative gate bias is applied below the V_{th}, a high electric field is induced at the drain-side edge of the gate. This results in electron leakage between the gate and drain, filling ionized donor states near the gate terminal. The resulting negative surface potential depletes the channel under the drain access region, creating a virtual gate that controls the channel current. The slow response of this virtual gate to applied voltages causes a delayed recovery of the I_D, leading to current collapse. To address current collapse, various strategies have been suggested. Surface passivation [108] is an effective method to minimize current collapse through the establishment of stable dielectric–semiconductor interfaces, which prevent gate-leaked electrons from occupying ionized surface traps [109]–110]. FPs serve as an alternate solution by distributing the electric field more uniformly across the drain region, lowering field peaks near the gate edge and reducing trap-related effects [111]–113]. Additional strategies include light illumination [114]–115] and adding a GaN cap layer [116] to further suppress trapping phenomena.

2.5.3 Gate and Drain Lag

Gate lag refers to the delayed I_D response after abrupt V_G shifts. Electron trapping by ionized surface state donors on the ungated device area serves as the primary reason for this phenomenon. When a strong reverse V_G is applied, leaked

electrons from the gate-drain region get trapped, which expands the channel depletion region and reduces the I_D. A second cause is charge trapping beneath the gate—mainly in the AlGaN or GaN layers—which shifts the V_{th} positively [117]. It has been observed that AlGaN/GaN HEMTs with ion tin oxide (ITO) gates exhibit gate-lag effects due to the presence of traps under the gate region. The higher leakage current in these devices supplies additional electrons that charge the trap states under the gate when a reverse-biased V_G is applied. To mitigate gate lag, employing a passivation layer and implementing a FP at the gate can significantly reduce its impact [77].

Drain lag is a transient effect where the I_D responds slowly to sudden changes in V_D, especially under strong negative V_G. It arises from the combined influence of gate and drain voltages. A high reverse gate bias can cause electron tunnelling to the surface, affecting electron availability in the 2DEG channel. When the V_D is pulsed high, the intensified electric field can excite channel electrons, causing some to escape and become trapped in the buffer, which reduces the I_D. Techniques like surface passivation, FPs, and gate dielectrics [118]–[119] help mitigate gate and drain lag, enhancing switching speed and device performance.

2.5.4 Gate Leakage

Gate leakage in GaN HEMTs poses a major challenge to performance and reliability, as electron tunnelling through the gate leads to unwanted current and degrades RF and noise characteristics [120]. Since a Schottky gate controls the 2DEG, a strong negative bias to turn off the device makes leakage a critical efficiency factor. Several studies have explored its dependence on temperature and bias conditions [121]–[122]. Studies show that Poole-Frenkel (PF) emission is the dominant mechanism behind increased gate leakage at elevated temperatures, where electric fields assist in releasing trapped electrons through defect paths in the AlGaN barrier. As V_G and temperature rise, the barrier height for emission lowers, boosting leakage current. At low temperatures, however, Fowler-Nordheim (FN) tunnelling becomes significant, with high reverse bias reducing barrier thickness and enabling electron tunnelling. FN tunnelling occurs when high electric fields enable electrons to pass through a triangular potential barrier, largely independent of temperature. In

contrast to PF emission, FN tunnelling is electric field-driven. Gate leakage is also influenced by thermionic emission and trap-assisted tunnelling, both of which vary with bias conditions [123]. To mitigate gate leakage in GaN HEMTs, strategies such as using FPs to reduce electric field concentration at the gate edge, and employing high-k dielectrics to suppress leakage, have proven effective [124]. Gate structure modifications—such as slanted tri-gates or gamma gates—also help distribute electric fields more evenly, further enhancing reliability and performance [125].

2.5.5 Inverse Piezoelectric Effect

The inverse piezoelectric effect in AlGaN/GaN HEMTs, triggered by high electric fields, induces mechanical strain that can create lattice defects and cracks in the AlGaN barrier, degrading electrical performance [126]. While lower temperatures lessen permanent damage, they may still reduce I_D and transconductance (g_m) [127]. Additionally, the mechanical stress increases elastic energy in the AlGaN layer, forming electrically active defects that raise gate leakage and electron trapping, compromising device stability [128]. A FP structure effectively mitigates the inverse piezoelectric effect by reducing peak electric fields and suppressing electron trapping at the AlGaN surface. This lowers tensile strain in the barrier layer, minimizing defect formation, gate capacitance degradation, and current collapse. Gate FPs also stabilize the electric field, improving V_{th} stability and reducing gate leakage, thereby enhancing device reliability under high-voltage stress.

2.5.6 Gate-Edge Degradation

Gate edge degradation [129] in GaN HEMTs occurs when high reverse gate bias increases gate leakage, worsens current collapse, and can raise parasitic resistance while reducing DC saturated current [130]. The strong electric field at the gate-drain junction induces tensile strain and elastic energy via the inverse piezoelectric effect [131]. When this strain exceeds a threshold, the AlGaN barrier forms crystallographic defects that facilitate trap-assisted tunnelling, further increasing leakage and trapping effects. A simple way to verify this failure mechanism is through a reverse-bias step-stress test, where the negative V_G is gradually increased while the device remains off, with the drain grounded and the

source either grounded or floating. Gate-edge degradation can be analysed using techniques such as destructive physical analysis (DPA), transmission electron microscopy (TEM), and electroluminescence microscopy [131]. Gate edge degradation in GaN HEMTs can be mitigated through several strategies. Optimizing the gate metallization profile helps control electric field distribution, a key factor in degradation [132]. Structures like FPs or T-shaped gates further manage the field intensity, minimizing defect generation. Additionally, high-quality passivation layers reduce surface states and trapping, enhancing device stability [108]– [109]. Maintaining the reverse gate bias below critical thresholds is key to preventing degradation. Effective thermal management [133]– [134] also plays a vital role, as elevated temperatures accelerate failure mechanisms. These combined approaches can help mitigate gate edge degradation and enhance the overall reliability of GaN HEMTs.

2.5.7 Peak Electric Field Distribution

In GaN HEMTs, high drain bias generates strong electric fields at the gate's drain-side edge [135], leading to charge trapping at the passivation and the III-nitride semiconductor interface, virtual gating, and current collapse [136]. As gate-to-drain spacing shrinks with scaling, the intensified fields further increase leakage and accelerate degradation, impacting performance. To mitigate peak electric field effects, various structural and design modifications have been proposed. FPs are a widely used solution, as they effectively distribute the electric field and suppress localized field peaks, thereby reducing current collapse and improving V_{br} [137]. Another effective approach is the implementation of notch [138] structures in the AlGaN barrier layer, which helps modulate the 2DEG concentration, leading to a more uniform electric field distribution. The use of a slanted tri-gate [139] or a gamma gate has also been shown to enhance field distribution, further minimizing electric field-induced performance degradation. These combined strategies ensure better electric field management, improving device reliability and overall efficiency.

2.6 State-of-the-Art Technology of HEMT

2.6.1 Field Plate

Field Plate (FP) structures are essential in the design and optimization of GaN HEMTs, significantly enhancing performance, reliability, and thermal management. The FP, a conductive electrode placed over the gate-drain or gate-source region, redistributes the electric field within the device. This redistribution reduces high electric field peaks near the gate edge, which can cause device degradation, current collapse, and lower V_{br} [111]. By lowering the peak electric field in the gate-drain region, FPs improve device reliability and operational lifetime, especially in high-voltage applications where electric field crowding can lead to premature failure [140]. FPs also address current collapse, a phenomenon where high-voltage stress traps electrons in surface states or buffer layers, reducing output current [141]. By smoothing the electric field, FPs minimize trapping effects, ensuring more stable and reliable operation [142]. Additionally, FPs increase the V_{br} in GaN HEMTs, which can be optimized by adjusting FP length (L_{FP}) and insulator thickness [143]. They also reduce gate leakage and enhance device linearity, stability, reliability, and efficiency. However, the FP structure introduces additional drain-to-gate feedback capacitance, which may adversely affect RF performance, particularly at high frequencies. FP technology is widely used in HEMTs to enhance performance. A single FP, such as given by Y. Ando *et al.*, significantly improves the gate-drain V_{br}, achieving a maximum of 160 V with an L_{FP} of 1 μm. The FP also effectively suppresses current collapse, a common issue in GaN-based devices, resulting in a maximum I_D of 750 mA/mm with negligible collapse [143]. AlGaN/GaN HEMT with a dual FP structure comprises a first FP integrated into the gate to suppress current collapse and improve V_{br}, and a second FP connected to the source, which reduces feedback capacitance. This dual-FP approach significantly increases the V_{br} from 125 V to 250 V, while also improving gain, linearity, and stability [144]. To improve the frequency response, an inner-FP (IFP) structure has been proposed [145], where the FP extends from the gate head to mitigate RF degradation while maintaining high V_{br}. The IFP significantly improves frequency response, with minimal voltage loss, making it ideal for high-power, high-frequency applications.

IFP enhances both V_{br} and RF characteristics, addressing the trade-off between these parameters caused by traditional FP structures. By optimizing the FP and IFP designs, high-power and high-frequency operation can be achieved, making the IFP HEMT a promising candidate for advanced RF and power applications. In multi-finger FP [146], both gate-connected and source-connected FPs are optimized, which effectively redistributes the electric field in the channel, reducing peak electric field intensity and increasing V_{br} by more than three times (from 40 V to 150 V). The multi-finger FP structure also minimizes current collapse and improves device reliability, enabling higher drain-to-source voltage operation up to 50 V. Suzuki *et al.* [147] also proposed an additional three-dimensional field plate structure (3DFP). By adjusting the spacing between the grooves, this design achieves near-collapse-free operation while maintaining the I_D. The incorporation of uniformly distributed multiple grooves enhances the effective FP area. Augustine Fletcher *et al.* [137] employed a discrete FP without a lateral plate, achieving a 330 V V_{br} (vs. 298 V conventionally) and reducing the gate-drain electric field. The FP design reduced leakage current tenfold due to smoother electric field distribution, minimized inverse piezoelectric and electron trapping effects, and fewer gate leakage-induced defects. Kabemura *et al.* [148] demonstrated improved performance with short and moderate-length FPs with a high-*k* passivation layer. Breakdown performance improves with both a higher dielectric constant and an increased deep-acceptor density ($2\text{-}3\times10^{17}$ cm^{-3}). Optimal devices achieve 500 V breakdown at 1.5 μm gate-drain spacing, demonstrating 3.3 MV/cm average field strength, showcasing high-*k* passivation's potential for high-voltage GaN HEMTs. Soni *et al.* [149] compared drain-connected lateral, vertical, and dual-FP designs. Lateral FPs showed V_{br} roll-off as peak electric fields shifted from drain to gate, while vertical FPs faced roll-off due to buffer thickness limits. The dual-FP structure resolved these by distributing the electric field between gate and drain, allowing HEMT scaling without sacrificing breakdown or on-state performance.

Xia *et al.* [150] introduced a micro-FP structure that enhances electric field distribution and offers charge-balancing, outperforming traditional lateral FP designs in V_{br} and current collapse suppression. Zhang *et al.* [151] proposed a super FP

method that avoids occupying the drift region, improving V_{br} while maintaining on-state performance. Recent breakthroughs in FP engineering have propelled AlGaN/GaN HEMT performance to unprecedented levels. The sunken source-connected FP (SCFP) architecture developed by Bothe *et al.* [152] has demonstrated remarkable capabilities, achieving >10 W/mm output power and >60% PAE at 10 GHz while reducing parasitic capacitances by up to 60%. This design's optimized electric field distribution enables 25% higher drain voltage operation and exceptional reliability (>6×10^7 hours at 225°C), establishing new benchmarks for high-power RF systems. Complementing these electrical advancements, innovative thermal management approaches have emerged as critical enablers for device reliability. Kobayashi *et al.* proposed an alternative FP design known as the slant FP [153], which suppresses current collapse more effectively than the conventional parallel-plate FP due to a weaker electric field at the gate edge. The current collapse diminishes as the number of SiCN steps increases. In pulsed I–V measurements, the slant FP demonstrates a notable reduction in current collapse compared to standard FP structures. Wong *et al.* [136] also created a SiN slant FP on AlGaN/GaN HEMTs using HSQ surface tension, achieving *fT/fmax* = 41/100 GHz, low on-resistance, and strong high-frequency performance 146 V V_{br} without enlarging the device. The development of asymmetric slant FPs [154] represents a fundamental shift from passive heat dissipation to active thermal mitigation. Electro-thermal analyses confirm these structures can reduce heat generation density by 50% and lower junction temperatures by 16%, while simultaneously improving electrical characteristics through field distribution optimization. Unlike conventional FPs, which are limited by thin SiN passivation layers, the air-bridge FP (AFP) structure extends from the source over the gate and lands between the gate and drain. By leveraging the air's low dielectric constant, this configuration more efficiently redistributes the surface electric field, leading to improved electric field uniformity. Simulation results show that an AFP HEMT achieves a V_{br} of 450 V—twice that of a conventional FP device (240 V) [155]. For high-frequency applications, the integration of air-bridged FPs with asymmetric passivation [156] has set new performance standards, delivering 31.6% improvement in cut-off frequency while maintaining DC characteristics. This approach, validated through precision modeling

(1.4% error), demonstrates how advanced FP architectures can simultaneously address multiple performance trade-offs. Together, these innovations in FP design-spanning electrical optimization, thermal management, and RF performance enhancement-chart a clear pathway for next-generation GaN HEMTs in both power and communication applications.

2.6.2 Key Barrier Materials in HEMT Technology

GaN HEMTs have become a cornerstone in modern semiconductor technology, particularly in high-power and high-frequency applications. The choice of barrier layer materials significantly influenced the performance of GaN HEMTs, which play a critical role in determining the device's electrical properties, by affecting crucial electrical properties such as electron mobility, charge carrier density, and breakdown strength. Traditional GaN HEMTs utilize AlGaN as the barrier layer due to its ability to induce a 2DEG at the GaN/AlGaN interface, which is essential for high electron mobility. However, recent advancements have explored alternative barrier materials, such as InAlN and InAlGaN to further enhance device performance. These materials aim to address limitations in AlGaN-based HEMTs, such as lattice mismatch strain and polarisation-induced effects, to enhance device efficiency, power density, and reliability. The state-of-the-art in GaN HEMT technology is thus evolving rapidly, driven by the need for improved performance in applications ranging from 5G communications to power electronics.

Use of InAlN as a barrier layer, offers a lattice-matched alternative to GaN when the indium composition is around 17–18%, reducing strain and defect density compared to AlGaN [157]. This lattice matching minimizes strain and dislocation densities at the heterojunction, leading to higher electron mobility and lower defect densities [158]. Lattice-matched InAlN/GaN HEMTs offer several advantages over traditional AlGaN/GaN HEMTs. Lattice-matched InAlN/GaN HEMTs overcome the strain-related reliability issues of AlGaN/GaN devices caused by lattice mismatch [159]. They provide higher 2DEG sheet carrier density—up to twice that of AlGaN/GaN—resulting in better DC and RF performance [160]. This allows thinner barrier layers while maintaining high carrier density, improving high-frequency

operation by enabling a high gate-length-to-barrier-thickness ratio without gate recessing, thereby reducing short-channel effects [158]. With their high critical electric field, thermal stability, and fast electron saturation velocity, InAlN/GaN HEMTs are increasingly preferred for high-power and high-frequency applications [161]. Another critical advantage of InAlN/GaN heterostructures is their thermal stability, with operation demonstrated up to 1000 °C without significant degradation [162]. The reason for this is the absence of mechanical stress, stable surface properties, and the InAlN barrier's suppression of diffusion paths. The $\boldsymbol{P_{SP}}$ of both GaN and InAlN layers remains stable at high temperatures, preserving the interfacial polarisation discontinuity and maintaining the 2DEG for channel modulation [162].

InAlN/GaN HEMTs have demonstrated remarkable performance in both DC and RF domains [159]-[160]. Lecourt *et al.* [158] developed a 225-nm T-gate InAlN/GaN HEMT on sapphire, with 1.2 A/mm DC current density, g_m of 460 mS/mm, f_T = 52 GHz and f_{max} = 120 GHz, and 2.9 W/mm output power at 18 GHz with 28% power added efficiency (PAE)—the best performance for InAlN/GaN HEMTs on sapphire at that time. Further advances showed record RF results: 47-nm T-gate InAlN/GaN HEMT on sapphire with regrown contacts achieved a record f_T/f_{max} of 190/301 GHz ($\sqrt{(f_T \times f_{max})}$ = 239 GHz), driven by a high 2DEG velocity of 1.4×10^7 cm/s, g_m of 610 mS/mm, and a V_{br} of 14.7 V, rivalling GaN-on-SiC performance [163]. On Si substrates, Xing *et al.* [164] reported a record f_T of 250 GHz, while a 50-nm InAlN/GaN HEMT achieved an on/off current ratio (I_{on}/I_{off}) of 7.28×10^6, subthreshold swing (*SS*) of 72 mV/dec, V_{br} of 36 V, and f_T/f_{max} of 140/215 GHz [165]. Scaling analysis suggests that 20-nm devices with regrown ohmic contacts and reduced parasitic capacitance could yield f_T/f_{max} of 320/535 GHz, highlighting the scalability of InAlN/GaN HEMTs on Si and their potential to overcome parasitic limitations for next-generation high-frequency RF applications. For millimetre-wave power applications, Xu *et al.* demonstrated 0.1-μm InAlN/GaN HEMTs operating at 71–86 GHz with 1.63 W output power and 15% PAE at 86 GHz [166]. Zhou *et al.* [167] reported that InAlN/GaN HEMTs deliver higher output power density than AlGaN/GaN due to higher current density, lower knee voltage, and reduced parasitic resistance—achieving 1.62 W/mm at 8 GHz versus 1.10

W/mm for AlGaN/GaN under the same bias. However, PAE drops at higher drain voltages because of increased gate leakage, limiting operation to <6 V. Additionally, studies on microwave noise performance have shown that these devices maintain low minimum noise figures [159]. Surface passivation also significantly impacts the performance of InAlN/GaN HEMTs. An Al_2O_3 strain-passivation layer improved sheet resistance (R_{sh}) and g_m by 15% and 25% [168], while atomic layer deposition (ALD)-deposited Al_2O_3 reduced trapping, enhanced V_{br}, and improved subthreshold behaviour [169]. Compared to SiN passivation, Al_2O_3 also exhibited a higher I_D (1.8 A/mm), indicating superior surface charge control [166].

Despite their promising performance, InAlN/GaN HEMTs face challenges related to reliability and hot-electron degradation. Tapajna *et al.* [170] reported electron temperatures up to 30,000 K—much higher than in AlGaN/GaN—causing trap formation in the GaN channel and surface states, which leads to V_{th} shifts and current degradation. This highlights the need for improved passivation techniques and optimized biasing schemes to mitigate these effects. Gate leakage further reduces PAE and reliability, as shown in [171], where small-signal analysis revealed frequency-dependent RF degradation: leakage current interacting with C_{gs} and C_{gd} impacts lower frequencies more severely. Mitigation strategies include InGaN back barriers (enhancing carrier confinement and reducing buffer leakage) and surface oxidation before gate deposition (suppressing barrier leakage). Combined, 70-nm HEMTs achieved record-low Ioff of 7.15×10^{-8} A/mm with excellent RF results (*fT/fmax* of 215/45 GHz for rectangular gates and 130/160 GHz for T-gates) [172]. At the frontier, GaN-on-Insulator (GaNOI) technology [173] fabricated via 200 mm wafer bonding delivers superior DC/RF performance, with 120-nm devices reaching f_T = 96 GHz and reduced R_{sh} (301 → 284 Ω/□). GaNOI enables CMOS integration on a single chip, supporting compact high-power RF systems, while 50-nm Si-based HEMTs [165] with f_T/f_{max} of 320/535 GHz remain leading for millimetre-wave applications. Future research should focus on optimizing the epitaxial growth process to reduce defect densities and improve the crystalline quality of the InAlN barrier layer. Additionally, the development of novel contact metallization schemes and gate dielectrics could further enhance the thermal stability and electrical

performance of InAlN/GaN HEMTs. The integration of these devices with advanced cooling technologies and novel device architectures, such as gate-recessed structures and multi-channel designs, could also unlock new possibilities for high-power and high-frequency applications.

InAlGaN/GaN HEMTs are also emerging as superior devices for high-power, high-frequency applications due to their strong breakdown field and high electron velocity. Compared to conventional AlGaN/GaN HEMTs, they achieve higher current density, faster frequency response, and better thermal handling. Wang *et al.* [174] reported a 2DEG density of 2.0 $\times 10^{13}$ cm^{-2}, with an I_D of 1.94 A/mm, f_T of 142 GHz, and f_{max} of 203 GHz— nearly double that of AlGaN/GaN. Performance was further enhanced using a T-gate and low-k BCB encapsulation to reduce parasitic capacitances. Likewise, Tu *et al.* [175] demonstrated InAlGaN/GaN HEMTs on high-resistivity Si with g_m of 451 mS/mm, I_D of 908 mA/mm, an $f_T \times L_G$ product of 13.9 GHz·μm (f_T/f_{max} of 100/97 GHz), and 1.7 W/mm output power at 10 GHz with 33% PAE. Innovative structural and material advances have significantly boosted InAlGaN/GaN HEMT performance. Kao *et al.* [176] improved mobility (1540 $cm^2/V{\cdot}s$), reduced R_{sh} (228.2 Ω/sq) with a peak I_D of 1490 mA/mm and g_m of 401 mS/mm using a GaN insertion layer, while Lecourt *et al.* [33] achieved record mobility (2200 $cm^2/V{\cdot}s$), f_T/f_{max} of 113/200 GHz and I_D of 1.25 A/mm on sapphire. Dogmus *et al.* [177] reported exceptional low-temperature mobility (7340 $cm^2/V{\cdot}s$ at 4 K) with strong RF capability (f_T/f_{max} of 65/180 GHz). Shrestha *et al.* [178] proposed a lattice-matched double-barrier InAlGaN/GaN HEMT with a recessed gate, achieving a positive V_{th} of 0.2 V, I_D of 1149 mA/mm , and g_m of 358 mS/mm, improving carrier injection and reliability. Advanced thermal and passivation strategies enhance power handling and reliability. Ohki *et al.* [179] cut thermal resistance by 60% using a SiC/diamond heat spreader, achieving 22.3 W/mm at S-band with 257 V V_{br}. Aubry *et al.* [180] improved ICP-CVD SiN passivation, reducing trapping and delivering 6 W/mm with 42% PAE at 30 GHz. Rzin *et al.* [181] showed that in situ SiN passivation (14–22 nm) minimized low-frequency noise, with 1/f noise dominated by gate-region effects, ensuring reliability for high-power RF systems. Delage *et al.* [182] and Sanyal *et al.* [183] further showed 10

W/mm at 30 GHz and an 8.1 THz·V Johnson's FOM on low-resistivity Si, demonstrating substrate versatility.

Recent advances highlight the superior performance of InAlGaN/GaN HEMTs. A study [184] using TCVD SiNx passivation achieved record X-band output (31 W/mm), high mobility (2048 cm²/V·s), I_D (1230 mA/mm), low R_{sh} (293 Ω/sq), and 227 V V_{br}, outperforming PECVD SiNx by suppressing 2DEG degradation and current collapse. Zhang *et al.* [185] employed an Fe-doped buffer with an InGaN back-barrier, reducing off-state leakage and delivering 4.6 W/mm at 94 GHz through enhanced carrier confinement. Murugapandiyan *et al.* [186] reported a 50-nm gate InAlGaN/GaN/AlGaN HEMT on SiC with a T-gate and regrown n++ GaN contacts, achieving a record f_{max}/f_T of 425/310 GHz, 2.9 A/mm I_D, 0.49 Ω·mm on-resistance (R_{on}), and 38 V V_{br}. InAlGaN/GaN HEMTs surpass AlGaN/GaN counterparts through higher 2DEG density, reduced R_{sh}, and advanced fabrication techniques like lattice-matched barriers, T-shaped gates, and diamond heat spreaders. These innovations, combined with quaternary barriers, optimized passivation, back-barriers, regrown contacts, and thermal management, position InAlGaN/GaN HEMTs as frontrunners for next-generation high-power, high-frequency, and low-noise RF applications, with potential for cost-effective integration on silicon and sapphire substrates.

2.7 Analytical Modeling of GaN HEMT

The main objective of semiconductor device modeling is to predict how a device will perform under particular conditions, such as applied voltages and currents (bias), external influences like temperature and radiation, and physical characteristics such as size and doping concentrations. An effective model balances accuracy with computational cost [187], and device models are generally grouped into several categories:

i) Physics-Based or Analytical Model: Derived from the physical principles of device operation, this model uses physics-based equations and device parameters to achieve high accuracy. However, it requires complex

calculations and slow simulations, making it computationally intensive but essential for understanding new devices.

ii) Behavioural or Empirical Model: This model predicts device behaviour using fitted mathematical equations rather than physical principles. It allows fast simulations but loses accuracy when conditions fall outside the fitting range.

iii) Semi-Physics or Semi-Empirical Model: This approach balances the accuracy of physics-based models with the efficiency of empirical models. It simplifies physical equations using practical assumptions and mathematical fitting, making it widely used in SPICE simulators and common in engineering applications.

iv) Numerical Model: This model uses numerical simulations to predict device performance under various conditions. Tools such as SILVACO, Sentaurus TCAD, and MEDICI provide virtual environments for device optimisation, allowing validation of results that would be expensive or time-consuming to obtain experimentally.

2.7.1 Model for 2DEG Sheet Density

Creating a current-voltage (I-V) model starts with modeling the 2DEG density as a function of the V_G. This requires defining the Fermi level's dependence on V_G, or its dependence on the 2DEG density. Early models for the Fermi level's dependence on the 2DEG density were developed more than 30 years ago for AlGaAs/GaAs HEMTs and are also applicable to AlGaN/GaN HEMTs. Initial approximations included $E_F = 0$ [16], a linear approximation [188], a second-order approximation [189], and a non-linear dependence [190]. Although these approaches provided straightforward expressions for the 2DEG, their precision was constrained. E_F as a function of n_s by a simple polynomial [191] was later introduced, providing a more accurate and analytical n_s model. The polarisation charge model, essential for accurate n_s modeling, was developed [192] to describe 2DEG density considering P_{SP} and P_{PZ} polarisation. Another model for n_s was introduced by Rashmi *et al.* [193] with three approximations, corresponding to "weak," "moderate," or "strong" inversion. This model incorporated the polarisation charge model proposed by

Ambacher *et al.* [192]. Further, new models were introduced by applying the Robin boundary condition to solve the 1-D Schrödinger equation [194]. An improved model was introduced [195] with incorporated parasitic channel conduction in the AlGaN layer at high V_G, estimating its onset voltage. However, this model relied on numerical methods, making it unsuitable for circuit simulators. In 2011, Khandelwal *et al.* [196] developed a unified analytical n_s model, using different approximations for E_F in subthreshold and above-threshold regions. This model initially failed to account for parasitic channel conduction at higher V_G. A fully analytical model for n_s was introduced [197], eliminating numerical methods and including electron charge in the AlGaN layer and parasitic channel conduction, accurately predicting 2DEG density saturation at higher voltages. A physics-based model for n_s and I-V/capacitance-voltage (C-V) characteristics using surface-potential (SP) analysis was proposed [198]-[199] to overcome threshold voltage definitions errors due to varying Fermi level with gate-to-channel voltages.

2.7.2 I-V Characteristics

When modeling output I-V characteristics, the saturation region in I_D (V_D, V_G) curves can account for or ignore channel length modulation, depending on its relevance to device operation. Notably, the same I-V models apply to devices with or without FP structures without significant errors. Like charge-control models, I-V models have existed since the early 1980s, initially developed for AlGaAs/GaAs HEMTs but adaptable to AlGaN/GaN HEMTs, excluding polarisation modeling. The initial AlGaAs/GaAs I-V characteristic model, proposed in [16], employed a charge-control approach that neglected the Fermi level voltage when computing the 2DEG density and treated carrier mobility as constant, unaffected by the lateral electric field. This simplification resulted in a two-piece linear drift-velocity versus field relationship, compromising accuracy. This was improved by incorporating the Fermi level dependence on V_G using a linear approximation with curve-fitted parameters from Fermi-Dirac simulations [188]. Further advancements [200] involved numerically solving Poisson and drift-diffusion equations to accurately model the 2DEG concentration and AlGaAs current as functions of V_G, thereby incorporating AlGaAs conduction effects. AlGaN/GaN HEMTs differ from AlGaAs/GaAs HEMTs

mainly due to their strong P_{SP} and P_{PZ} polarisation, eliminating the need for additional doping. This leads to a fundamental difference in I-V models: the charge-control model centres on the polarisation-induced 2DEG and disregards any charge from doping (assuming the AlGaN layer is unintentionally doped). The 2DEG in N- and Ga-face AlGaN/GaN heterostructures using P_{SP} and P_{PZ} polarisation [192] were modelled, forming the foundation for the first analytical I-V model. This I-V model [201] incorporated field-dependent and excluded the Fermi level voltage in the charge-control model. It accurately modelled the saturation region by dividing the channel into low-field and high-field regions, focusing on precise output conductance modeling, crucial for microwave signals. An enhanced analytical model for n_s was proposed [192], integrated into the I-V characteristics model. The charge-control model used three different approximations to describe how the Fermi level varies with 2DEG sheet density, each designed for weak, moderate, or strong inversion regimes. The I-V characteristics of AlGaN/GaN HEMTs were also modelled [194] using a V_{th}-dependent analytical approach. This work introduced a more advanced charge-control model by solving the 1-D Schrödinger equation using the Robin boundary condition, resulting in greater accuracy for E_F dependence on V_G compared to the Dirichlet condition [191]. In another study [202], a 2-D analytical model addressed the kink effect in output characteristics, incorporating an advanced charge-control model that solved the 2-D Poisson equation using Robin boundary conditions. This established a direct relationship between 2DEG density and structural parameters, such as Al composition and AlGaN layer thickness, enhancing the understanding of device performance. Additionally, a modified Polyakov-Schwierz mobility model was introduced to describe the I-V characteristics, successfully demonstrating negative differential mobility in drift velocity and outperforming the Canali model [203].

One study [204] proposed an analytical model that simplifies the I_D into a five-parameter closed-form equation, employing a two-zone approach (gated and velocity-saturated regions). This model extends to RF operation through a 12-parameter parasitic network, effectively fitting both DC and S-parameter measurements while providing intuitive design insights. However, it neglects

trapping and self-heating effects to maintain simplicity. Yigletu *et al.* [205] developed compact models for I-V and C-V characteristics using a unified charge control model, considering only the first energy level in the 2DEG. Validated across devices with gate lengths ranging from 0.35 to 1 μm, this model incorporates self-heating and short-channel effects, thereby enhancing its applicability. Similarly, Karumuri *et al.* [206] introduced a charge linearization approach for I_D modeling, accounting for parasitic barrier layer conduction and transistor-based access region modeling. The model was validated for both AlGaN/GaN and AlInN/GaN HEMTs, confirming its robustness across different material systems. Collectively, such models enhance the understanding and design of AlGaN/GaN HEMTs, addressing key performance factors while recognising limitations like thermal and trapping effects. A 2-D analytical model for AlGaN/GaN HEMTs [207] incorporates self-heating effects by including temperature-dependent parameters such as 2DEG density, Fermi level, mobility, and saturation velocity. It explains the negative differential resistance at high power dissipation and is validated against experimental data on Sapphire and SiC substrates. Similarly, Huque *et al.* [208] developed a temperature-dependent analytical model for DC I–V characteristics of AlGaN/GaN power HEMTs, analysing the impact of elevated temperatures (300–500 K) on band gap energy, sheet carrier density, V_{th}, mobility, and saturation velocity. Although suitable for circuit simulators and capable of predicting performance under extreme conditions, the model neglects temperature effects on $\emptyset_b$, polarisation charges, and bulk resistances, which limits its accuracy. Nonetheless, it provides a basis for optimising power HEMTs in high-temperature applications and advancing thermal modeling. In a related study, Tijent *et al.* [209] introduced a simplified analytical model to estimate sheet carrier density and I–V characteristics of AlGaN/GaN HEMTs, considering polarisation charges, V_G, Al content, gate length, mobility, and temperature. By solving Poisson's equation, this model effectively predicts key parameters such as I_D and f_T, showing good agreement with experimental data. Its simplified approach—excluding minor AlGaN contributions and focusing on above-threshold behaviour—makes it useful for educational purposes and preliminary device design. However, the omission of self-heating and access resistance reduces accuracy at high V_G. Overall, these models offer complementary insights into

AlGaN/GaN HEMT behaviour, balancing complexity with practicality while indicating the need for improved treatment of thermal and structural effects. Future work should address the overlooked effects by employing advanced computational methods and validating models across broader experimental conditions to improve the reliability and scalability of AlGaN/GaN HEMTs in high-power, high-frequency, and high-temperature applications. This review highlights the groundwork established by existing models and positions the proposed research to overcome these limitations through the development of a more comprehensive analytical model for next-generation AlGaN/GaN HEMT designs.

2.8 TCAD Silvaco Simulation Methodology

The two-dimensional device simulations were conducted using Silvaco Atlas TCAD [210], a versatile simulation tool designed to model various semiconductor devices, ranging from highly scaled silicon MOSFETs to high-power bipolar transistors. It also enables the simulation of heterostructure devices like AlGaN/GaN HEMTs, SiC-MESFETs, and GaN-MOSFETs by integrating advanced physical models and reliable numerical methods to ensure accurate device behaviour representation. These simulations aim to examine the internal physical mechanisms within the device structure and enhance understanding of the fundamental physics, which is essential for optimizing future semiconductor device performance. In Silvaco Atlas TCAD, the actual semiconductor device is approximated as a virtual 2D/3D model, where physical properties are discretized across a non-uniform mesh of nodes. Thus, the virtual device serves as a simplified representation of the real device. The structure is divided into multiple grid points (nodes), where electrical properties such as electric field, voltage, and currents are calculated through numerical simulations. Consequently, the meshing process plays a critical role in device simulation. While higher mesh density improves calculation accuracy, it also increases simulation time, creating a trade-off between precision and computational efficiency. Achieving the maximum benefit from physical simulation requires a careful balance between precision and computation time. Silvaco offers several simulation tools, with this work utilizing ATLAS—a physics-based 2D/3D device simulator for analysing semiconductor device behaviour under specified bias

conditions. The process begins by defining the device structure, including doping profiles and mesh. This can be done either by simulating fabrication steps in ATHENA (with mesh refinement in DEVEDIT) or by scripting directly in DECKBUILD to specify mesh, material composition, and doping. Within ATLAS, models, biasing conditions, and numerical methods are then configured to compute the device's electrical characteristics.

The simulator then generates three key output files: runtime data showing simulation progress, log files recording electrode currents and voltages, and structure files containing physical quantities at different bias points. For visualization, TONYPLOT is generally used to present log and structure files. The data obtained from TONYPLOT was transferred and visualized in Microsoft Excel to improve readability and presentation quality.

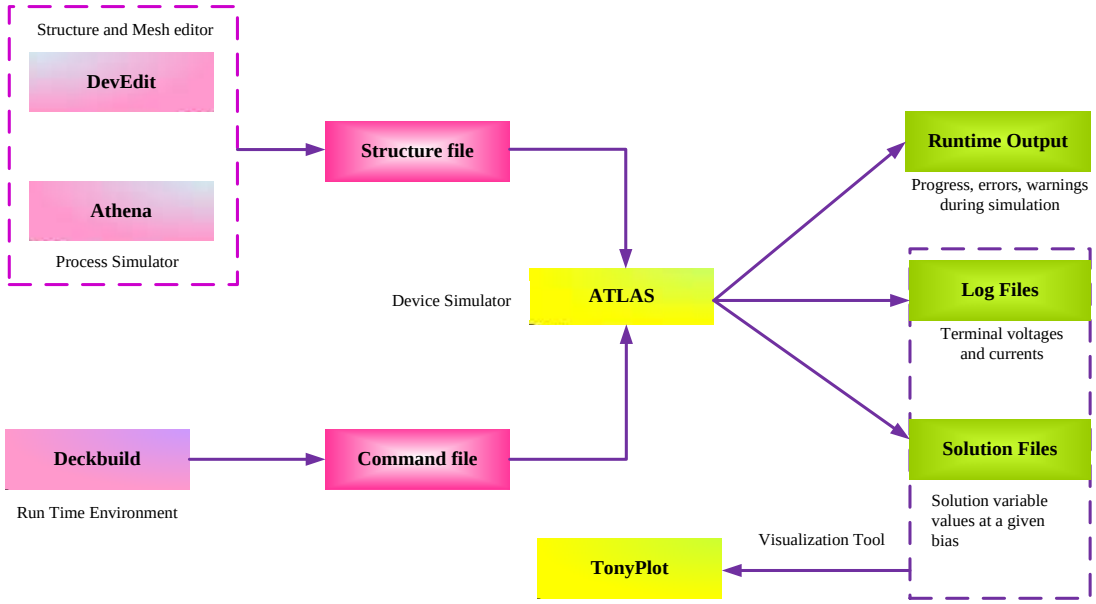


Fig 2.8. Workflow of Silvaco simulations, highlighting the input parameters and output results of ATLAS.

2.8.1 Basic Semiconductor Equations

Extensive research in device physics has led to the development of a universal mathematical model applicable to all semiconductor devices [211]. Semiconductor device modeling relies on a universal mathematical framework

derived from Maxwell's laws. The key equations are Poisson's, continuity, and transport equations, which describe electrostatic potential, charge distribution, and carrier behaviour.

Poisson's Equation links the electrostatic potential (ϕ) with charge density (ρ) and permittivity (ε):

$$\nabla^2\varphi = -\nabla.E = \rho / \varepsilon$$

(2.5)

Continuity equations for electrons and holes account for carrier generation (g), recombination (r), and current densities j_N and j_P:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.j_N - r_N + g_N$$

(2.6)

$$\frac{\partial n}{\partial t} = \frac{-1}{q}\nabla.j_P - r_P + g_P \qquad (2.7)$$

Here, N is the electron concentration and P is the hole concentration, while their corresponding current densities are denoted by j_N and j_P. The terms r_N and r_P denote recombination rates, and g_N and g_P represent generation rates.

2.8.2 Carrier Transport and Recombination Models

A critical component of device simulation in TCAD is the accurate modeling of carrier transport under different operating conditions. This includes mobility behaviour, recombination mechanisms, impact ionization, and carrier statistics, all of which directly influence the electrical performance of GaN HEMTs. These models account for the dependence of transport and recombination on electric field, temperature, doping, and material properties, ensuring realistic prediction of device performance.

2.8.2.1 Carrier Mobility Models

Carrier mobility is affected by lattice temperature, electric field, and doping concentration due to scattering from phonons, impurities, surfaces, and defects. Additionally, under strong electric fields, mobility decreases due to velocity

saturation. Correctly modeling these effects ensures that R_{on}, current levels, and switching speed are accurately reproduced in simulations. In ATLAS, several models are available:

a) Constant Low-field Mobility Model – assumes uniform mobility independent of doping or field but includes temperature dependence.
b) Albrecht Mobility Model [212] – incorporates doping and temperature dependence.
c) Parallel Electric Field-Dependent Mobility Model [213] – accounts for velocity saturation in strong fields.
d) GANSAT.N Model – a specialized high-field mobility model for GaN-based devices (e.g., AlGaN/GaN HEMTs), based on Monte Carlo [214] simulation data, ensuring accurate high-field transport behaviour.

These models are activated via the MOBILITY statement, with user-adjustable parameters (e.g., AN.ALBRCT, VSATN).

2.8.2.2 Carrier Generation–Recombination (G–R) Models

Generation-recombination (G-R) occurs when an electron transitions from the valence band to the conduction band, creating an electron-hole pair. Carrier generation and recombination strongly influence leakage currents and switching dynamics. The main models include:

a) Shockley–Read–Hall (SRH) Model – trap-assisted recombination through defect or impurity levels; implemented by enabling SRH in the MODELS statement.
b) Concentration-Dependent SRH (CONSRH) – allows carrier lifetimes to vary with doping concentration.
c) Auger Recombination Model [215]-[216] – three-particle interaction where recombination energy is transferred to another carrier, dominant in heavily doped regions.

Model parameters such as electron/hole lifetimes (TAUN0, TAUP0) and Auger coefficients (AUGN, AUGP) are defined in the MATERIAL statement.

2.8.2.3 Impact Ionization Models

In high electric fields, carriers gain sufficient energy to create additional electron–hole pairs, leading to avalanche breakdown. ATLAS employs Selberherr's Model, which expresses ionization rates of electrons and holes as exponential functions of the local electric field.

2.8.2.4 Carrier Statistics Models

Carrier statistics determine the calculation of electron and hole densities under different doping and field conditions.

a) Boltzmann Statistics [217]-[218] – a simplified form valid under non-degenerate conditions (lightly doped semiconductors).
b) Fermi–Dirac Statistics – required for degenerate (heavily doped) materials; enabled via the FERMIDIRAC option in the MODELS statement.

ATLAS allows switching between approximations, ensuring flexibility in device modeling across doping regimes.

2.9 Summary

This chapter presents an in-depth literature review on GaN based HEMTs, exploring their structural properties, operational fundamentals, and device design. The analysis starts with an overview of the III-Nitride crystalline framework, then proceeds to examine the operational dynamics and different HEMT configurations, distinguishing between Normally-On and Normally-Off designs. Critical performance-limiting factors—such as thermal effects, current collapse, leakage currents, and electric field management—are thoroughly evaluated, emphasizing their influence on device efficiency and long-term stability. Modern mitigation strategies, including FP integration and advanced barrier materials, are also reviewed to enhance HEMT functionality. Further, the chapter investigates analytical modeling approaches for GaN HEMTs, particularly addressing 2DEG density estimation and I-V behaviour. It also elaborates on the TCAD Silvaco simulation framework, covering core semiconductor physics, charge carrier mobility, and recombination processes. By bridging theoretical models with computational simulations, this chapter lays the

groundwork for subsequent research aimed at improving GaN HEMT performance through optimized design and material engineering.

CHAPTER 3

Optimization of Field Plate Architectures for HEMT Devices

3.1 Introduction

Owing to the high saturation velocity and the formation of 2DEG, GaN-based devices can achieve high output current [219]. However, current research challenges include enhancing the breakdown voltage (V_{br}), increasing the cut-off frequency (f_T), and minimizing the on-resistance (R_{on}) of the device. To enhance the V_{br} of power devices, several techniques are used, including guard rings, junction termination extension (JTE) [220], and field plates (FPs) [221]. Among these, FPs offer the simplest fabrication process [222]. This is also one of the most effective techniques to enhance the breakdown characteristics of AlGaN/GaN HEMTs [112]. FP is a conductive layer placed over the gate in a HEMT that helps redistribute the electric field, reducing peak field concentrations near the gate edge and thereby improving device reliability. Various FP designs exist, such as single-FP [143], dual-FP [144], [223], inner [145], slant [153], multi-finger [146], multistep [224], and air-bridge [155] configurations. However, increasing V_{br} often involves a trade-off with f_T and R_{on}. Therefore, optimizing the device's physical design is crucial to boost V_{br} while keeping R_{on} low and f_T high [228]. Recent studies have demonstrated that the strategic placement and design of FPs can significantly influence V_{br}, capacitance, and high-frequency operation [143]. However, the addition of FPs often introduces trade-offs, such as increased capacitance and reduced frequency performance, necessitating careful design optimization [112]. This chapter explores different FP structures—ranging from gate-connected FPs with innovative geometries to source- and drain-connected FPs, including single and dual FPs—using TCAD simulations to evaluate their impact on electrical and analogue performance. The chapter is organized into four sections, each corresponding to one of the studies, followed by a comparative discussion and concluding remarks. The aim is to synthesize these findings to provide a cohesive understanding of FP optimization strategies for AlGaN/GaN HEMTs, contributing to the broader objective of this thesis: advancing the design of high-performance GaN-based power devices.

3.2 Influence of Field Plate Placement on HEMT Characteristics

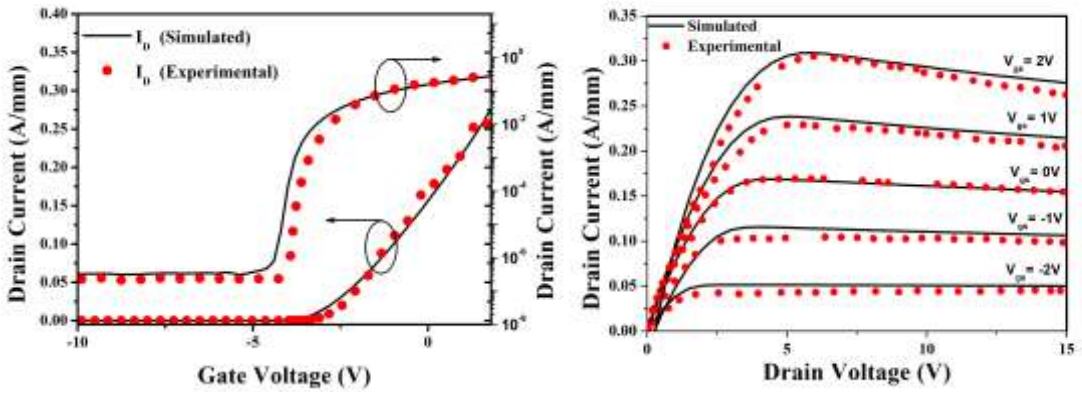
An AlGaN/GaN HEMT with a FP structure was developed, featuring a 0.2 µm-GaN buffer layer, a 20 nm n-doped AlGaN barrier grown above it and a 600 nm Si_3N_4 passivation layer deposited on top. The device has a gate length (L_G) of 0.5 µm, gate–drain spacing (L_{GD}) of 3.7 µm, and source–gate spacing (L_{SG}) of 0.5 µm. The Schottky gate contact has a work function of 5.23 eV. FP length (L_{FP}) is varied from 0.5 to 3.1 µm to study electrical and analogue performance using the ATLAS TCAD simulator [210]. The AlGaN and GaN channel doping concentrations are 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3}, respectively, with an Al mole fraction of 0.23 in the AlGaN barrier. Different physics models, like the Selberherr impact ionization model (Selb), the concentration-dependent lifetime Shockley-Read Hall recombination (Consrh) model, the Albrecht model, the Gansat and the Fermi–Dirac model are employed in the proposed Silvaco (TCAD) simulation. The ionization coefficients used are AN = 2.98×10^8, AP = 2.23×10^7, BN = 3.44×10^7, and BP = 2.7×10^8, where AP and BP represent hole impact ionization rates, while AN and BN correspond to electron impact ionization rates. Additionally, the piezoelectric-polarization (strain) model is incorporated to analyse the 2DEG formed at the AlGaN/GaN interface due to polarization effects. The simulation physical models employed in this chapter are detailed in Section 2.8. Device parameters and physical specifications used in this experiment are listed in Table 3.1 and 3.2.

Table 3.1. AlGaN/GaN HEMT device parameters

ATLAS specification	GaN	AlGaN
Bandgap (eV)	3.4	3.96
Mobility of electron (cm^2/V-s)	900	600
Mobility of hole (cm^2/V-s)	10	10
Conduction band effective density of states	2.24	2.07
Valence band effective density of states ($10^{19}cm^{-3}$)	1.16	1.16

Table 3.2. Physical specifications employed to design the AlGaN/GaN HEMT

Parameters	Values (µm)
Gate length (L_G)	0.5
AlGaN layer (d_{AlGaN})	0.02
GaN layer	0.2
Passivation layer	0.6
Source to gate distance (L_{SG})	0.5
Gate to drain distance (L_{GD})	3.7
Field plate length (L_{FP})	Varying from 0.5 to 3.1
Field plate thickness (T_{FP})	0.02



(a) (b)

Fig. 3.1. Calibration of simulator: DC curves of HFET (a) I_D-V_G, and (b) I_D-V_D characteristics, where the black lines represent the simulated data and the red symbols represent experimental data.

The simulation environment was validated by designing a GaN-based super HFET structure using the existing TCAD simulator and comparing the results with experimental data from [226]. Fig. 3.1 illustrates that the simulation outputs closely match the experimental results. For uniformity, the same simulation parameters were used across all structural analyses in this work. Four different cross-sectional views of AlGaN/GaN HEMTs structures—a standard HEMT without-FP, gate-connected FP, source-connected FP, and drain-connected FP—are given in Fig. 3.2. Si_3N_4 is

used as the passivation layer because it provides higher V_{br} than SiO_2 [227]. To analyse the breakdown characteristics, the L_{FP} of the structures given in Fig. 3.2 were adjusted between 0.5 and 3.1µm. For the AlGaN/GaN HEMT structure without-FP, V_{br} reaches a maximum of 261 V, as shown in Fig. 3.3(a). In contrast, the gate-connected FP AlGaN/GaN HEMT achieves significantly higher V_{br} across different L_{FP} (ranging from 0.5 µm to 3.1 µm), as illustrated in Fig. 3.3(b). The highest V_{br} of 742 V is obtained at an L_{FP} of 0.9 µm. For the source-connected FP AlGaN/GaN HEMT, the highest V_{br} of 765 V (Fig. 3.3(c)) is achieved at an optimal L_{FP} of 2.1 µm, which is also the maximum V_{br} observed in this comparative study. In contrast, the drain-connected FP HEMT structure shows only a marginal improvement, reaching a V_{br} of 317 V at

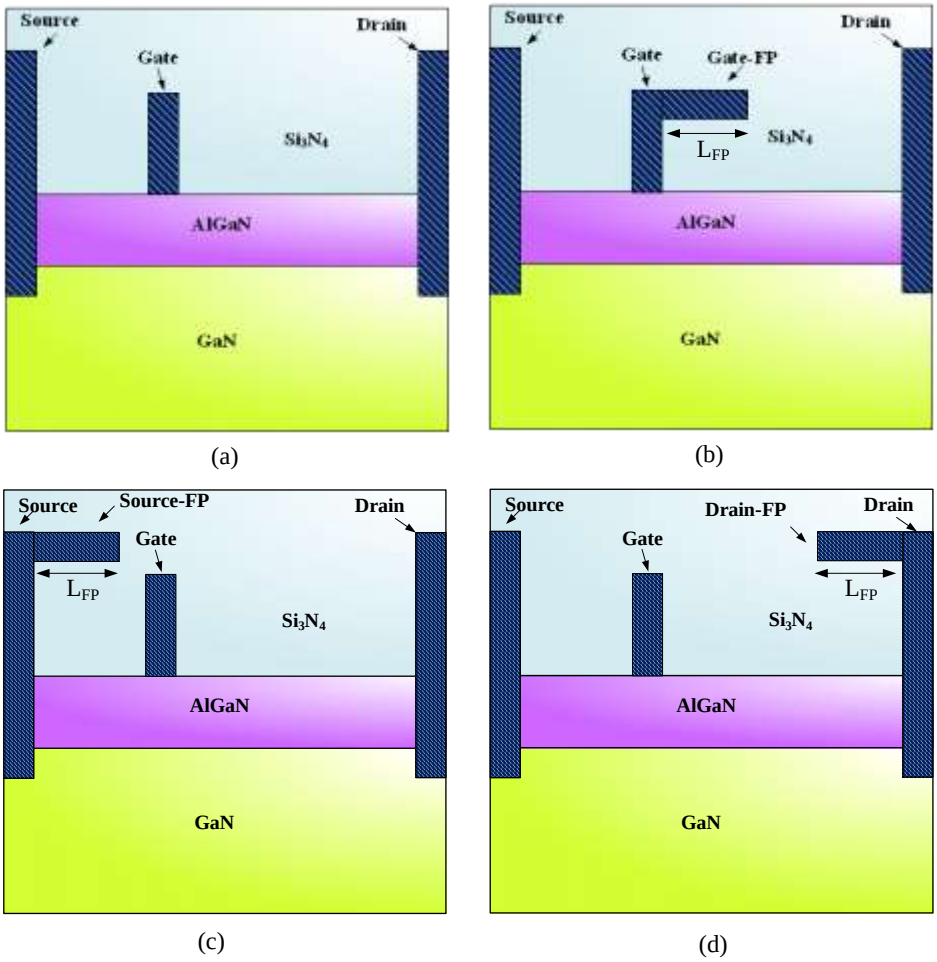


Fig. 3.2. Various AlGaN/GaN HEMT configurations: (a) without-FP, (b) gate-connected FP, (c) source-connected FP, and (d) drain-connected FP.

L_{FP} = 1.7 µm (Fig. 3.3(d)), which is slightly higher than the V_{br} of the without-FP design. The electrical characteristics of four different AlGaN/GaN HEMT structures—a standard HEMT without-FP, gate-connected FP (0.9 µm), source-connected FP (2.1 µm), and drain-connected FP (1.7 µm)—were compared, with each featuring the highest V_{br} in its respective configuration. The findings from this analysis are summarized in Fig. 3.4. The transfer (I_D-V_G) characteristics (Fig. 3.4(a)) were simulated at a drain voltage (V_D) of 0.1 V, from which the maximum transconductance (g_m) was identified at a V_G of -2 V. Simultaneously, the output (I_D-V_D) characteristics (Fig. 3.4(c)) were obtained at a fixed V_G of 0 V. The conventional structure without- FP exhibits a threshold voltage (V_{th}) of -2.29 V, maximum g_m of 51.4 mS/mm, maximum drain current (I_{dmax}) of 54 mA/mm, and drain saturation current (I_{dss}) of 1.298 A/mm.

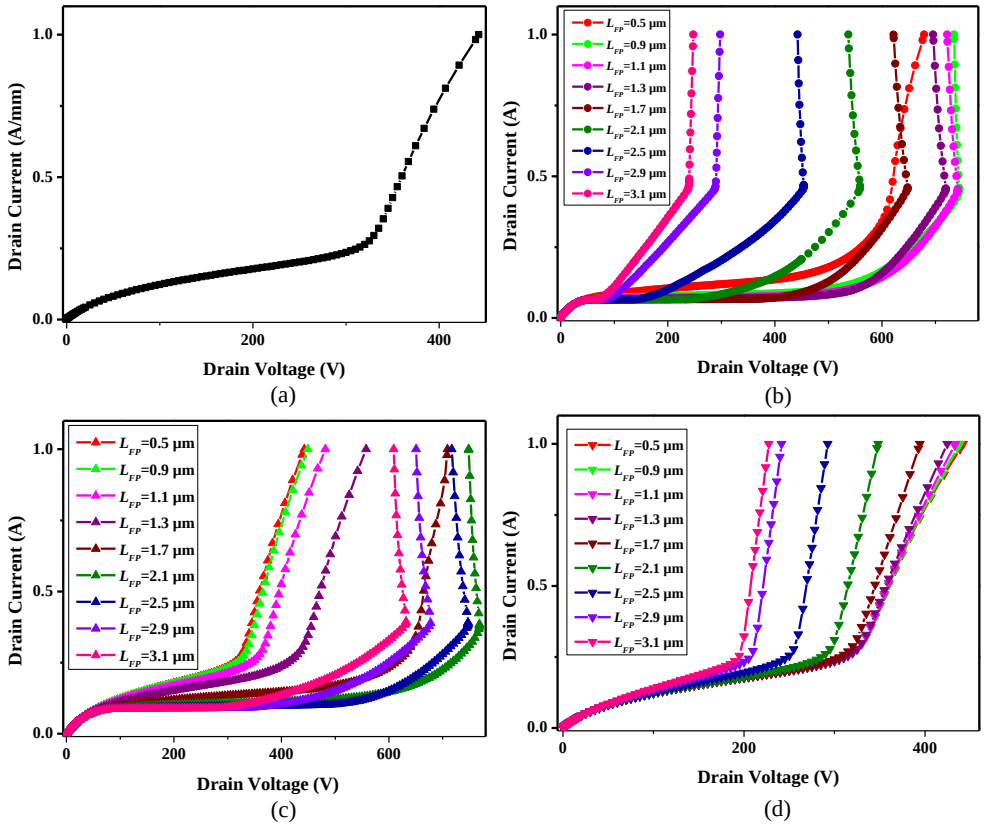


Fig. 3.3. V_{br} characteristics of AlGaN/GaN HEMTs: (a) without-FP, (b) gate-connected FP, (c) source-connected FP, and (d) drain-connected FP configurations for different L_{FP}.

Consequently, the AC analysis was carried out at a bias condition of V_D = 8 V. Under this biasing, small-signal parameters were extracted, which were subsequently used to evaluate f_T. The conventional without-FP structure demonstrates a C_{gs} and C_{gd} of 1.67 pF/mm and 0.21 pF/mm, respectively, achieving a f_T of 53.67 GHz but showing a relatively low V_{br} of 281 V. When examining the FP configurations, the gate-connected FP HEMT maintains the same V_{th} while showing comparable drain current characteristics (I_{dmax} = 54 mA/mm, g_m = 51.1 mS/mm, I_{dss} = 1.294 A/mm). This configuration exhibits slightly higher capacitances (C_{gs} = 1.91 pF/mm, C_{gd} = 0.38 pF/mm) and a reduced f_T of 44.10 GHz, but demonstrates significant improvement in V_{br} (742 V). The source-connected FP HEMT presents similar performance with a maximum g_m of 51.1 mS/mm, I_{dmax} of 53 mA/mm, I_{dss} of 1.293 A/mm, and achieves the highest V_{br} among the FP configurations at 765 V, while maintaining a competitive f_T of 48.67 GHz and showing the lowest C_{gd} (0.18 pF/mm) among FP devices.

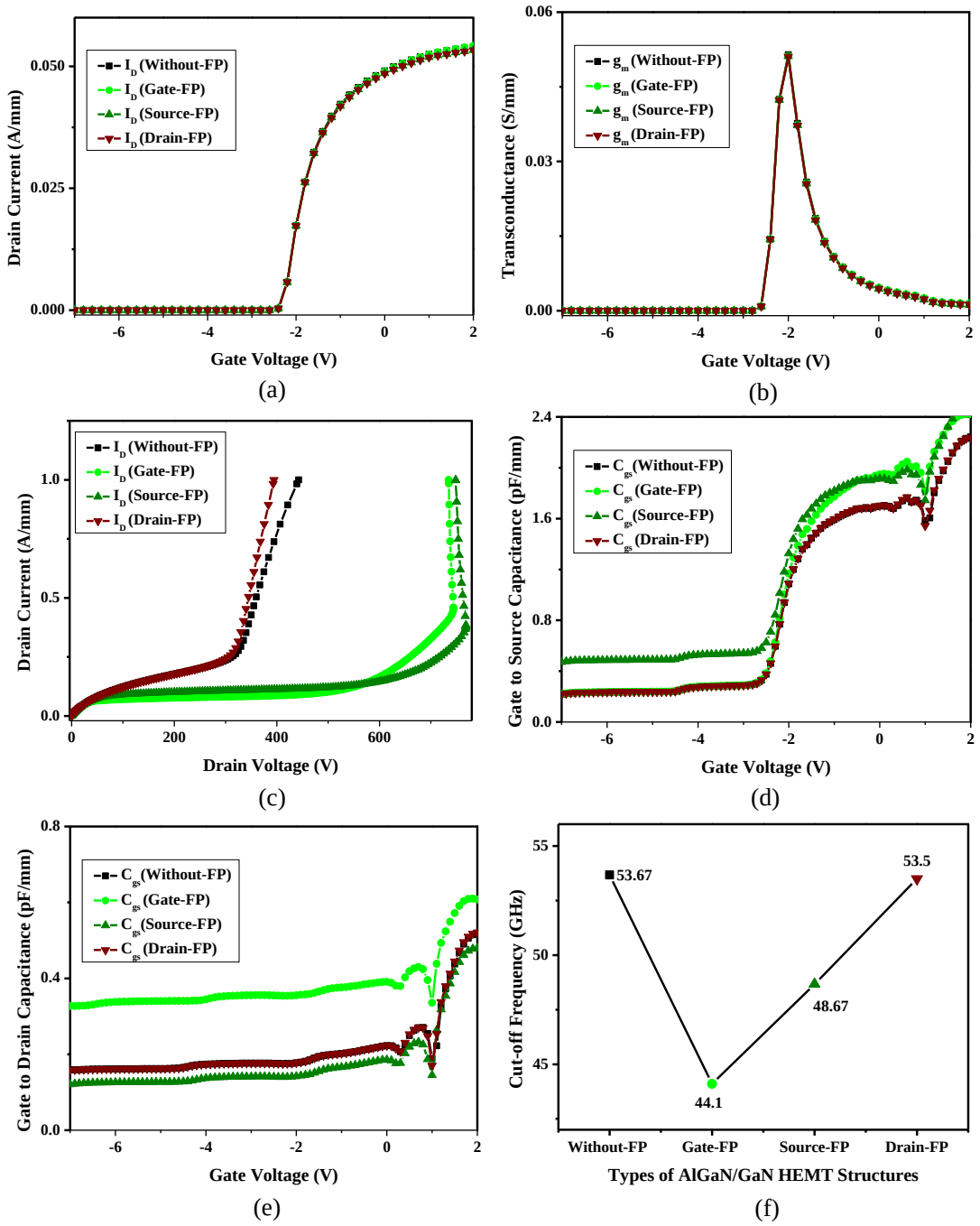


Fig. 3.4. Electrical characterization of the four AlGaN/GaN HEMT configurations: (a) I_D-V_G characteristics, (b) g_m, (c) V_{br}, (d) C_{gs}, (e) C_{gd}, and (f) f_T.

The drain-connected FP HEMT shows characteristics closest to the without-FP device, with maximum g_m of 51.0 mS/mm, I_{dmax} 53 mA/mm, and I_{dss} of 1.297 A/mm, while demonstrating only marginal improvement in V_{br} (317 V) compared to the without-FP structure. This configuration maintains excellent frequency response

(f_T = 53.50 GHz) and capacitance values nearly identical to the without-FP device (C_{gs}= 1.68 pF/mm, C_{gd}= 0.21 pF/mm). The comparative analysis (Fig. 3.4) reveals that while all FP configurations maintain similar DC characteristics, the source-connected FP implementation provides the optimal balance between V_{br} enhancement and frequency performance degradation, whereas the drain-FP shows minimal improvement over the without-FP structure. The gate-connected FP configuration offers intermediate performance, significantly improving breakdown characteristics while moderately affecting frequency response and capacitance values. The optimized length of source-FP is comparatively more than the length of gate-FP. Therefore, despite the marginally higher V_{br} observed in the source-FP configuration, the subsequent detailed investigation in this thesis concentrates on the gate-FP structure, owing to its superior scalability, simpler design, and broader potential for performance optimisation. Further evaluation of analogue parameters, such as capacitance and maximum operating frequency, suggests that incorporating an FP adversely affects these characteristics. Therefore, careful optimization of the FP design and placement is essential to achieve balanced performance in HEMT devices.

3.3 Impact of Different Gate Field Plate Structures on HEMT

To study the influence of various gate-FP configurations (Fig. 3.5) on the performance of AlGaN/GaN HEMTs, four gate -FP structures—Γ Gate-FP, ⅂ Gate-FP, T Gate-FP, and F Gate-FP—are studied along with a conventional without-FP structure using ATLAS. These architectures are systematically categorized as cases a through e in Table 3.3. All device parameters maintain the values specified in Tables 3.1 and 3.2, with the sole modification being the L_{FP}, which is now set to 0.4 μm and a gate positioned 0.5 μm from the source.

Table 3.3. Classification of gate-FP designs

Cases	Types of Gate-FP
a	Without-FP
b	Γ-FP
c	⅂-FP
d	T-FP
e	F-FP

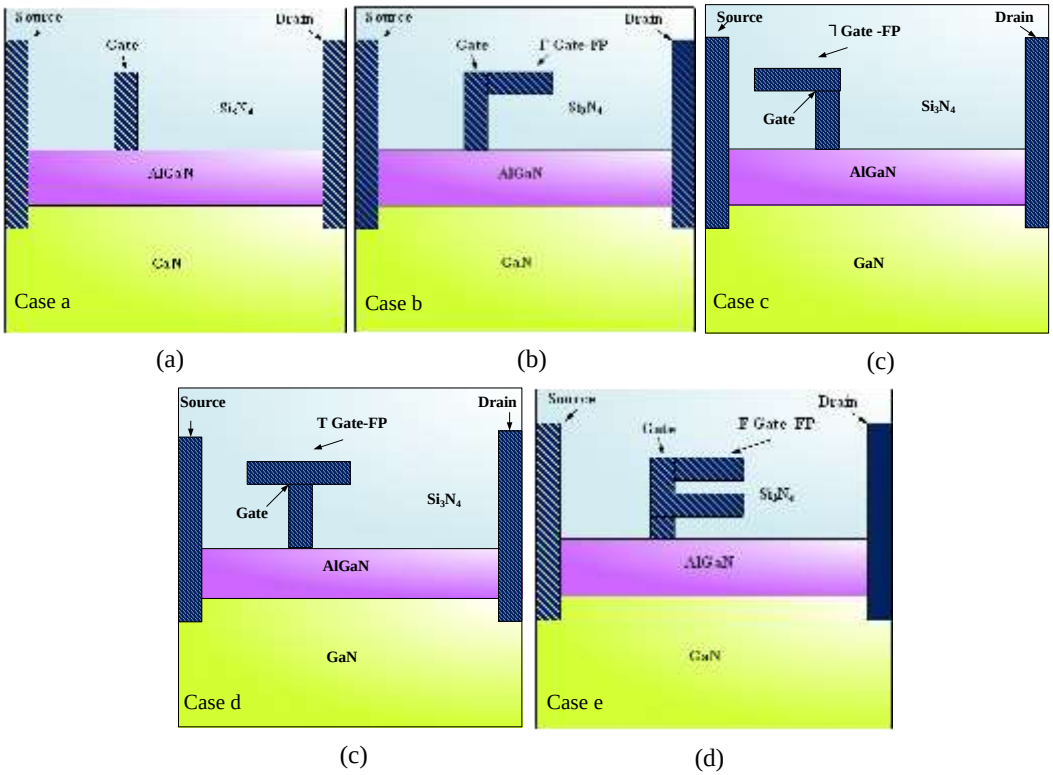


Fig. 3.5. Schematic cross-sections of various gate-FP AlGaN/GaN HEMT structures: (a) without-FP, (b) Γ-gate FP, (c) ⅂-gate FP, (d) T-gate FP, and (e) F-gate FP.

AlGaN/GaN HEMT with different gate-FP structures were simulated using Silvaco, and their electrical properties are presented in Fig. 3.6. The I_D-V_G characteristics were evaluated with a V_D of 0.1 V as the V_G was swept from -7 V to 2 V. Meanwhile, the I_D-V_D characteristics were simulated at a constant V_G of 0 V. The electrical characteristics of AlGaN/GaN HEMT devices with various 0.4 µm gate-FP configurations were systematically analysed and compared against a reference device

without-FP. The conventional without-FP structure exhibits a V_{th} of -2.298 V, I_{dmax} of 54 mA/mm, and I_{dss} of 1.298 A/mm. The maximum g_m shows minimal variation between 51.2-51.4 mS/mm regardless of FP geometry, indicating consistent small-signal amplification capability. V_{br} analysis demonstrates significant improvement with FP incorporation. While the without-FP and ㄱ-FP structures show identical V_{br} of 281 V, consistent with typical GaN HEMT performance limitations due to electric field concentration at the gate edge [228], other FP geometries exhibit substantial enhancement: Γ-FP and T-FP reach ~490 V, and the F-FP configuration achieves the highest V_{br} of 530 V. This improvement aligns with prior work demonstrating FP effectiveness in reducing peak electric fields [228]. The FP's superior performance is attributed to optimized field distribution, reducing intensity at critical points [227].

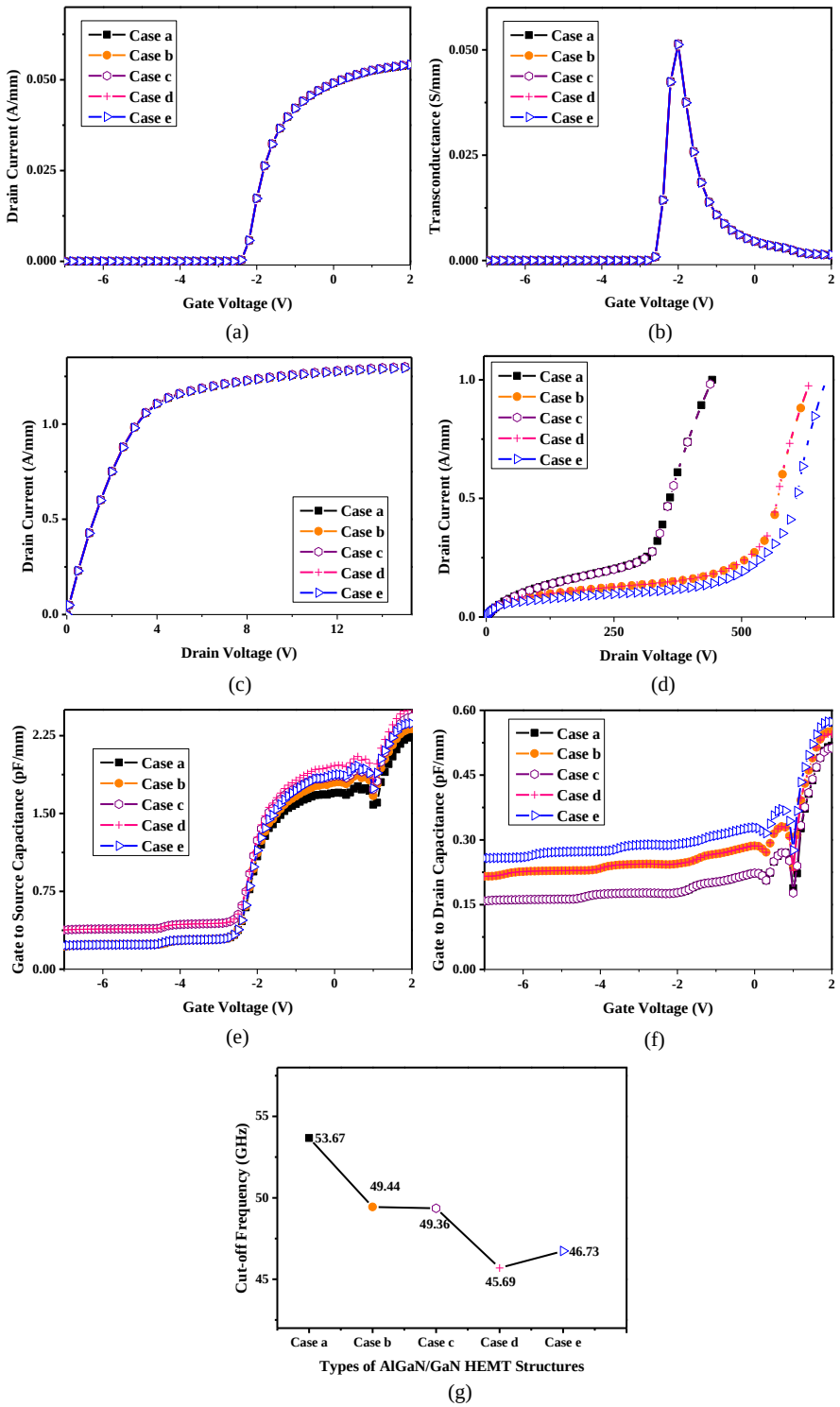


Fig. 3.6. AlGaN/GaN HEMTs with different gate-FP configurations: (a) I_D-V_G characteristics, (b) g_m, (c) I_D-V_D characteristics, (d) V_{br}, (e) C_{gs}, (f) C_{gd}, and (g) f_T.

This performance variation highlights that FP shape significantly impacts breakdown characteristics without substantially affecting other DC parameters. While the Γ-FP demonstrates a lower V_{br} compared to the F-FP, it exhibits superior f_T performance. Fig. 3.6(e)-(g) presents the AC characteristics (V_D = 8 V) for various gate-FP AlGaN/GaN HEMT structures. The AC analysis indicates that FP implementation moderately increases both C_{gs} and C_{gd} compared to the without-FP device (1.67 pF/mm and 0.21 pF/mm, respectively). Specifically, the Γ-shaped FP shows C_{gs} of 1.77 pF/mm and C_{gd} of 0.28 pF/mm; ⅂-shaped FP results in C_{gs} = 1.86 pF/mm and C_{gd} = 0.21 pF/mm; the more complex T-shaped FP demonstrates higher values with C_{gs} = 1.96 pF/mm and C_{gd} = 0.27 pF/mm; and the F-shaped FP shows C_{gs} = 1.84 pF/mm and C_{gd} = 0.32 pF/mm. This capacitance variations correlate with observed f_T trends, where the device without-FP achieves the highest f_T (53.67 GHz), with FP configurations showing a gradual reduction - Γ-FP at 49.44 GHz, ⅂-FP at 49.36 GHz, F-FP at 46.73 GHz and T-FP at 45.69 GHz. Capacitance (C_{gs} and C_{gd}) increased with the addition of FP, which could impact high-frequency performance due to the negative Miller feedback effect [229].

3.4 Single and Dual-FP Structures

In this section, single and dual-FP configurations, specifically Γ-type and F-type structures, are studied to evaluate their impact on breakdown and electrical characteristics. Seven structures (Fig. 3.7) are simulated, one featuring without-FP (Case I), single source Γ-type (Case II), single gate Γ-type (Case III), single source F-type (Case IV), single gate F-type (Case V), dual Γ-type (Case VI), and dual F-type (Case VII) FPs. The single-FP structure reduces the peak electric field at the gate edge, causing the electric field to concentrate at the FP-electrode edge instead. This occurs because of the thin Si_3N_4 film and the extended length of the FP electrode. Additionally, the high electric field at the FP-electrode edge accelerates electrons.

Conversely, the dual-FP structure enhances the uniformity of the electric-field distribution through its multistep design [227]. The single-FP structure with a gate-FP helps alleviate electric-field concentration. The gate-edge electric field peak in the

gate-FP design is marginally lower than that in the source-FP case, owing to the potential difference between the gate and FP electrodes. All device parameters align with those listed in Tables 3.1 and 3.2, except for the L_{FP}. In this configuration, the source-connected L_{FP} is set to 2.4 μm while the gate-connected L_{FP} is 0.9 μm.

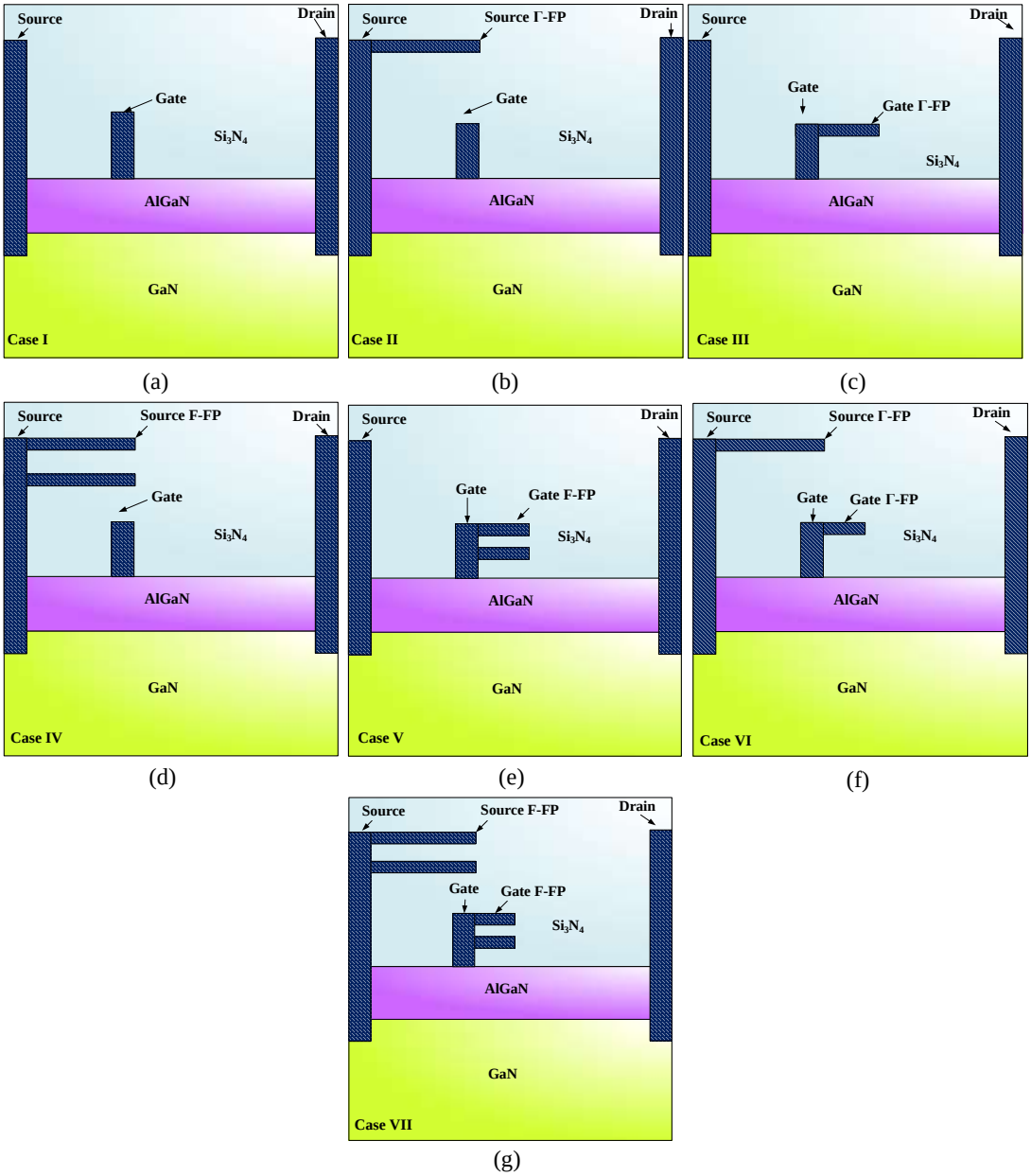
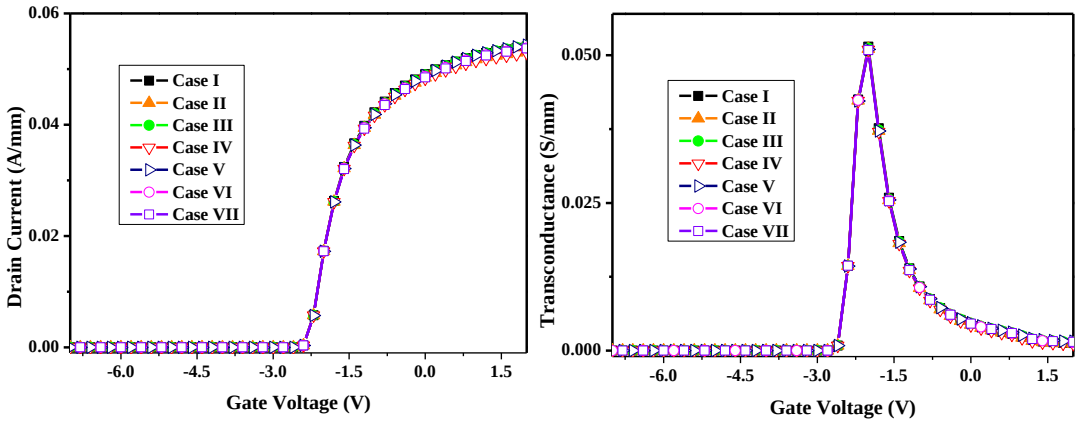


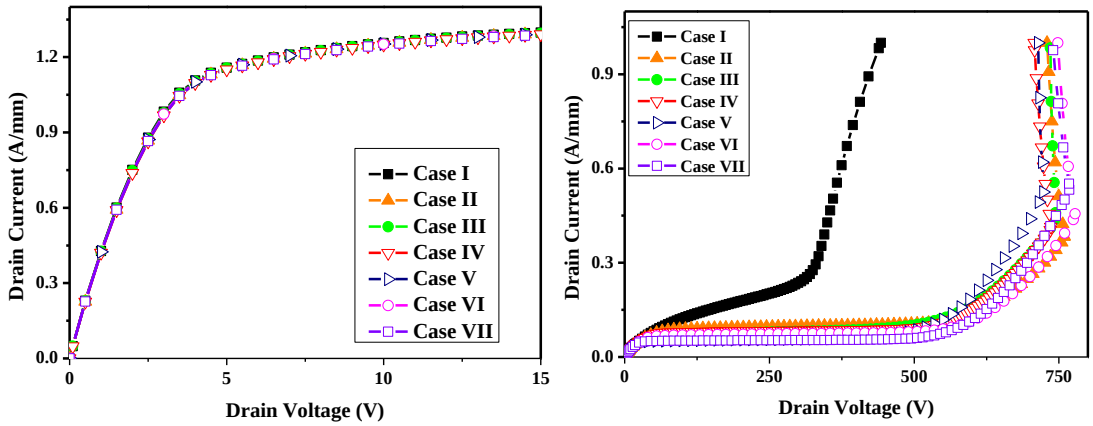
Fig. 3.7. Schematic cross-sections of AlGaN/GaN HEMTs with different FP designs: (a) without-FP (Case I), (b) single source Γ-FP (Case II), (c) single gate Γ-FP (Case III), (d) single source F-FP (Case IV), (e) single gate F-FP (Case V), (f) dual Γ-FP (gate & source) (Case VI), and (g) dual F-FP (gate & source) (Case VII).

This section presents a detailed electrical characterisation of AlGaN/GaN HEMT devices with various FP configurations, comparing seven different designs against a conventional without-FP structure (Case I). The I_D-V_G characteristics (Fig. 3.8) were evaluated with a V_D of 0.1 V. Simultaneously, the output characteristics were obtained at a fixed gate bias of 0 V. V_{th} is consistently maintained at -2.29 V (Fig. 3.8(a)) for all configurations, indicating that FP modifications preserve the fundamental turn-on characteristics.



(a) (b)

Fig. 3.8. Evaluation of (a) I_D-V_G characteristics (b) g_m in AlGaN/GaN HEMTs with different FP configurations.



(a) (b)

Fig. 3.9. Analysis of (a) I_D-V_D characteristics, (b) V_{br} in AlGaN/GaN HEMTs with different FP configurations.

The analysis reveals that while drain current characteristics remain remarkably consistent across all configurations - with I_{dss} (Fig. 3.9(a)) maintaining a narrow range of 1.287-1.298 A/mm and I_{dmax} varying only between 52-54 mA/mm

(Fig. 3.8(a)), the V_{br} shows significant variation depending on the FP geometry. The without-FP structure (Case I) demonstrates the lowest V_{br} at 281 V. At the same time, FP implementations show substantial improvements, particularly in dual-FP configurations where the dual F-FP HEMT (Case VII) achieves the highest V_{br} at 781 V (Fig. 3.9(b)). The g_m remains stable across all cases (50.8-51.4 mS/mm) (Fig. 3.8(b)), confirming that FP integration does not significantly impact small-signal gain.

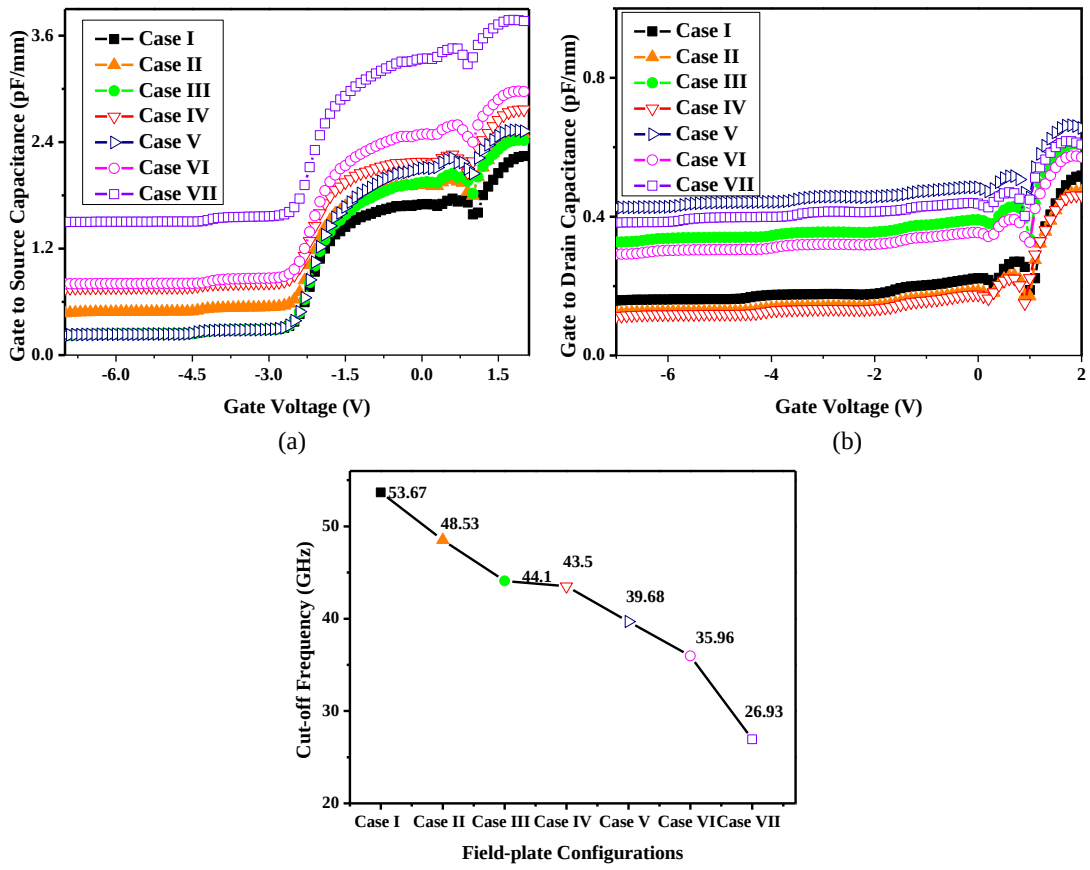


Fig. 3.10. Comparison of (a) C_{gs}, (b) C_{gd}, and (c) f_T for AlGaN/GaN HEMTs with different FP configurations.

At the 0.9 µm gate L_{FP}, results indicate the Γ-FP structure surpasses the single F-FP design in V_{br} capability, representing a performance inversion compared to the earlier findings in Section 3.3. This advantage can be attributed to the F-FP's more effective electric field distribution at minimal dimensions, where its extended horizontal section provides better field smoothing in the critical gate-drain access

region. The structure's ability to simultaneously modulate both vertical and lateral field components becomes particularly advantageous at smaller scales. However, as the FP extends to 0.9 μm, the Γ-FP regains its V_{br} superiority over the F-FP design. This crossover behaviour stems from fundamental differences in FP architecture: The Γ-FP's angled geometry enables more efficient field line termination across longer distances, the F-FP's horizontal extension at greater lengths may induce unwanted charge accumulation, and the Γ-FP maintains better control of the peak electric field location.

However, the capacitance characteristics and frequency response at V_D = 8 V show notable variations, with C_{gs} increasing from 1.67 pF/mm in the without-FP device to 3.30 pF/mm in the dual F-FP configuration (Fig. 3.10(a)). At the same time, f_T decreases correspondingly from 53.67 GHz to 26.93 GHz (Fig. 3.10(c)), highlighting the trade-off between breakdown performance and high-frequency operation that must be considered in FP design optimisation. Based on the analysis of V_{br} and f_T, the dual F-FP HEMT (Case VII) exhibits the highest V_{br} (781 V), making it the most suitable for high-voltage applications. However, it has the lowest f_T (26.93 GHz), indicating a trade-off between voltage robustness and high-frequency performance. In contrast, the conventional HEMT without-FP (Case I) achieves the highest f_T (53.67 GHz) but the lowest V_{br} (281 V), making it better for high-speed, low-voltage applications. The Γ-FP configurations (Cases II, III, and V) offer a balanced compromise, with significantly improved V_{br} (up to 761 V) while maintaining relatively higher f_T (above 39 GHz). Thus, the choice of FP structure depends on the application requirements—dual F-FP for high-voltage endurance, conventional HEMT for high-frequency operation, and Γ-FP designs for a moderate balance of both.

3.5 Innovative Gate-FP Structures with High-*k* Passivation

The use of a metal FP has previously been studied as a technique to increase V_{br} [111], [228]. It is widely recognised that incorporating an FP improves the power performance of AlGaN/GaN HEMTs [8], [230]. Another approach to enhancing V_{br} is the application of a high-*k* passivation layer. Experimental research [231] has

demonstrated that devices passivated with Si_3N_4 exhibit higher V_{br} compared to non-passivated ones. The passivation layer serves two primary purposes: shielding the device's top layer from external factors and minimising the peak electric field concentration near the drain-side gate edge [229]. In AlGaN/GaN HEMTs, a high-*k* passivation layer is employed to boost the V_{br} [232], as it effectively moderates the electric field distribution between the gate and drain. This section investigates advanced gate-FP configurations and examines their potential for further optimisation of electrical characteristics, particularly V_{br} and f_T. All device parameters remain consistent with the specifications in Tables 3.1 and 3.2, with the exception of L_{FP}. In all configurations, the FP thickness is kept constant at 0.02 μm, with the right-side FP measuring 0.9 μm in length and the left-side FP measuring 0.4 μm. All physical models employed in the simulation remain unchanged from those detailed in Section 3.2 of the study. Here, the passivation material used is a high-*k* dielectric, HfO_2. With a higher dielectric constant (*k*), the electric field distribution at the drain-side gate edge becomes more uniform, thereby lowering the impact ionisation rate. Devices with high-*k* passivation demonstrate an improved breakdown performance compared to those with low-*k* passivation [233].

Fig. 3.11 illustrates cross-sectional schematics of AlGaN/GaN HEMTs featuring various FP configurations: (i) the baseline structure without-FP (Case A), (ii) Γ-FP (Case B), (iii) F-FP (Case C), (iv) inverted F-FP (Case D), (v) inverted T-FP (Case E), (vi) step-FP (Case F), (vii) floating T-FP (Case G), (viii) T-FP (Case H), (ix) double F-FP (Case I), (x) staircase-FP (Case J), and (xi) double-deck FP (Case K). Each configuration is clearly labelled (Cases A-K) to facilitate direct comparison of its structural differences. The schematic representation enables visualisation of key dimensional variations in the FP extensions, including their protrusion lengths, vertical

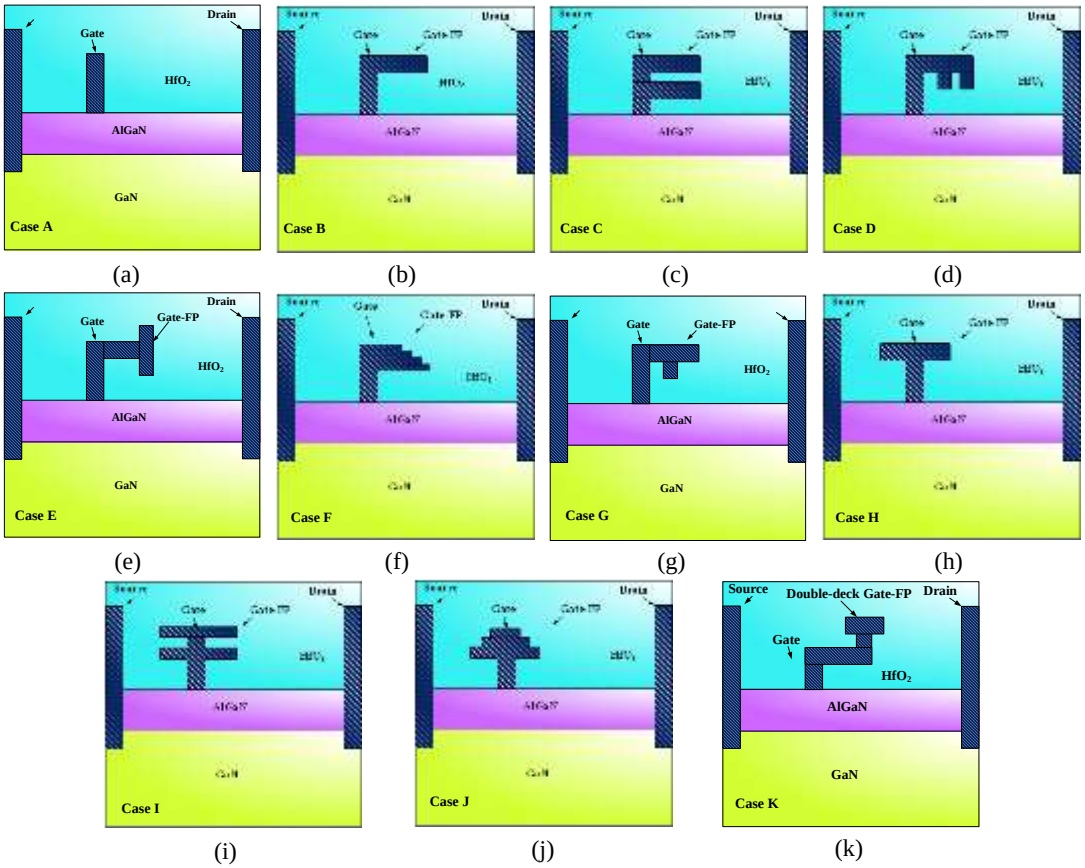
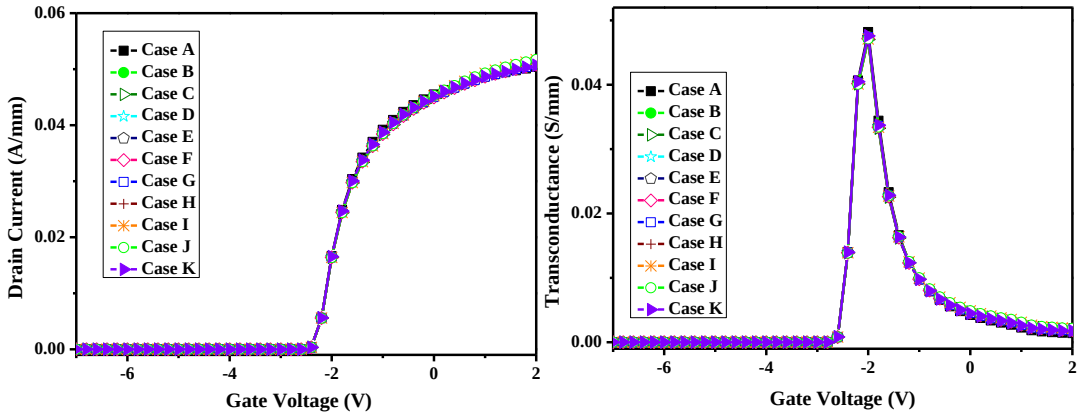


Fig. 3.11. Schematic cross-sections of AlGaN/GaN HEMTs with different FP designs: (a) without-FP (Case A), (b) Γ-FP (Case B), (c) F-FP (Case C), (d) inverted F-FP (Case D), (e) inverted T-FP (Case E), (f) step-FP (Case F), (g) floating T-FP (Case G), (h) T-FP (Case H), (i) double F-FP (Case I), (j) staircase -FP (Case J) and, (k) double-deck FP.

stacking arrangements, and connection points relative to the gate electrode. Simulations were conducted on AlGaN/GaN HEMTs featuring different gate-FP configurations, and their results were analysed. Moreover, the conventional Si_3N_4 passivation layer is substituted with a high-*k* HfO_2 in this section. Fig. 3.12(a) displays the I_D-V_G characteristics across a V_G of -7 V to 2 V at a V_D of 0.1 V. Interestingly, all FP configurations maintain an identical V_{th} of -2.30 V, confirming that the FP modifications do not alter the basic turn-on characteristics of the devices. The negative V_{th} indicates that the device operates in a Normally-On state (depletion-mode HEMT), as the heterointerface and the 2DEG channel exhibit strong polarisation effects. The analysis of drain current characteristics reveals remarkable

consistency across all FP configurations. The I_{dmax} maintains exceptional stability, ranging narrowly between 50 and 51 mA/mm for all cases, demonstrating that FP implementation does not significantly impact the peak current-carrying capability of the devices.



(a) (b)

Fig. 3.12. Evaluation of (a) I_D-V_G characteristics, and (d) g_m for AlGaN/GaN HEMTs featuring different gate-FP designs and a high-*k* passivation layer.

g_m performance follows a similar pattern of consistency, with all configurations maintaining values between 47 and 48.1 mS/mm (Fig. 3.12(b)). The without-FP device (Case A) shows the highest g_m of 48.1 mS/mm, while most FP implementations cluster around 47.1-47.5 mS/mm. This marginal reduction in g_m for field-plated devices may be attributed to the slight increase in access resistance or changes in electric field distribution introduced by the FP structures. The Γ-FP configuration (Case B) demonstrates comparable g_m performance to the without-FP device at 47.4 mS/mm, suggesting that certain FP geometries can maintain excellent small-signal gain characteristics while providing other performance benefits.

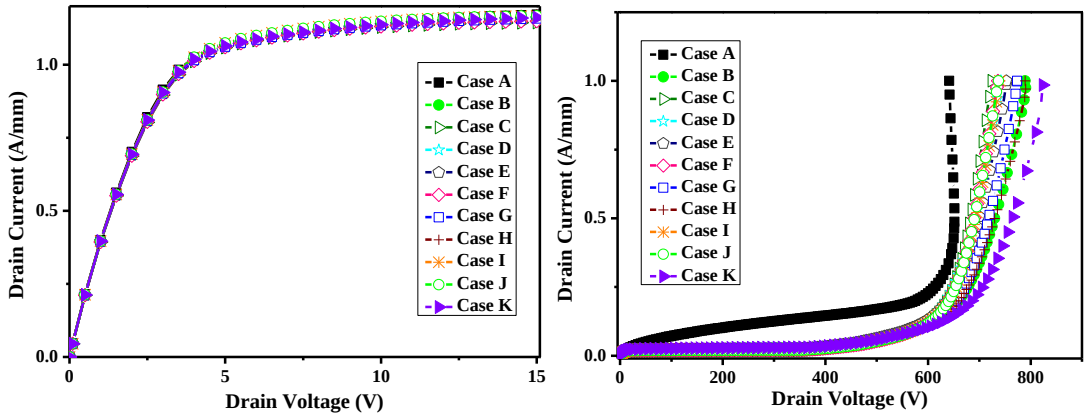


Fig. 3.13. Comparison of (a) I_D-V_D characteristics, and (b) V_{br}, for AlGaN/GaN HEMTs featuring different gate-FP designs and a high-*k* passivation layer.

Additionally, Fig. 3.13(a) illustrates the standard I_D-V_D characteristics for various gate-FP designs with a 0.5 µm L_G, where the V_D is swept from 0 V to 15 V under a V_G of 0 V. I_{dss} shows slightly more variation, with values spanning from 1.14 to 1.17 A/mm, where the T-FP (Case H) and without-FP structure (Case A) exhibit the highest I_{dss} values of 1.17 A/mm. This minor variation in I_{dss} suggests that while FPs introduce structural modifications, they have minimal effect on the channel's maximum electron density and carrier transport properties. V_{br} (Fig. 3.13(b)) shows more significant variation between the different FP designs. The double-deck gate-FP structure (Case K) demonstrates the highest V_{br} at 788 V, closely followed by the T-FP (Case H) at 777 V and the Γ-FP configuration (Case B) at 762 V, representing substantial improvements over the reference device without-FP (Case A), which shows 647 V.

However, these improvements come with trade-offs in frequency response and capacitance characteristics. The AC analysis, performed at V_D = 8 V, reveals clear trends in capacitance behaviour that depend on the complexity of the FP. Both C_{gs} (Fig. 3.14(a)) and C_{gd} (Fig. 3.14(b)) generally increase with more elaborate FP designs, with the double F-FP structure (Case I) showing the highest value of C_{gs} at 3.54 pF/mm. The without-FP device (Case A) exhibits the lowest capacitances at 1.95 pF/mm (C_{gs}) and 0.33 pF/mm (C_{gd}). Frequency performance (Fig. 3.14(c))

shows an interesting trade-off, where the without-FP configuration (Case A) achieves the highest f_T = 40.06 GHz, while more complex designs tend to reduce this parameter. The double-deck FP (Case K) structure yields the second-highest f_T (28.59 GHz), ranking just above the Γ-FP (27.50 GHz). A higher f_T indicates a greater switching speed, making it an excellent choice for high-speed applications. However, adding an FP raises capacitance, which can impact the device's switching performance. This shows that the FP modifications do not compromise the gate insulation properties. This chapter establishes that careful optimisation of FP design can enhance breakdown characteristics without significantly compromising DC performance. Moreover, the use of an HfO2 passivation layer enhances V_{br} but at the cost of increased capacitance, which lowers the f_T.

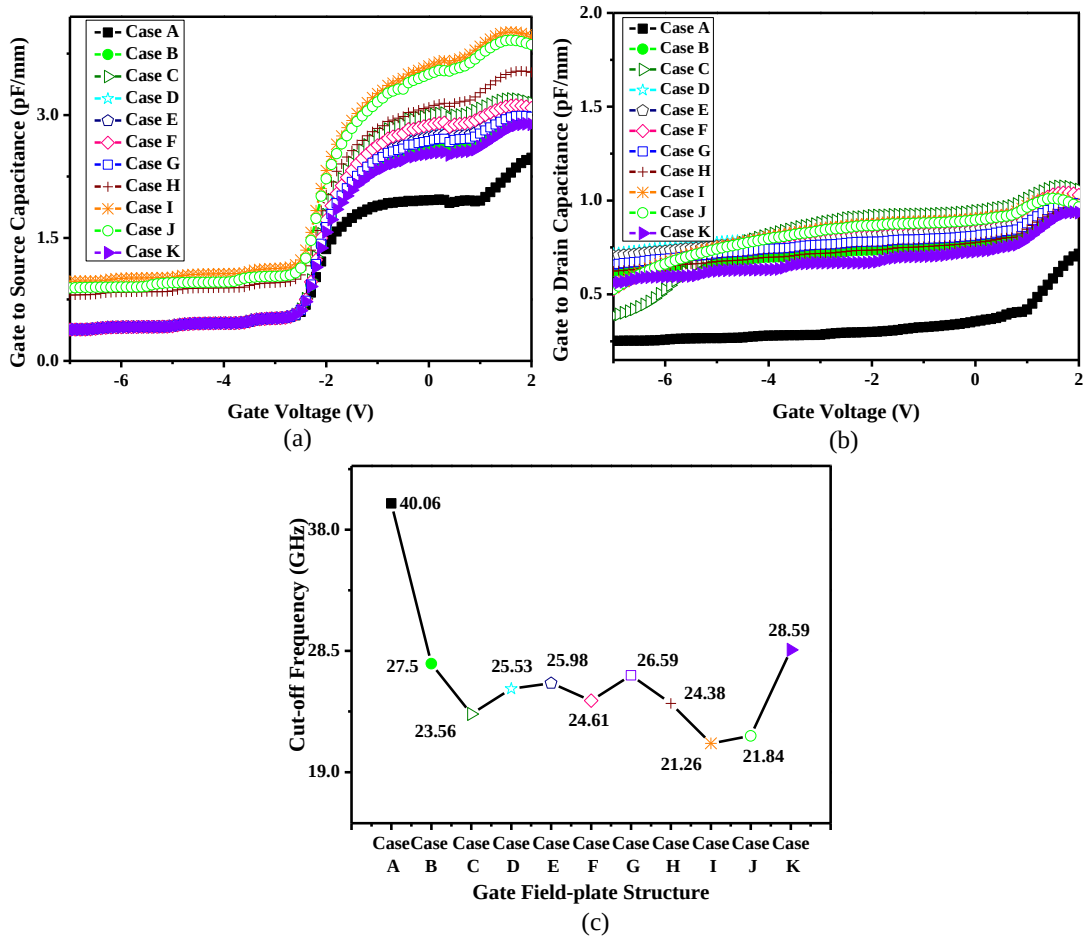


Fig. 3.14. Comparison of (a) C_{gs}, (b) C_{gd}, and (c) f_T for AlGaN/GaN HEMTs featuring different gate-FP designs and a high-*k* passivation.

Table 3.4. Comparison of electrical parameters for different gate structures (Cases A–K)

Case	I_{dss} (A/mm)	g_m (mS/mm)	V_{br} (V)	V_{th} (V)	C_{gs} (pF/mm)	C_{gd} (pF/mm)	f_T (GHz)
A	1.17	48.1	647	-2.301	1.95	0.33	40.06
B	1.15	47.4	762	-2.302	2.56	0.76	27.50
C	1.14	47	647	-2.302	2.94	0.93	23.56
D	1.15	47.2	661	-2.302	2.72	0.85	25.53
E	1.15	47.3	677	-2.302	2.68	0.83	25.98
F	1.14	47.1	652	-2.302	2.82	0.88	24.61
G	1.15	47.4	712	-2.302	2.63	0.80	26.59
H	1.17	47.4	777	-2.302	3.06	0.77	24.38
I	1.16	47.1	654	-2.302	3.54	0.89	21.26
J	1.16	47.1	652	-2.302	3.44	0.89	21.84
K	1.16	47.5	788	-2.302	2.48	0.71	28.59

Table 3.4 summarises the key electrical performance of the device for Cases A through K. It should be noted that the DC parameters were evaluated at V_D = 0.1, while the AC parameters were extracted under small-signal conditions at V_D = 8 V. From the comparison of all FP structures, it is observed that Case H, i.e. T-FP and Case K, i.e. double-deck FP, yield the highest V_{br}. As shown in Table 4, both of them exhibit nearly identical I_{dss} (1.17 vs. 1.16 A/mm) and I_{dmax} (51 vs. 50 mA/mm), indicating similar current-handling capability. The g_m also shows negligible variation (47.5 vs. 47.6 mS/mm). The V_{th} remains identical at –2.302 V. In terms of f_T, Case K exhibits a higher f_T than Case H mainly due to its lower parasitic capacitances. Specifically, both C_{gs} and C_{gd} are reduced in Case K (2.48 vs. 3.06 pF/mm and 0.71 vs. 0.77 pF/mm, respectively). The reduction in capacitances lowers the total input capacitance without significantly altering g_m, which remains nearly the same for both cases. This leads to faster charging/discharging of the gate, enabling higher frequency operation. Therefore, the improved electrostatic design of Case K reduces

parasitic effects, resulting in enhanced high-frequency performance compared to the T-FP.

The Case K achieves a marginally higher V_{br} of 788 V compared to 777 V for the Case H, indicating a more favourable electric field distribution. The electric field distributions (Fig. 3.15) of the two structures reveal distinct differences in peak field localisation and spreading. In the first structure (Case H), a sharper and more concentrated peak is observed at the gate edge, indicating stronger field crowding. This results in a higher local electric field, which can reduce the V_{br} and increase reliability concerns due to hot-carrier effects. In contrast, the second structure (Case K) demonstrates a more uniform electric field profile, with the peak electric field effectively suppressed and redistributed toward the drain side. This reduction in peak

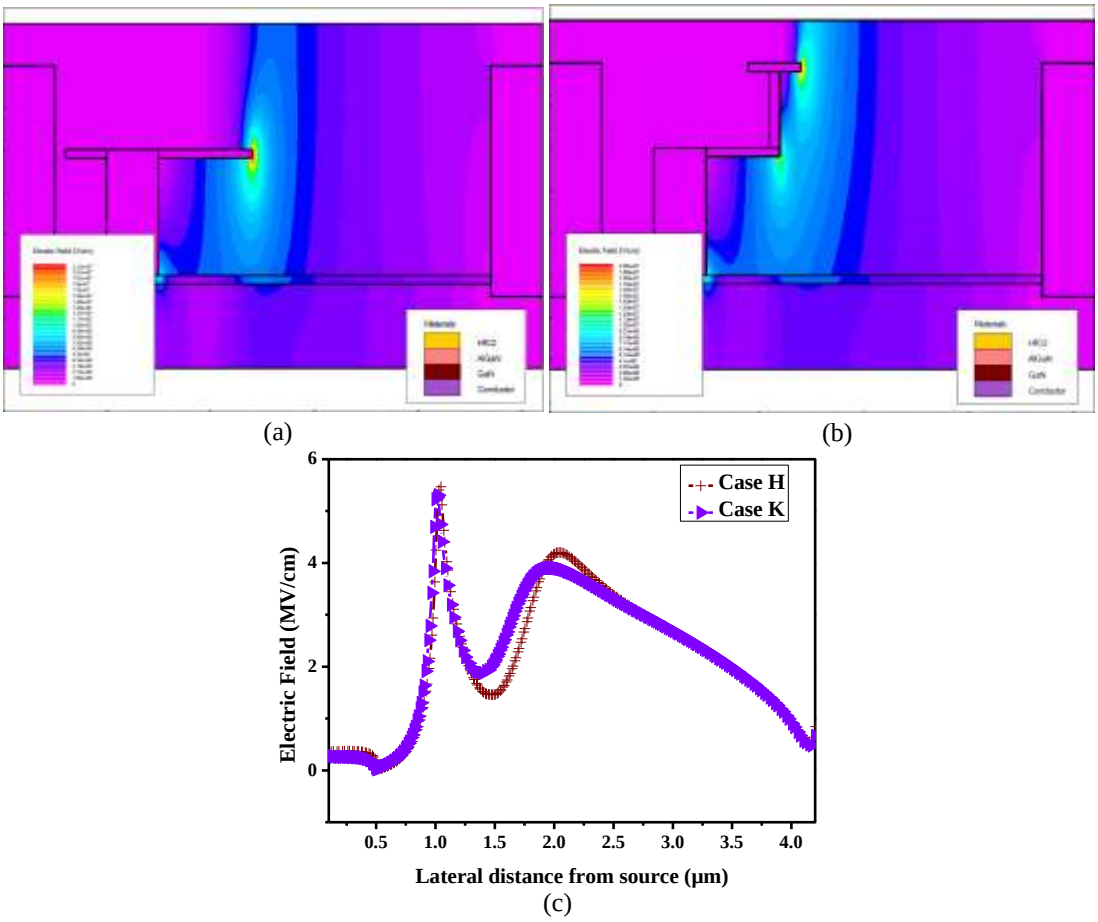


Fig. 3.15. Electric field contour plots and lateral distribution for Case H and Case K. (a) Case H exhibits a sharp peak concentrated at the gate edge. (b) Case K

demonstrates suppressed and more uniformly distributed fields. (c) The lateral profile confirms reduced peak field intensity and smoother distribution in Case K, leading to improved V_{br} and device reliability.

intensity minimises field crowding at the gate edge, thereby enhancing V_{br} and improving device robustness. The lateral electric field plot further confirms these observations. Case H exhibits a pronounced field spike near the gate edge, whereas Case K significantly reduces this peak, resulting in a smoother field distribution across the channel length. This redistribution lowers the peak field in Case K and improves field balancing along the lateral distance, which directly contributes to higher V_{br} and improved reliability in Case K. Among the simulated structures, Case K exhibits comparatively better performance metrics than Case H, particularly in terms of V_{br}, capacitances, and f_T. Therefore, for detailed analysis and further optimisation, the subsequent investigation in this work is primarily concentrated on Case K (double-deck FP).

3.6 Summary

This comprehensive study of FP configurations in AlGaN/GaN HEMTs has yielded several critical insights into device optimisation for power electronics applications. The evaluation of FP positioning demonstrates that gate-connected configurations consistently achieve superior V_{br} compared to their source-connected counterparts for the same FP length. In contrast, single drain-connected FP prove largely ineffective for V_{br} enhancement. This finding underscores the importance of strategic FP placement, particularly near the gate region where electric field crowding is most severe. Among the various gate-FP geometries examined, the T-FP and double deck gate-FP structures emerge as particularly promising designs, delivering the most significant improvements in breakdown characteristics. However, these configurations present distinct trade-offs — while the T and double-deck gate-FP achieves higher V_{br}, it suffers from increased capacitance and consequently reduced f_T compared to the Γ-FP. This performance dichotomy highlights the fundamental compromise between voltage robustness and high-frequency operation in field-plated devices.

The research further reveals that while extending FP length initially boosts V_{br}, this benefit saturates once the plate sufficiently covers the high-field region. This saturation effect provides practical guidance for device design, suggesting that FPs need only extend to the point of complete high-field coverage. Additionally, the incorporation of HfO_2 passivation proves highly effective, not only enhancing V_{br} through electric field profile smoothing but also mitigating impact ionization effects. The study of dual FP configurations demonstrates their advantage over single FP designs, as the dual arrangement promotes more uniform electric field distribution across the device. While FPs undeniably improve breakdown performance, their impact on high-frequency characteristics cannot be overlooked. The inherent capacitance introduced by these structures inevitably degrades f_T, presenting a fundamental limitation that must be carefully managed in RF applications. These findings collectively provide a framework for optimizing FP designs, balancing the competing demands of voltage handling, frequency response, and overall device reliability in next-generation power electronics. Thorough analysis reveals that the double-deck gate-FP structure demonstrates superior performance metrics compared to the T-FP, especially with respect to V_{br}, and f_T.

CHAPTER 4

Effect of Passivation Layers on Electrical Characteristics of AlGaN/GaN HEMT

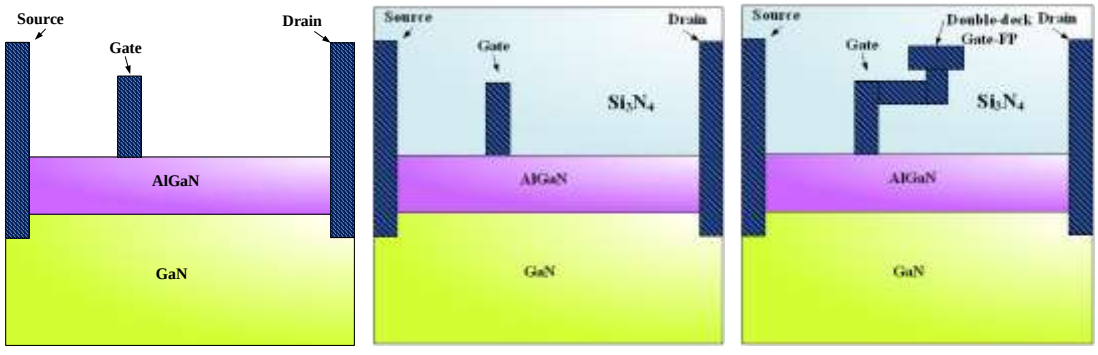
4.1. Introduction

The Passivation layer plays a critical role in AlGaN/GaN HEMTs by both protecting the device surface from environmental influences and reducing the intense electric-field crowding near the drain-side gate edge. In the previous chapter, the role of field plates (FPs) in enhancing the breakdown voltage (V_{br}) was examined, showing that while FPs effectively redistribute the electric field, they also increase parasitic capacitance and degrade RF performance. To overcome such limitations, this chapter investigates passivation strategies, which not only protect the device surface but also suppress peak electric fields at the gate–drain interface, thereby offering a pathway to improved breakdown and reliability [234]. A smoother drain current improves V_{br}, and passivation enhances V_{br} without degrading device performance. Recent research has extensively explored GaN-based HEMTs, including the impact of dielectric passivation layers [235]. The effectiveness of passivation in AlGaN/GaN HEMTs strongly depends on the choice of dielectric material, as it directly influences interface quality, surface state density, and parasitic capacitances. Si_3N_4 has been widely employed due to its excellent surface coverage, compatibility with existing processes, and its proven ability to suppress current collapse [231]. However, the relatively low dielectric constant (k) of Si_3N_4 limits its capability for electric field modulation. To address this, high-k dielectrics such as aluminium oxide (Al_2O_3) [236], hafnium silicate ($HfSiO_4$) [237], hafnium oxide (HfO_2) [238] etc. have been investigated. Although traditional passivation materials like Si_3N_4, Al_2O_3, and Hf-based oxides are well-established for AlGaN/GaN HEMT devices, SnO_2 has not yet been reported in that application context. Nonetheless, SnO_2 possesses a wide bandgap, a relatively high k, and robust chemical stability—attributes that are desirable for surface passivation. Previous works in SnO_2-based MOSFETs, thin-film transistors, and oxide electronics demonstrate its electrical resilience and film quality, making it a promising, though underexplored, candidate

for passivation in GaN HEMTs [239]-[240]. The double-deck gate-FP structure is adopted here as it offers superior V_{br} and cut-off frequency (f_T) compared to conventional FPs, as discussed in Chapter 3. By splitting and redistributing the electric field, this dual-layer design reduces peak intensity while preserving low on-resistance (R_{on}), thus achieving better overall performance than earlier single-FP approaches. This chapter analyses AlGaN/GaN HEMTs in various configurations—unpassivated, passivated (with and without double-deck gate-FP)—and also evaluates the impact of dual passivation layers on the electrical characteristics of AlGaN/GaN HEMTs.

4.2 Impact of Passivation on Device Performance

Fig. 4.1 illustrates the schematic cross-sections of the unpassivated device (without-FP) and passivated structures (with/without double-deck gate-FP). All device parameters stay the same as those listed in Tables 3.1 and 3.2, and the FP length (L_{FP}), is fixed to 0.9 µm. The heterostructure uses a 0.02 µm AlGaN barrier on a 0.2 µm GaN buffer to form the 2DEG channel, with an Al mole fraction of 0.23. A 0.6 µm passivation layer is applied in the access region, and the physics models and calibration follow Section 3.2.



(a) (b) (c)

Fig. 4.1. AlGaN/GaN HEMT device structure (a) with no passivation layer, (b) Si_3N_4 passivated, and (c) Si_3N_4 passivated with a double-deck gate-FP.

Simulations were performed on three configurations: (i) a baseline structure without passivation or FP, (ii) a Si_3N_4-passivated structure without FP, and (iii) a structure incorporating both FP and passivation, to evaluate their impact on device performance. Fig. 4.2(a) shows the transfer (I_D–V_G) characteristics at drain

voltage (V_D) = 0.1 V, while Fig. 4.2(b) presents the output (I_D–V_D) characteristics of unpassivated and passivated devices (0.5 µm gate length) at gate voltage (V_G) = 0 V. The threshold voltage (V_{th}) remains nearly the same across all configurations, ranging from -2.298 V to -2.299 V, indicating minimal impact from passivation or the FP.

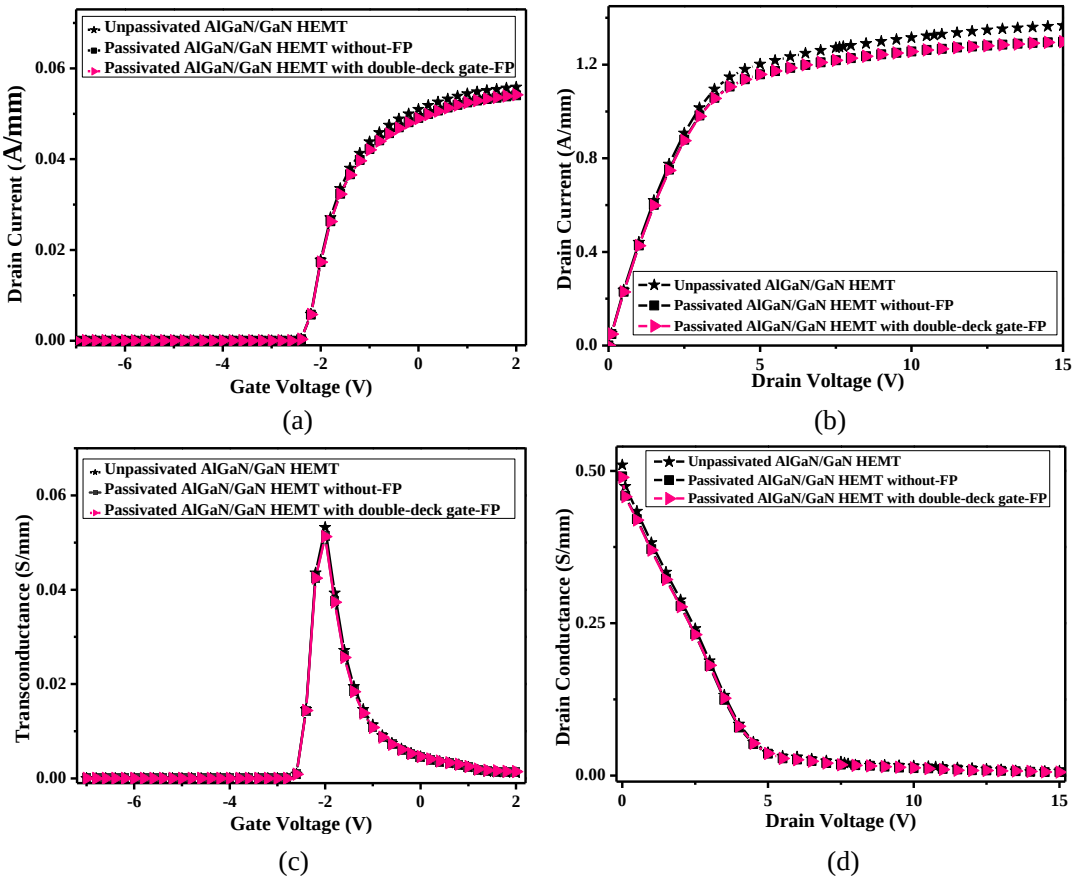


Fig. 4.2. Electrical characteristics of AlGaN/GaN HEMT: (a) I_D-V_G, (b) I_D-V_D, (c) g_m vs. V_G, and (d) g_{ds} vs. V_D —compared across three configurations: unpassivated, Si_3N_4-passivated, and Si_3N_4-passivated with an FP.

Fig. 4.2(c) and (d) display the transconductance (g_m) and drain conductance (g_{ds}), respectively, as functions of V_G and V_D. However, the g_m and maximum drain current (I_{dmax}) show slight reductions when passivation is applied, decreasing from 53.23 mS/mm and 55 mA/mm (unpassivated) to 51.25 mS/mm and 54 mA/mm (passivated with FP). The drain saturation current (I_{dss}) also follows a similar trend, dropping from 1.367 A/mm (unpassivated) to 1.297 A/mm (passivated with FP) (Fig.

4.2(b)). To investigate the V_{br} enhancement, the electric field distribution in the simulated devices was analysed using TCAD. Without passivation (Fig. 4.3(a)), the electric field is highly localized, creating peak intensities that induce premature breakdown. With Si_3N_4 passivation (Fig. 4.3(b)), the field becomes more uniform, lowering peak field strength and improving V_{br}. This improvement is attributed to the Si_3N_4 layer's ability to suppress surface states and reduce field crowding in critical regions. The incorporation of an FP (Fig. 4.3(c)) further optimizes breakdown performance by evenly spreading the electric field, particularly near the gate and drain edges, preventing localized breakdown. The combination of Si_3N_4 passivation and the FP results in superior device robustness, as confirmed by the field distribution analysis.

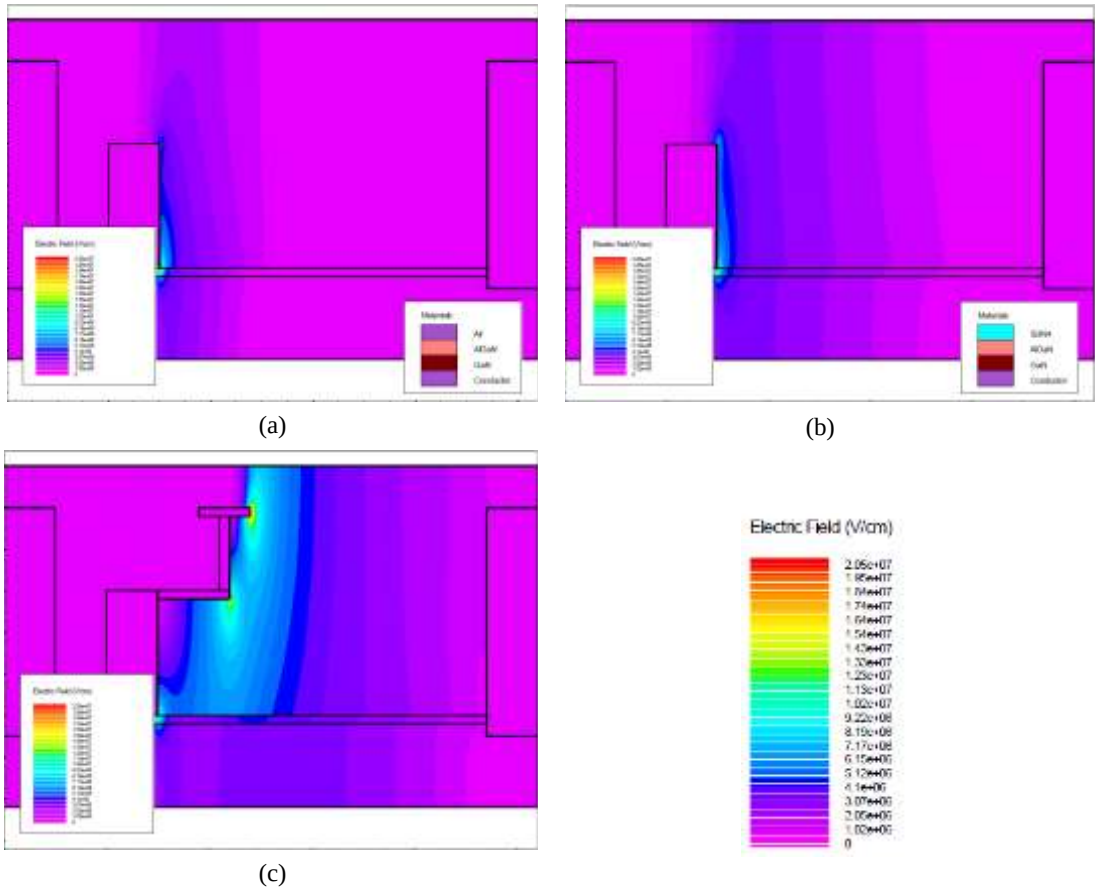
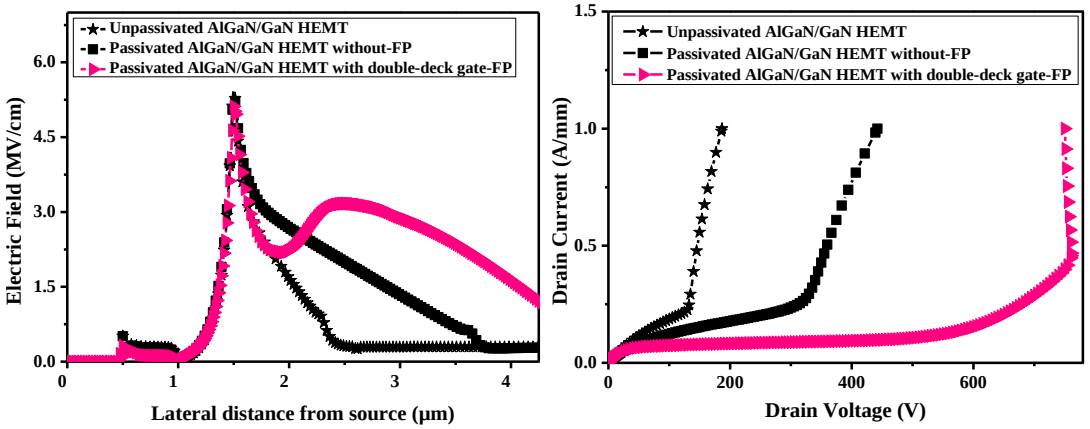


Fig. 4.3. Electric field profile in the AlGaN/GaN HEMT (a) unpassivated, (b) Si_3N_4 passivated, and (c) Si_3N_4 passivated with FP.

Fig. 4.4(a) compares the simulated electric field distribution for unpassivated and passivated structures (with and without-FP). The passivated device exhibits a

reduced peak electric field near the gate edge. Fig. 4.4(b) presents the breakdown characteristics, where passivation improves V_{br} by suppressing the electric field at the gate's drain side, whereas the unpassivated device exhibits a significantly lower V_{br}. Introducing both a passivation layer and an FP significantly improved the breakdown performance. The addition of an FP further suppresses the peak field, leading to an additional V_{br} enhancement. The V_{br} dramatically increases from 135 V (unpassivated) to 281 V (Si_3N_4 passivated without-FP) and further to 751 V (with-FP), highlighting the FP's effectiveness in enhancing device robustness.



(a) (b)

Fig. 4.4. (a) Spatial electric field variation and (b) V_{br} performance for an AlGaN/GaN HEMT under three conditions: unpassivated, Si_3N_4 passivated, and Si_3N_4 passivated with an FP.

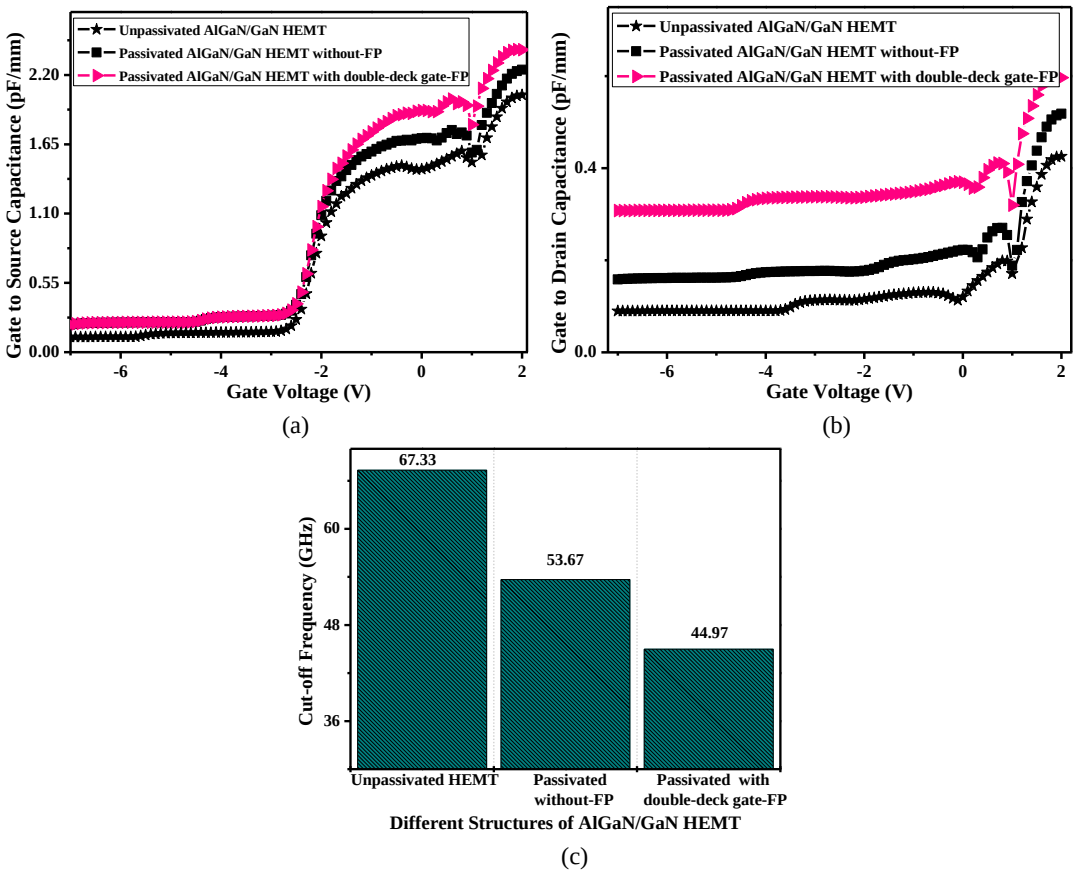


Fig. 4.5. Comparison of (a) C_{gs} vs $V_{G,}$ (b) C_{gd} vs $V_{G,}$ and (c) f_T for three device configurations: unpassivated, Si_3N_4 passivated, and Si_3N_4 passivated with an FP.

The AC analysis of various HEMT configurations was carried out at V_D = 8 V. Fig. 4.5(a) and (b) compare the gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances for three device configurations, showing higher values in passivated HEMTs and further increases with FP addition. Since these capacitances strongly influenced f_T, the passivated device shows degraded f_T performance, as illustrated in Fig. 4.5(c). These trade-offs suggest that while passivation and FP improve breakdown characteristics, they slightly degrade high-frequency performance due to increased capacitance.

4.3 Impact of Different Passivation Materials on AlGaN/GaN HEMT

While the previous section highlighted the general benefits of passivation, the choice of dielectric material plays a crucial role in determining device behaviour. This section, therefore, compares commonly used materials such as SiO_2, Si_3N_4, and

Al_2O_3, along with high-k oxides including $HfSiO_4$, HfO_2, and the less explored SnO_2, to assess their relative effectiveness in GaN HEMTs. For this purpose, a double-deck gate-FP AlGaN/GaN HEMT was analysed with different passivation materials, each implemented at a fixed thickness of 0.6 µm.

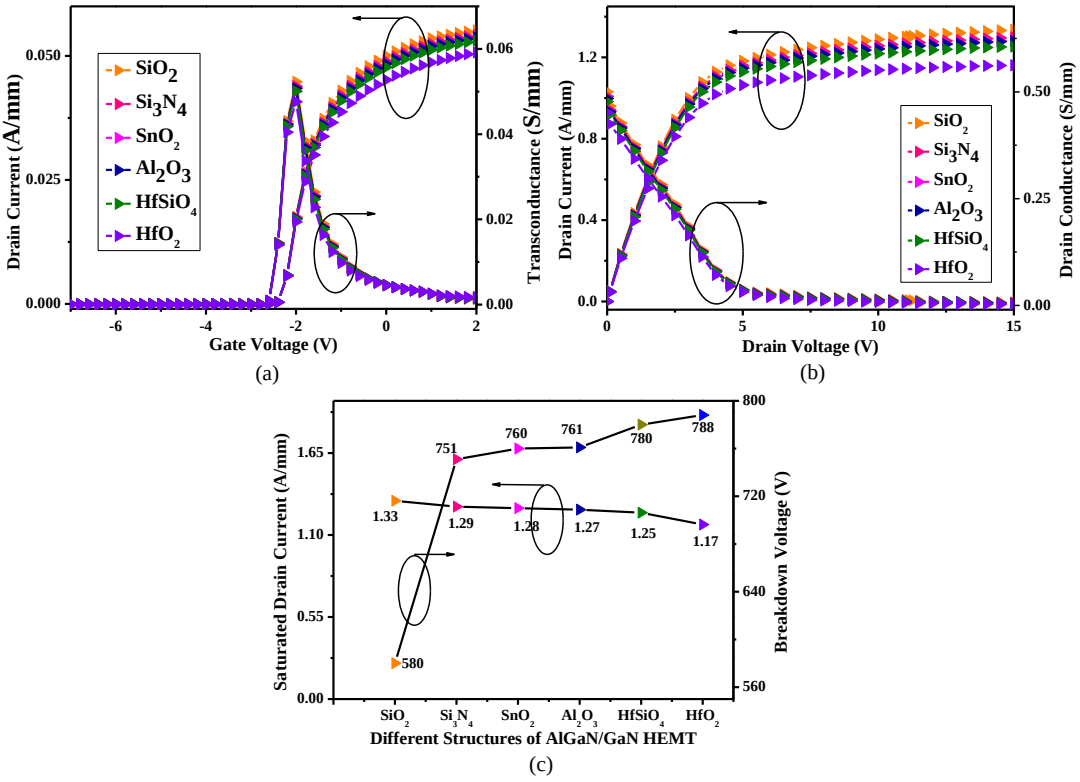


Fig. 4.6. Impact of passivation materials on (a) I_D-V_G characteristics, (b) I_D-V_D characteristics, and (c) I_{dss} and V_{br}.

The I_D–V_G characteristics (Fig. 4.6(a)) were obtained at a low drain bias of V_D = 0.1 V in order to accurately determine the V_{th} and g_m behavior without significant influence of channel-length modulation. Among the dielectrics used, SiO_2 passivation yielded the highest g_m (52.2 mS/mm), while HfO_2 exhibited the lowest (48 mS/mm). From this analysis, the peak g_m was identified at V_G = -2 V**.** Using the linear extrapolation method on the I_D–V_G characteristics, V_{th} values ranged from −2.29 V to −2.30 V. The V_{th} remains relatively stable but shifts slightly more negative, implying minor changes in charge trapping or interface effects. The negative V_{th} confirms normally-ON (D-mode) operation, attributed to strong polarization-induced 2DEG formation at the heterointerface. Fig. 4.6(b) shows the

I_D-V_D characteristics of double-deck gate-FP AlGaN/GaN HEMT with various passivation materials at $V_G = 0$ V. The SiO_2-passivated device exhibits the highest I_{dss} due to its low k, which minimizes parasitic capacitance, though it provides weaker field modulation. As the k of the passivation material increases, a reduction in I_{dss} is observed, as shown in Fig. 4.6(c), which also presents the variation in V_{br} across different materials. The enhancement in V_{br} correlates with the k of the passivation material—higher k reduces the electric field near the gate-drain edge, thereby increasing V_{br}. Additionally, under more negative V_G, V_{br} further improves in high-k regions due to suppressed buffer leakage current [241]. In these cases, impact ionization governs the breakdown mechanism rather than leakage current limitations. Consequently, high-k passivation materials deliver superior V_{br} compared to low-k alternatives. Among these dielectrics, HfO_2 exhibits the highest V_{br} (788 V), whereas SiO_2 demonstrates the lowest (580 V).

Further simulations were carried out at a higher drain bias of $V_D = 8$ V (Fig. 4.7(a)) to evaluate the RF characteristics. Fig. 4.7(b) and (c) compare the C_{gs} and C_{gd} for these device configurations. Both C_{gs} and C_{gd} increase with the k, attributed to stronger fringing fields in high-k passivation layers [242]. Consequently, SiO_2, with its lower permittivity, exhibits the lowest C_{gs} of 1.68 pF/mm, while HfO_2, having a higher permittivity, shows the highest C_{gs} of 2.40 pF/mm (Fig. 4.7(b)). The f_T can be defined as Eq. (4.1), where C_{gg} is the total gate capacitance. The f_T, representing the unity-current-gain frequency, serves as a critical metric for evaluating RF device performance. Among the simulated structures, the HEMT device without any passivation layer achieves the highest f_T value. However, when comparing passivated devices, the SiO_2-passivated HEMT demonstrates superior f_T compared to other passivation materials. Fig. 4.7(d) shows that the f_T decreases from 54.10 GHz (for SiO_2) to 30.81 GHz (for HfO_2) as higher-κ dielectric materials are used, primarily because of rising gate capacitance and a decrease in g_m. Since g_m and f_T directly correlate with switching speed, this makes SiO_2-passivated devices particularly suitable for high-speed applications. The f_T can be calculated using:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{4.1}$$

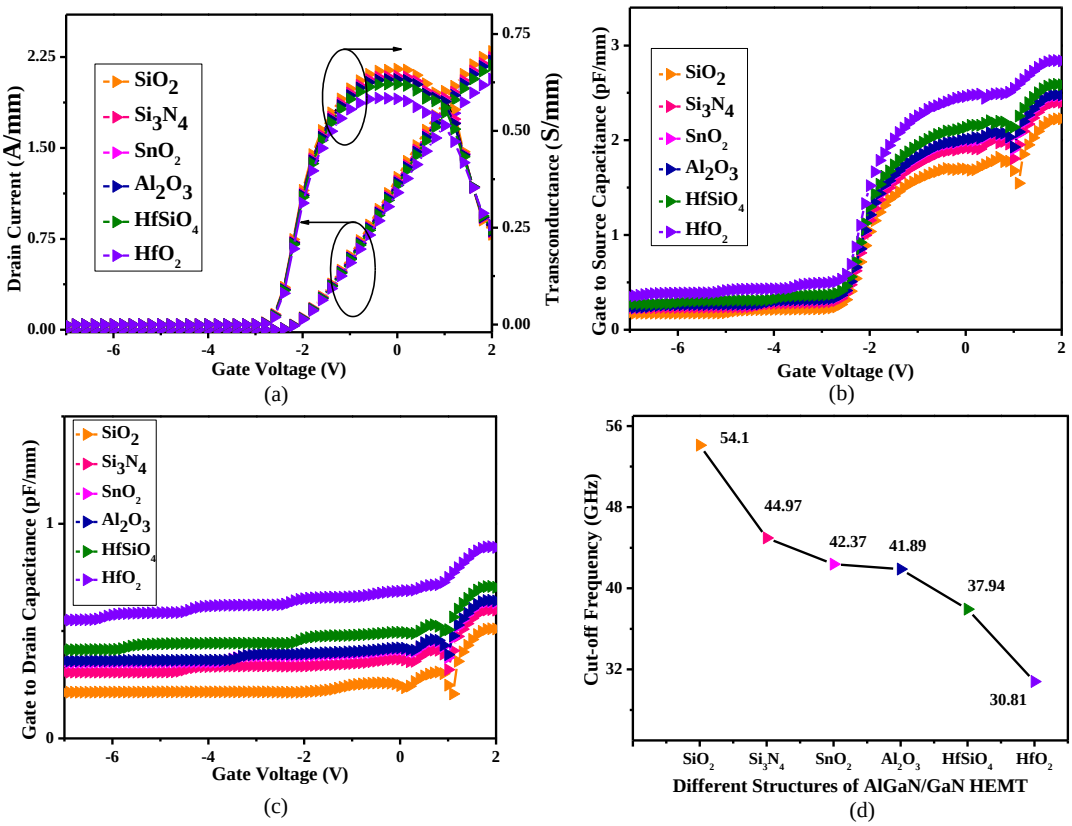


Fig. 4.7. AlGaN/GaN HEMT (a) I_D-V_G characteristics, (b) C_{gs} relative to V_G, (c) C_{gd} relative to V_G, and (d) comparison of f_T for various passivation materials.

From an AC analysis standpoint, the f_T shows decreasing trends with increasing k, suggesting a trade-off between dielectric strength and high-frequency performance. These analyses suggest that while high-κ dielectrics improve DC performance and scaling potential, they may compromise AC performance due to increased parasitic capacitances and reduced carrier velocities. Moreover, high-k passivation layers in HEMTs improve leakage current but present several challenges. The poor interface quality and high defect density of high-k materials can trap charges, lowering carrier mobility and causing threshold voltage shifts [243]. Thermal instability at HEMT processing temperatures may also lead to interfacial reactions that degrade device performance [244]. Mechanical stress from high-k films can induce defects, cracks, or delamination [245], while their higher cost and limited scalability make uniform

large-area deposition difficult compared to conventional passivation [243]. Overcoming these issues requires optimized material selection, process refinement, and a deeper investigation into the behaviour of high-*k* materials in HEMTs. Thus, the choice of passivation material has a significant impact on the RF performance of AlGaN/GaN HEMTs. Low-dielectric materials, such as SiO_2 or Si_3N_4, enhance high-frequency operation but offer limited voltage gain, whereas high-dielectric materials, like HfO_2, improve voltage handling but degrade frequency response. Designers must balance these trade-offs based on application requirements, opting for SiO_2 or Si_3N_4 for high-speed RF applications and HfO_2 or $HfSiO_4$ for higher voltage tolerance in power electronics.

4.4 Impact of Dual Passivation layers on Device Performance

In this section, a dual-layer passivation scheme combining HfO_2 and Si_3N_4 was employed to enhance HEMT device performance. Although SiO_2 exhibits a slightly higher f_T than Si_3N_4 due to its lower parasitic capacitance, it suffers from inferior interface quality and increased leakage, mainly caused by its larger conduction-band offset and oxygen-related interface traps. In contrast, Si_3N_4 provides superior gate control, owing to its higher dielectric constant, and effectively suppresses trap-induced dispersion [246]. Therefore, Si_3N_4 was chosen, together with HfO_2, for the dual passivation layer structure. The DC characteristics of Si_3N_4- and HfO_2-passivated AlGaN/GaN HEMTs, as shown in Fig. 4.8, were evaluated at different V_D (V_D = 0.1–8 V). Both structures show a similar V_{th} trend, with V_{th} gradually shifting from approximately –2.3 V at V_D = 0.1 V to around –1.9 V at higher drain biases. However, Si_3N_4 consistently yields higher drain current (I_{dmax}) and g_m compared to HfO_2 across all bias points. For instance, at V_D = 8 V, Si_3N_4 exhibits I_{dmax} = 2.244 A/mm and g_m = 640 mS/mm, while HfO_2 records lower values of I_{dmax} = 2.069 A/mm and g_m = 585 mS/mm. These results indicate that Si_3N_4 passivation yields better current driving and transconductance performance than HfO_2 under the investigated conditions.

Further simulations were carried out at V_D = 8 V to evaluate the device's DC and RF figures of merit (FOM). The transconductance-to-current ratio (g_m/I_D), g_{ds},

early voltage (V_{EA}), g_m, and intrinsic gain (A_V) are critical figures of merit (FOMs) for analog circuit design [247]. Among these, A_V is particularly vital for operational transconductance amplifiers [248]. These metrics are derived as gate-dependent functions using Eqs. (4.2) and (4.3).

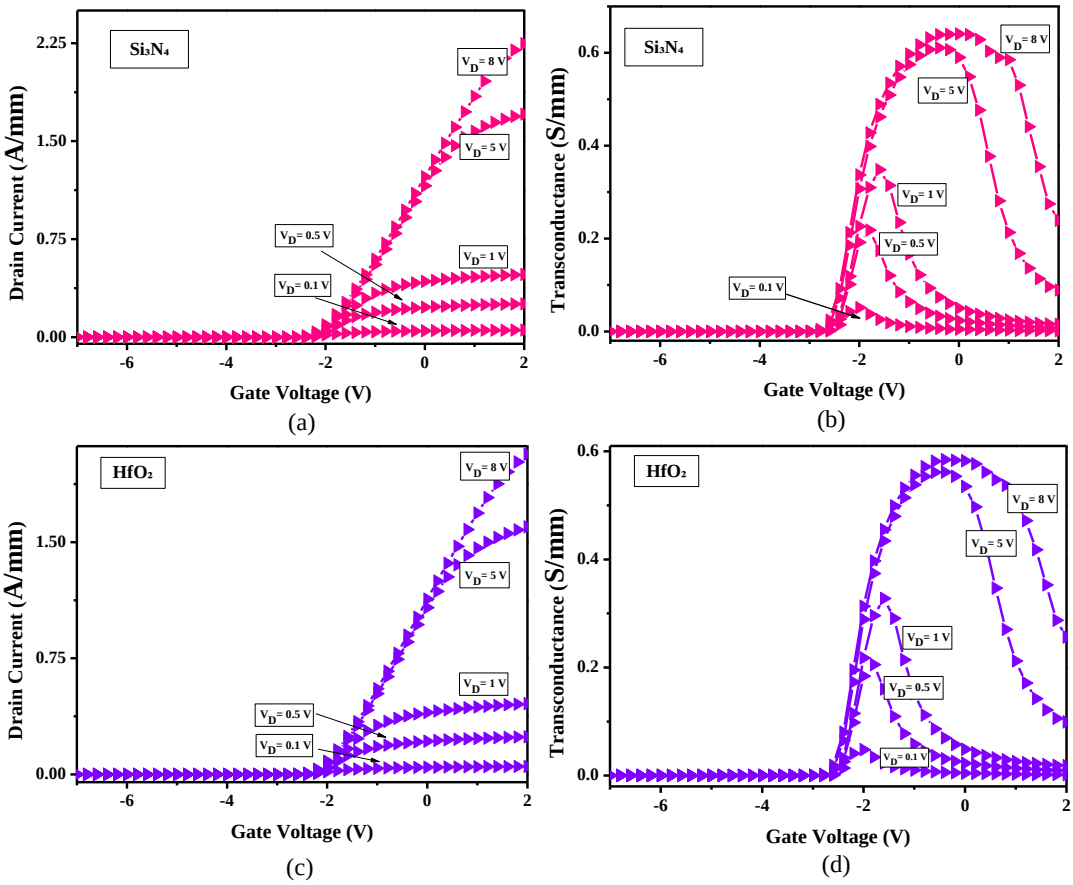


Fig. 4.8. Transfer characteristics of AlGaN/GaN HEMTs with Si_3N_4 and HfO_2 passivation at different V_D: (a) I_D–V_G for Si_3N_4, (b) g_m–V_G for Si_3N_4, (c) I_D–V_G for HfO_2, and (d) g_m–V_G for HfO_2.

$$V_{EA} = I_D/g_{ds} \tag{4.2}$$

$$A_V = g_m/g_{ds} \tag{4.3}$$

Key RF performance indicators—including terminal capacitances (C_{gs}, C_{gd}), f_T, transconductance frequency product (*TFP*), gain frequency product (GFP), and gain

transconductance frequency product (*GTFP*) —were evaluated through small-signal AC analysis (at V_D = 8 V). The *GFP*, *TFP,* and *GTFP*—calculated using Eqs. (4.4)–(4.6)—are critical performance metrics. *TFP* is particularly useful for medium- to high-speed devices, balancing power and bandwidth, while *GFP* is essential for high-frequency amplifiers. Table 4.1 compares Si_3N_4 and HfO_2 passivated structures, showing that for enhanced analog performance—where maximizing V_{EA} and A_V is crucial—HfO_2, owing to its higher-*k*, exhibits higher values of V_{EA} (84.19 V) and A_V (54.75) compared to Si_3N_4 (70.92 V and 41.26, respectively). However, Si_3N_4 demonstrates superior RF performance, yielding higher *GFP* (1851 GHz), *TFP* (26.17 GHz/V), *GTFP* (1080 GHz/V) and f_T (44.97 GHz) compared to HfO_2 (1653 GHz, 19.64 GHz/V, 1075 GHz/V and 30.81 GHz). The larger C_{gs} and C_{gd} in HfO_2 account for its lower f_T, while Si_3N_4 ensures better high-frequency characteristics.

$$GFP = A_V \times f_T \tag{4.4}$$

$$TFP = (g_m / I_D) \times f_T \tag{4.5}$$

$$GTFP = A_V \times TFP \tag{4.6}$$

Table 4.1. Electrical performance evaluation of the double-deck gate-FP AlGaN/GaN HEMT structures employing single Si_3N_4 and HfO_2 passivation materials

Parameters	**Si_3N_4**	**HfO_2**
Dielectric Constant (*k*)	7.5	22
V_{EA} (V)	70.92	84.19
A_V	41.26	54.75
GFP (GHz)	1851	1653
TFP (GHz/V)	26.17	19.64
GTFP (GHz/V)	1080	1075
C_{gs} (pF/mm)	1.89	2.40
C_{gd} (pF/mm)	0.36	0.67

f_T (GHz)	44.97	30.81

Two types of dual passivation material structures have been considered, as shown in Fig. 4.9. In the first configuration (Type-A: HfO_2/Si_3N_4) shown in Fig. 4.9(a), HfO_2 serves as the top passivation layer, while Si_3N_4 acts as the underlying base layer. Conversely, the second arrangement (Type- B: Si_3N_4/HfO_2) (Fig. 4.9(b)) reverses this order, positioning Si_3N_4 as the top layer with HfO_2 beneath it. This specific material combination was strategically selected based on its complementary advantages: HfO_2 provides superior V_{br} characteristics, while Si_3N_4 offers enhanced high-frequency performance, as demonstrated in previous analysis of passivation materials (Section 4.3). The investigation encompassed six distinct device configurations with progressively increasing HfO_2 (Type-A) and Si_3N_4 (Type-B) layer thicknesses (0.1, 0.2, 0.3, 0.4, 0.5, and 0.55 µm) to evaluate thickness-dependent effects on device characteristics while maintaining a constant total passivation thickness of 0.6 µm. Electrical characteristics were comprehensively analysed across all configurations.

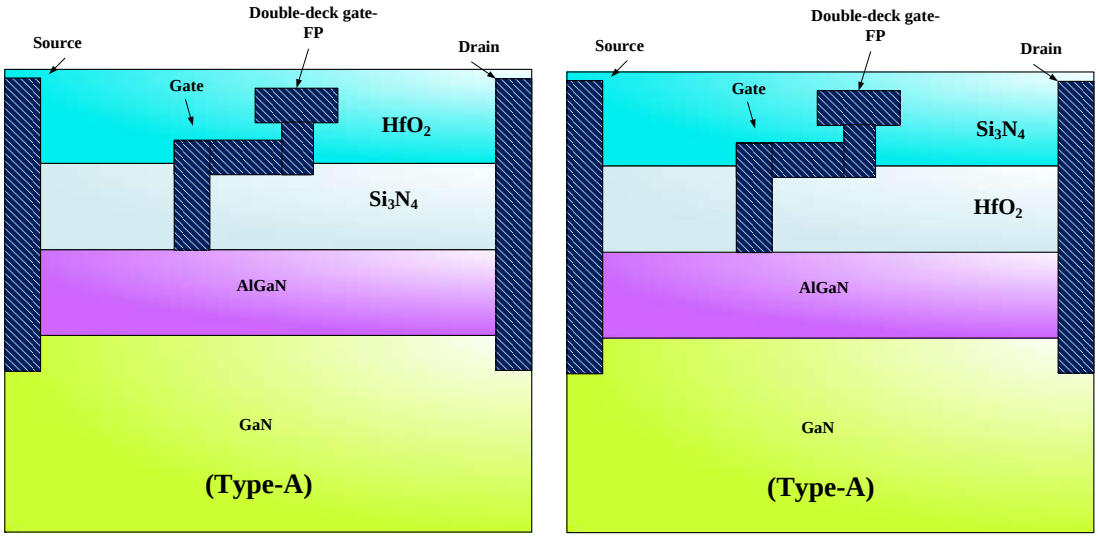


Fig. 4.9. The cross-sectional view of the dual passivation layer in AlGaN/GaN HEMT structures, showing (a) Type-A and (b) Type-B configurations.

Fig. 4.10(a), (b) shows the I_D–V_G characteristics simulated at V_D = 0.1 V. The results indicate that the V_{th} remains consistently stable, ranging from -2.29 to -2.30 V

across all thickness variations for both Type-A and B structures (see Table 4.2). This stability suggests that the dual-layer configuration provides reliable V_{th} performance, irrespective of thickness. Moreover, the peak gm is observed at V_G = –2 V. A single-passivation layer of Si_3N_4 yields a higher g_m of 51.20 mS/mm compared to HfO_2, which has a g_m of 48 mS/mm. For dual-layer Type-A structures, g_m values range from 51.20 mS/mm to 50.10 mS/mm (Fig. 4.10(c)), demonstrating minimal degradation compared to Si_3N_4-only structures, while consistently maintaining values above 50 mS/mm across all thickness variations. In contrast, Type-B structures exhibit g_m values ranging from 47.6 mS/mm to 49.2 mS/mm (Fig. 4.10(d), Table 4.2), suggesting that Type-A devices achieve slightly superior g_m.

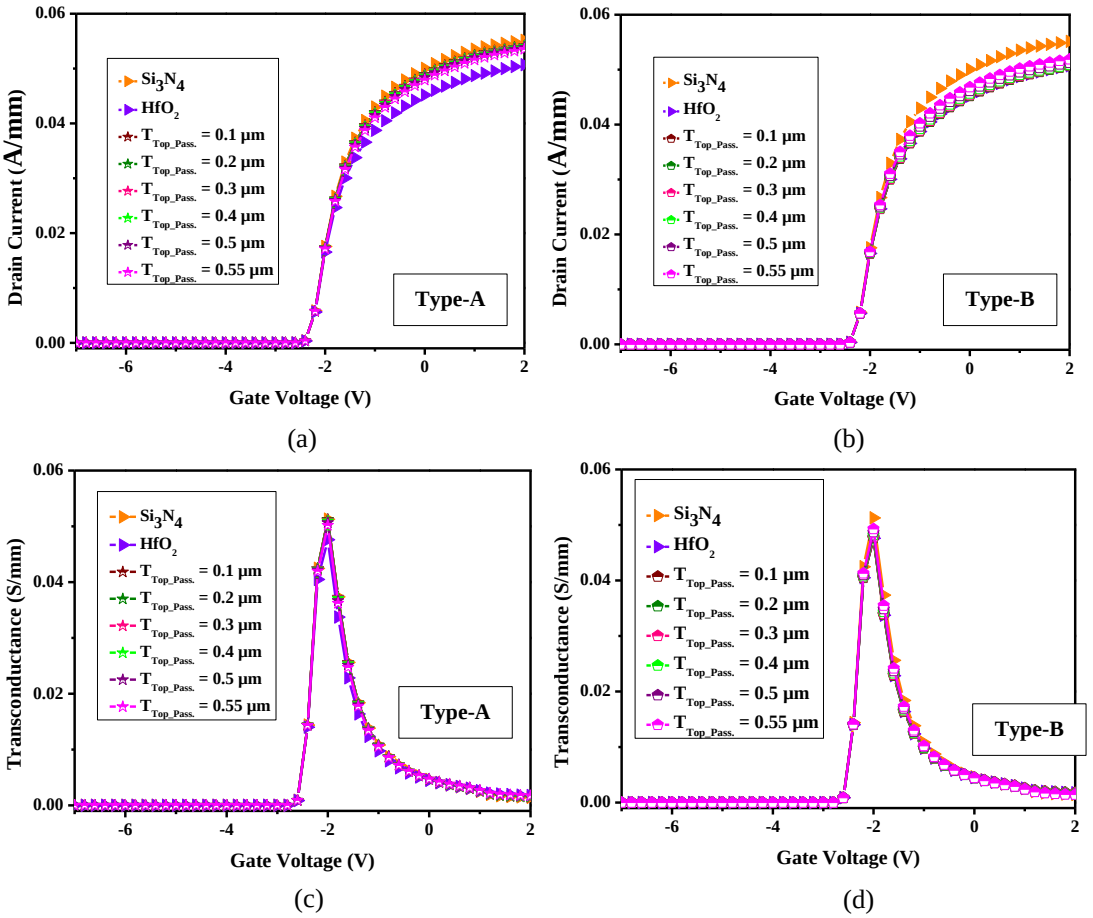


Fig. 4.10. Characteristics of dual passivation layer AlGaN/GaN HEMT: (a) I_D-V_G (Type-A), (b) I_D-V_G (Type-B), (c) g_m vs. V_G (Type-A), and (d) g_m vs. V_G (Type-B).

Table 4.2. DC Performance evaluation of Type-A and B structures across varying top passivation layer thicknesses

Thickness of Top Passivation Material (µm) / Characteristics	0.1	0.2	0.3	0.4	0.5	0.55
V_{th} (V)						
Type-A	-2.29	-2.29	-2.29	-2.29	-2.30	-2.30
Type-B	-2.30	-2.30	-2.30	-2.30	-2.30	-2.30
I_{dss} (A/mm)						
Type-A	1.297	1.296	1.296	1.293	1.282	1.262
Type-B	1.160	1.161	1.163	1.173	1.194	1.220
g_m (mS/mm)						
Type-A	51.20	51.13	51.10	50.90	50.60	50.10
Type-B	47.60	47.70	47.80	48.10	48.60	49.20
V_{br} (V)						
Type-A	781	798	792	786	734	781
Type-B	797	769	763	765	773	767

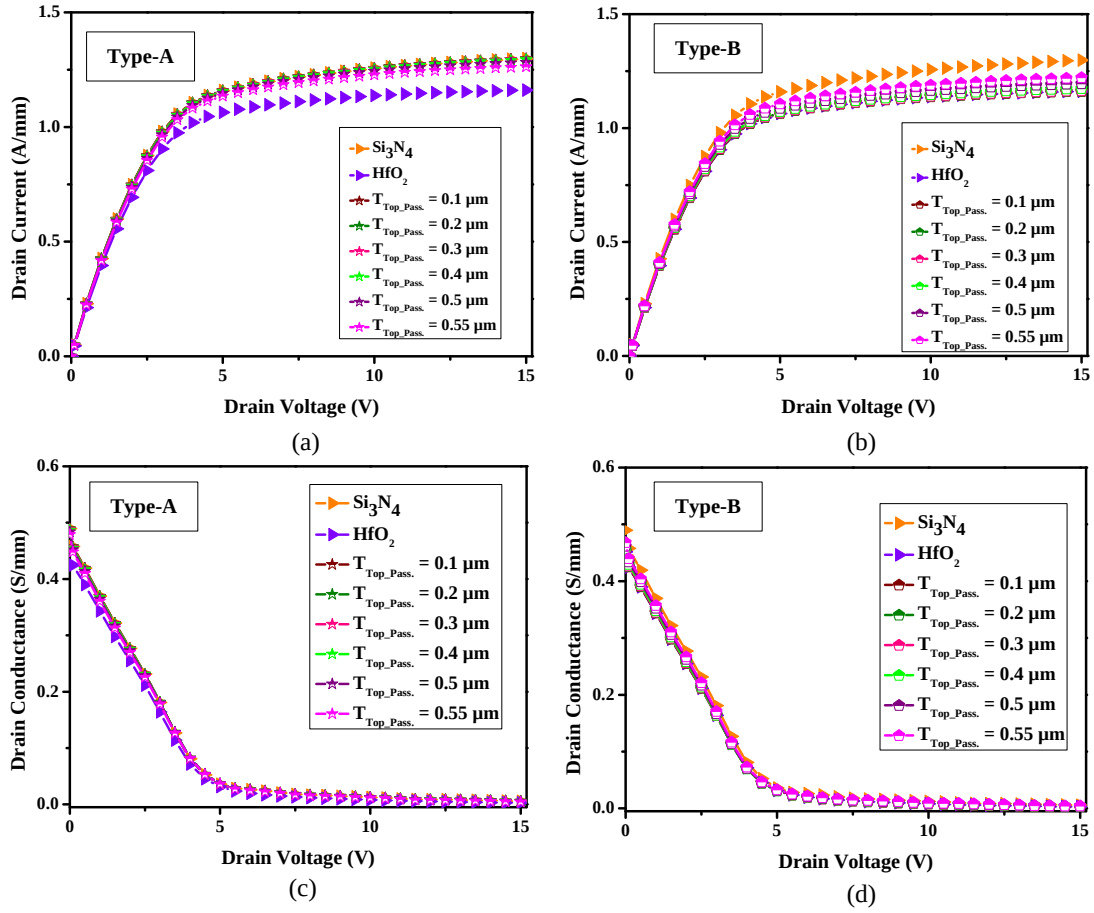
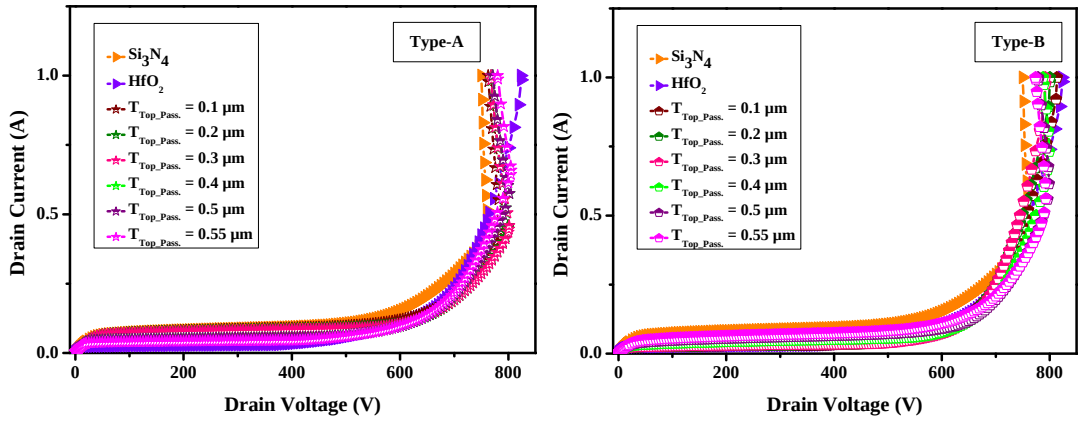


Fig. 4.11. Characteristics of dual passivation layer AlGaN/GaN HEMT: (a) I_D-V_D (Type-A), (b) I_D-V_D (Type-B), (c) g_{ds} vs. V_D (Type-A), and (d) g_{ds} vs. V_D (Type-B).

Fig. 4.11 presents the I_D-V_D characteristics at V_G = 0 V, where Table 4.2 shows that the single-layer Si_3N_4 achieves higher I_{dss} (1.297 A/mm) than HfO_2 (1.178 A/mm). In dual layers, Type-A mirrors Si_3N_4 performance (1.297 A/mm to 1.262 A/mm), while Type-B aligns more closely with HfO_2 (1.16 to 1.22 A/mm) as the top passivation layer thickness increases from 0.1 to 0.55 µm. This suggests that the bottom material significantly influences I_{dss}, with Type-A outperforming Type-B. The dual-passivation structures exhibit superior breakdown characteristics compared to single-passivated devices (Fig. 4.12, Table 4.2). In Type-A, the maximum V_{br} of 798 V is obtained at a HfO_2 top-layer thickness of 0.2 µm, highlighting the advantage of the high-*k* dielectric in suppressing electric field crowding at the gate edges, while the underlying Si_3N_4 ensures good interface quality with the semiconductor. For Type-B, the highest V_{br} of 797 V occurs at a Si_3N_4 thickness of 0.1 µm, which also

surpasses that of single-passivation structures. Overall, Type-A maintains slightly higher and more consistent breakdown voltages (734–798 V) compared to Type-B (763–797 V). This difference is attributed to dielectric ordering: placing HfO_2 on top enhances vertical field screening and strengthens breakdown capability. It is also seen that the V_{br} does not vary monotonically with the upper passivation thickness. This behaviour arises because the FP modifies the electric-field distribution in a non-linear manner. As the relative thicknesses of Si_3N_4 and HfO_2 change, the capacitive coupling between the FP and the channel is altered, which in turn shifts the location of the peak electric field between the gate corner, FP edge, and drain-side region. Since breakdown is governed by the maximum local electric field, such relocations cause fluctuations in V_{br} rather than a smooth trend.



(a) (b)

Fig. 4.12. Breakdown characteristics of (a) Type-A and (b) Type-B configurations.

Table 4.3 summarizes the calculated DC and RF parameters for dual-passivation materials structures, where V_{EA} serves as a key factor in differentiating Type-A from Type-B. Type-B exhibits significantly higher values (75.71-88.08 V) compared to Type-A (70.9–75.57 V), suggesting that Type-B maintains better output resistance and weaker channel modulation. This can be attributed to the electrostatic stability provided by the Si_3N_4 top layer, which helps improves linearity in the output region. Although V_{EA} decreases slightly with increasing passivation thickness in both structures, the overall advantage of Type-B is clear. In terms of A_V, Type-B again shows higher values than Type-A across all thicknesses (>49). Type-A, in contrast, maintains a relatively stable gain between 41 and 43. This reduction in Type-B's gain

can be attributed to a modest rise in g_{ds} with increasing thickness of the top Si_3N_4 layer, lowering the overall gain. Nevertheless, the higher absolute values of A_V in Type-B ensure better amplification capability compared to Type-A.

Table 4.3. Electrical Performance evaluation of Type-A and B structures across varying top passivation layer thicknesses

Thickness of Top Passivation Material (µm) / **Characteristics**	**0.1**	**0.2**	**0.3**	**0.4**	**0.5**	**0.55**
C_{gs} (pF/mm)						
Type-A	1.92	1.95	2	2.10	2.26	2.40
Type-B	2.47	2.39	2.34	2.12	1.99	1.92
C_{gd} (pF/mm)						
Type-A	0.38	0.39	0.41	0.46	0.55	0.62
Type-B	0.70	0.66	0.64	0.51	0.43	0.40
f_T (GHz)						
Type-A	44.15	43.19	41.99	39.46	35.68	32.84
Type-B	28.83	29.91	30.78	34.86	38.59	41.40
V_{EA} (V)						
Type-A	70.91	70.90	70.89	71.23	72.18	75.57
Type-B	88.08	88.10	88.05	84.63	80.39	75.71
A_V						
Type-A	41.25	41.23	41.23	41.40	42.16	43.75
Type-B	57.16	57.20	57.20	54.83	52.36	49.57
GFP (GHz)						
Type-A	1821	1781	1731	1634	1500	1437
Type-B	1648	1711	1761	1911	2021	2052
TFP (GHz/V)						
Type-A	25.68	25.12	24.42	22.94	20.70	19.02
Type-B	18.71	19.42	20.00	22.58	25.14	27.10
GTFP (GHz/V)						
Type-A	1059	1036	1006	949	873	832
Type-B	1069	1111	1144	1238	1316	1344

Gate capacitances (C_{gs} and C_{gd}) in dual-passivation configurations show a slight but consistent rise. In Type-A, increasing the HfO_2 thickness leads to a gradual

increase in both capacitances (C_{gs} and C_{gd}) as seen in Fig. 4.13(a) and (c), which in turn causes a steady degradation in f_T, falling from 44.15 GHz at 0.1 µm to 32.84 GHz at 0.55 µm (Fig. 4.13(e)). On the other hand, Type-B shows the opposite behaviour: the top Si_3N_4 thickness increase results in a monotonic reduction of parasitic capacitances (Fig. 4.13(b) and (d)), thereby improving f_T from 28.83 GHz to 41.40 GHz (Fig. 4.13(f)). This clearly highlights the importance of dielectric ordering, the low-*k* Si_3N_4 on top effectively suppresses capacitive loading, leading to enhanced RF speed. The combined FOM, *GFP*, *TFP*, and *GTFP*, provide a comprehensive view of RF suitability. In Type-A, all three parameters degrade continuously as the HfO_2 thickness increases, confirming that thicker high-k passivation at the top penalizes RF performance due to enhanced capacitive loading. For *GFP*, Type-A outperforms Type-B at top-layer thicknesses of 0.1 and 0.2 µm, but Type-B surpasses Type-A once the thickness reaches 0.3 µm. A similar trend is observed in *GTFP*, where Type-A is higher only at top layer thickness of 0.1 µm, while Type-B dominates at larger thicknesses. For TFP, Type-A starts at 25.6 GHz/V and decreases steadily; it remains higher than Type-B up to 0.4 µm, but beyond 0.5 µm, Type-B values exceed those of Type-A. This difference arises from the material stacking order: in Type-A, with HfO_2 on top (Type-A), the higher dielectric constant directly increases C_{gs} and C_{gd}, leading to larger capacitive loading and degradation of RF FOMs as thickness increases. In contrast, when Si_3N_4 is placed on top (Type-B), the lower dielectric constant minimizes gate-edge capacitance, while HfO_2 beneath improves interface passivation and channel control. This configuration allows Type-B to sustain or even improve its RF performance with increasing passivation thickness. The thickness-dependent analysis reveals that Type-A yields the maximum f_T at a 0.1-µm top layer and the highest V_{br} at 0.2 µm, whereas Type-B attains the highest V_{EA} and A_V at a 0.2-µm top layer and delivers optimum GFP, TFP, and GTFP at 0.55 µm. These results emphasize that although both passivation stacks maintain the same total thickness, the ordering of HfO_2 and SiN strongly governs device electrostatics and RF behaviour. The simulation results also indicated that the dual-passivation structures generally outperform single-passivation counterparts across most thicknesses, except in the case of f_T, where the maximum value achieved remains lower than that of both Si_3N_4- and HfO_2-passivated structures.

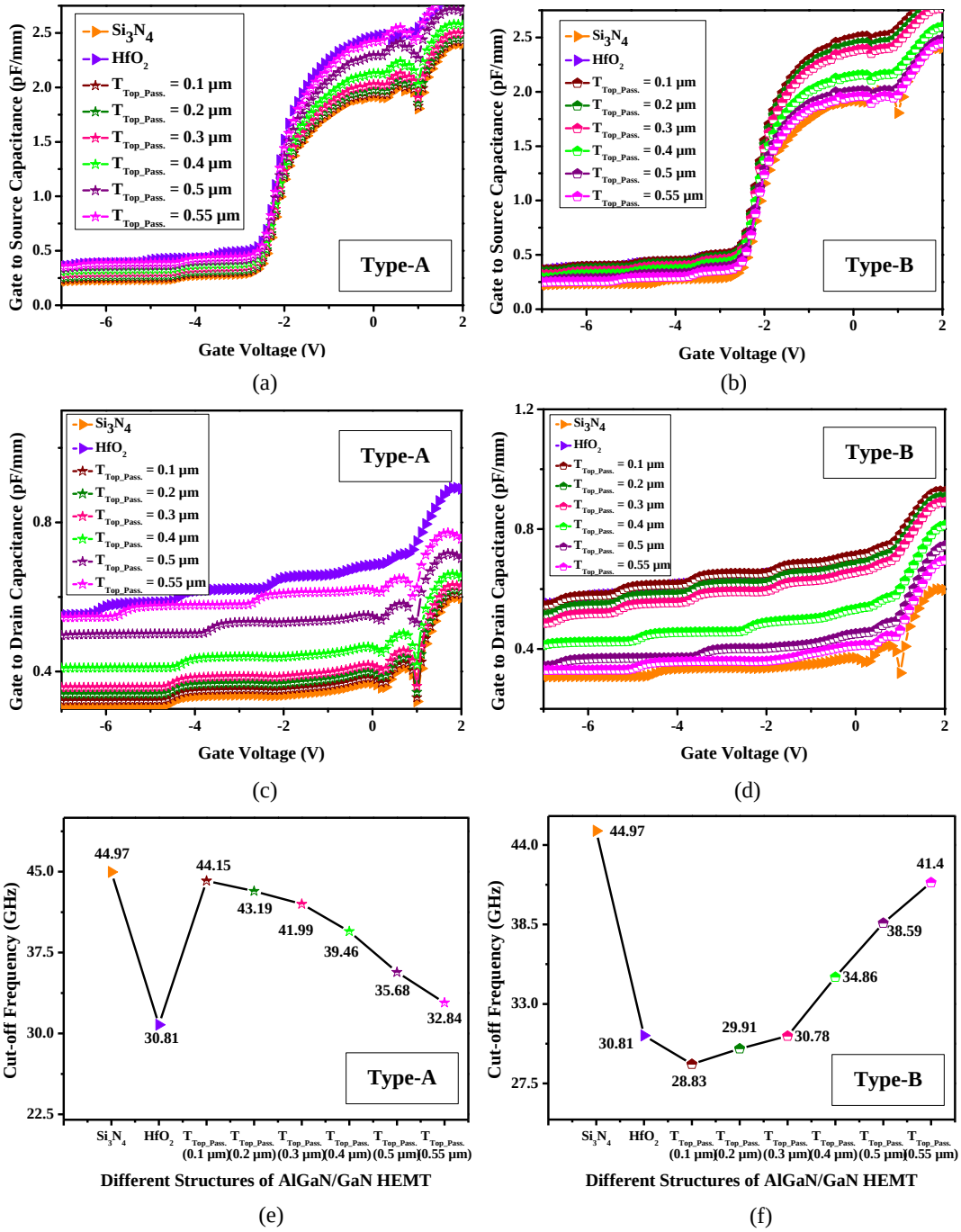


Fig. 4.13. Dual passivation layers AlGaN/GaN HEMT structures: (a) C_{gs} vs. V_G (Type-A), (b) C_{gs} vs. V_G (Type-B), (c) C_{gd} vs. V_G (Type-A), (d) C_{gd} vs. V_G (Type-B), (e) f_T (Type-A), and (f) f_T (Type-B).

4.5. Summary

This chapter comprehensively evaluates the performance of AlGaN/GaN HEMTs with various passivation schemes, revealing critical insights for device

optimization. The HfO_2-passivated devices demonstrate superior breakdown characteristics, achieving a remarkable V_{br} of 788 V, which confirms the advantage of high-*k* dielectrics in enhancing voltage withstand capability. However, SiO_2-passivated HEMTs exhibit the best RF performance, due to their lower parasitic capacitance, making them ideal for high-frequency applications. This highlights the inherent trade-off between breakdown strength and frequency response in the selection of passivation materials. To address this limitation, a dual-passivation approach was investigated, where the comparative study of Type-A and Type-B dual-layer passivated GaN HEMTs demonstrates the critical influence of passivation material ordering and thickness on device performance. Type-A exhibits superior DC performance, with higher I_{dss}, g_m, and V_{br}, owing to the stronger gate control and electric field modulation provided by the high-*k* HfO_2 top layer. Overall, the V_{br} analysis confirms that both dual-layer passivation schemes offer a significant advantage over their single-layer constituents, with V_{br} values for Type-A (~798 V) and Type-B (~797 V) substantially exceeding those of single-layer structures. This confirms the intrinsic benefit of a dual-layer approach for enhancing breakdown ruggedness. Type-A structures achieve relatively higher V_{br} as compared to Type-B. HfO_2 on top serves as a more effective field spreader, redistributing the electric field at the gate edge and thereby improving V_{br}. RF analysis confirms that Type-B, with Si_3N_4 as the top passivation layer and HfO_2 below, outperforms Type-A. While Type-A benefits from reduced gate capacitances at thinner HfO_2 thicknesses, its performance quickly degrades as the top layer is made thicker. In contrast, Type-B continues to gain RF advantages with increasing Si_3N_4 thickness, demonstrating the effectiveness of placing a low-k dielectric on top of a high-k material in dual-layer passivation stacks. Although Type-A exhibits higher f_T values up to 0.4 μm, the associated increase in parasitic capacitances causes a rapid decline in *GFP* and *TFP*, *GTFP*. Since RF circuit suitability depends on composite FOMs (*TFP*, *GFP*, *GTFP*) along with analog FOM (V_{EA}, A_V), Type-B offers better overall RF performance. This chapter highlights the critical role of passivation engineering, where not only the material choice but also the layer ordering and thickness distribution significantly influence the overall DC and RF characteristics of GaN HEMTs.

CHAPTER 5

Investigation of Multi-Material Barrier GaN-based HEMT with Double-Deck Gate Field Plate

5.1 Introduction

High-power and high-frequency amplifiers use GaN-based HEMTs for their superior material properties [249], but advancements in GaN HEMT technology have pushed traditional AlGaN/GaN devices to their performance limits, demanding further improvements. One proposed approach to improve high-frequency performance involves increasing the aluminium content in the AlGaN barrier layer. However, this strategy reduces the critical thickness of the fully strained AlGaN barrier due to the increasing lattice mismatch between AlGaN and GaN, leading to local relaxation at the heterointerface through the formation of misfit dislocations and cracks [250]. To address this issue, InAlN and InAlGaN have been proposed as alternative barrier materials to AlGaN. InAlN/GaN [251] and InAlGaN/GaN [252] heterostructures exhibit stronger spontaneous polarization-induced electric fields compared to AlGaN/GaN, resulting in higher electron concentrations in the 2DEG. Specifically, InAlN-based heterostructures achieve an electron density in the 2DEG of 2.5-3×10^{13} cm^{-3}, more than double the normal value of AlGaN/GaN 2DEG. Additionally, the InAlN/GaN heterostructure exhibits electron mobility of 1800cm^2 /V·s comparable to AlGaN/GaN heterostructures, while maintaining a higher electron concentration in the 2DEG [253]. Due to their high 2DEG electron density, InAlN/GaN-based HEMTs are projected to operate over a wider frequency range**s** [180]. Quaternary InAlGaN has also been proposed as a potential alternative to AlGaN for barrier layers, offering two key advantages. First, the quaternary material allows for independent tuning of the bandgap and lattice constant [254], enabling control of the built-in strain below the crucial value necessary to evade relaxation. Second, incorporating aluminium significantly can enhance polarization in the InAlGaN barrier, largely due to spontaneous polarization effects. However, a major challenge with InAlN is alloy immiscibility, which has been observed during

material growth, resulting in indium-rich surface pits that are difficult to eliminate [255]. These serious issues have made it more difficult to obtain premium InAlN materials. Combining AlGaN and InAlN to form quaternary InAlGaN reduces the immiscibility gap, making InAlGaN/GaN HEMTs more feasible. Studies have shown that quaternary barrier InAlGaN/GaN HEMTs can achieve electron mobilities as high as 1900 $cm^2/V{\cdot}s$ [256], exceeding the average electron mobility of ~1300 $cm^2/V{\cdot}s$ in ternary InAlN/GaN HEMTs [257]. A key disadvantage of InAlN/GaN and InAlGaN/GaN HEMTs is their vulnerability to significant leakage currents, which arise from the intense electric field concentration at the gate edge, particularly toward the drain side. The resulting crowding effect of the electric field can compromise device reliability and lead to premature breakdown. Consequently, InAlN/GaN and InAlGaN/GaN HEMTs typically exhibit lower breakdown voltage (V_{br}) compared to AlGaN/GaN HEMTs, even though they give higher drain current, limiting their applicability in ultra-high-power applications that require high V_{br} along with large drain currents [167]. To overcome these limitations, symmetric and asymmetric GaN HEMT structures have been proposed, which aim to enhance both V_{br} and drain current while leveraging the polarization advantages of InAlN and InAlGaN. This chapter investigates incorporating two or three different barrier materials within a single HEMT structure to design a device capable of handling high current densities and high operating voltages for ultra-high-power applications.

5.2 Single Material Barrier Structure and its Thickness Optimization

Fig. 5.1 presents a cross-sectional view (not to scale) of AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMTs with a double-deck field plate (FP) structure at the gate. The gate length (L_G), source-to-gate (L_{SG}) distance, and source-to-drain distance (L_{SD}) are 0.5 µm, 0.5 µm, and 4.7 µm, respectively. The device architecture includes a 0.6 µm Si_3N_4 passivation layer, a variable barrier layer—AlGaN (Al composition = 0.23), InAlN (In composition = 0.17) or InAlGaN (In composition = 0.16) — a 0.2 µm GaN buffer layer incorporating a 30 nm GaN channel layer, all arranged from top to bottom. The gate FP length (L_{G_FP}) is 1.1 µm, with a thickness (T_{G_FP}) of 0.02 µm. The top deck T-gate has a length (L_{U_FP}) of 0.5 µm, a thickness (T_{U_FP}) of 0.02 µm, and the vertical FP thickness (T_{V_FP}) is 0.08 µm. The same

physics models and simulator validation approach described in Section 3.2 are applied here**.** The specified dimensions and models are applied consistently across all the device structures considered in this chapter.

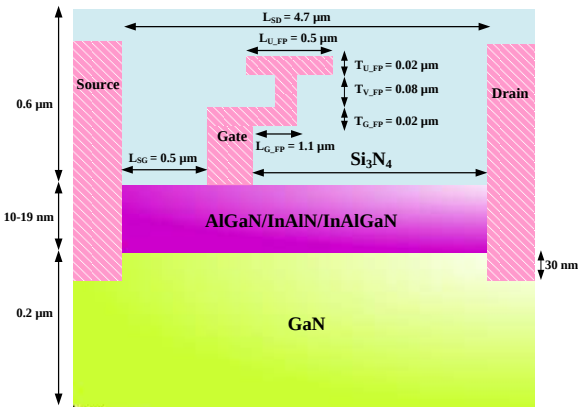


Fig. 5.1. Schematic diagram of HEMT with a double-deck gate FP structure.

Three HEMT structures were simulated with varying barrier thicknesses, ranging from 10 to 19 nm, utilizing distinct barrier layers, including AlGaN, InAlN, and InAlGaN. All three structures maintain consistent dimensions as previously specified. Initially, the AlGaN/GaN HEMT was simulated to assess its various

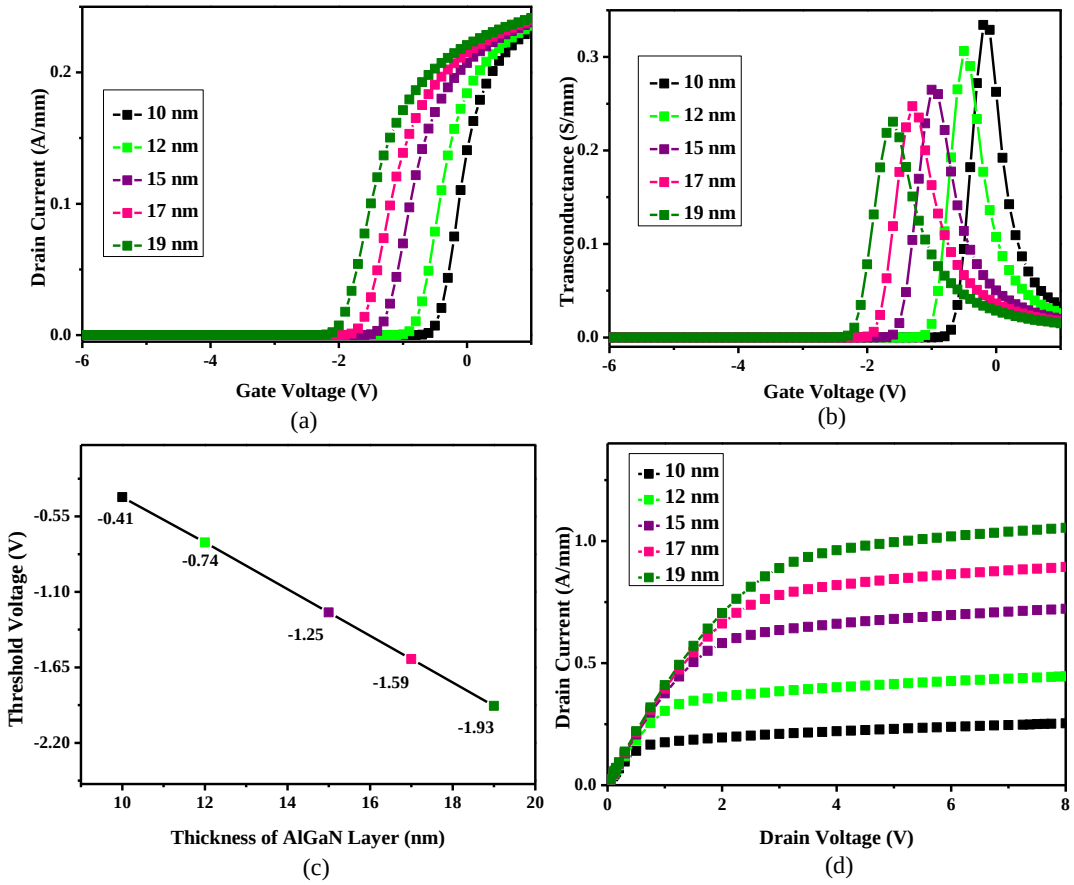


Fig. 5.2. AlGaN/GaN HEMT structure's (a) I_D-V_G, (b) g_m, (c) V_{th}, and (d) I_D-V_D characteristics with different barrier thickness.

electrical properties. The electron concentration significantly influences the device's transfer (I_D-V_G) and output characteristics (I_D-V_D). In Fig. 5.2(a), the gate voltage (V_G) was changed from −6 V to 1 V with a 0.1 V increment, at a drain voltage (V_D) of 0.5 V, to obtain the transfer characteristics (I_D-V_G). The peak transconductance (g_m) for AlGaN layer thicknesses of 10 nm and 19 nm was observed to range from 334 mS/mm to 230 mS/mm, respectively, indicating a decrease in g_m with increasing barrier thickness (Fig. 5.2(b)). As the barrier thickness increases, a shift in the threshold voltage (V_{th}) to more negative values are observed (Fig. 5.2(c)). Additionally, the observed gate leakage current ($I_{G\_Leakage}$) varied between 3.50 µA/mm and 4.06 µA/mm. The I_D-V_D characteristics (Fig. 5.2(d)) at V_G = 0 V showed that the maximum drain saturation current (I_{dss}) increases with the AlGaN barrier thickness, rising from 0.252 A/mm at 10 nm to 1.053 A/mm at 19 nm.

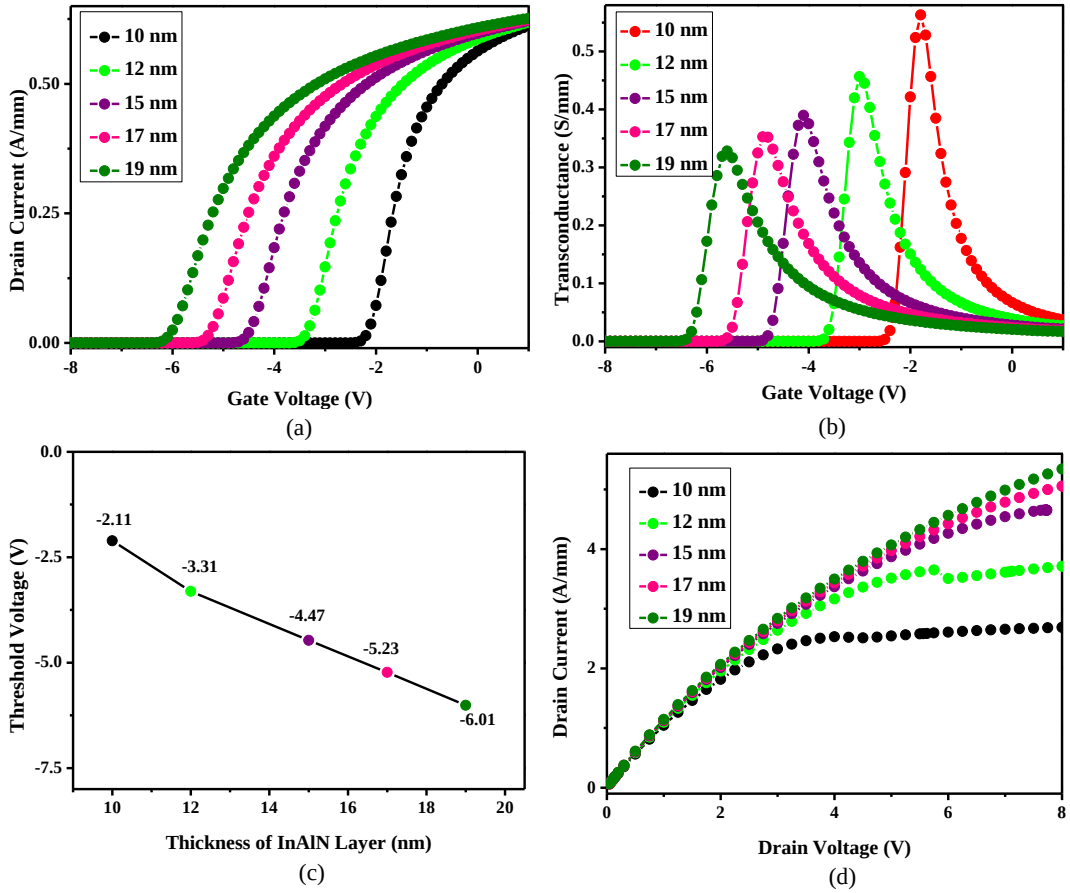


Fig. 5.3. InAlN/GaN HEMT structures (a) I_D-V_G, (b) g_m, (c) V_{th}, and (d) I_D-V_D with different barrier thickness.

Furthermore, the InAlN/GaN HEMT structure was simulated using the same dimensions and material parameters, with a variable barrier layer thickness. The I_D-V_G characteristics (Fig. 5.3(a)) at V_D = 0.5 V, shows that the peak g_m ranges from 562 mS/mm at 10 nm to 328 mS/mm at 19 nm InAlN barrier thickness, illustrating a reduction in g_m with increasing barrier thickness (Fig. 5.3(b)). There is also a shift in the V_{th} towards a more negative value as shown in Fig. 5.3(c). The $I_{G\_Leakage}$ for the InAlN barrier structure ranges from 57.5 µA/mm to 72.6 µA/mm, exhibiting a significantly elevated value compared to the AlGaN barrier structures. The maximum I_{dss} increases with increasing InAlN barrier thickness, from 2.688 A/mm at 10 nm to 5.274 A/mm at 19 nm (Fig. 5.3 (d)).

Fig. 5.4(a) compares the I_D-V_G characteristics of InAlGaN/GaN HEMT structures, where the peak g_m ranges from 492 mS/mm at 10 nm to 314 mS/mm at 19 nm InAlGaN barrier thickness. Similar to the previous structures, g_m decreases with

increasing barrier thickness (Fig. 5.4(b)). As illustrated in Fig. 5.4(c), a shift in V_{th} towards more negative values is observed, following a trend consistent with AlGaN and InAlN barrier structures. The $I_{G\_Leakage}$ for the InAlGaN barrier structure ranges

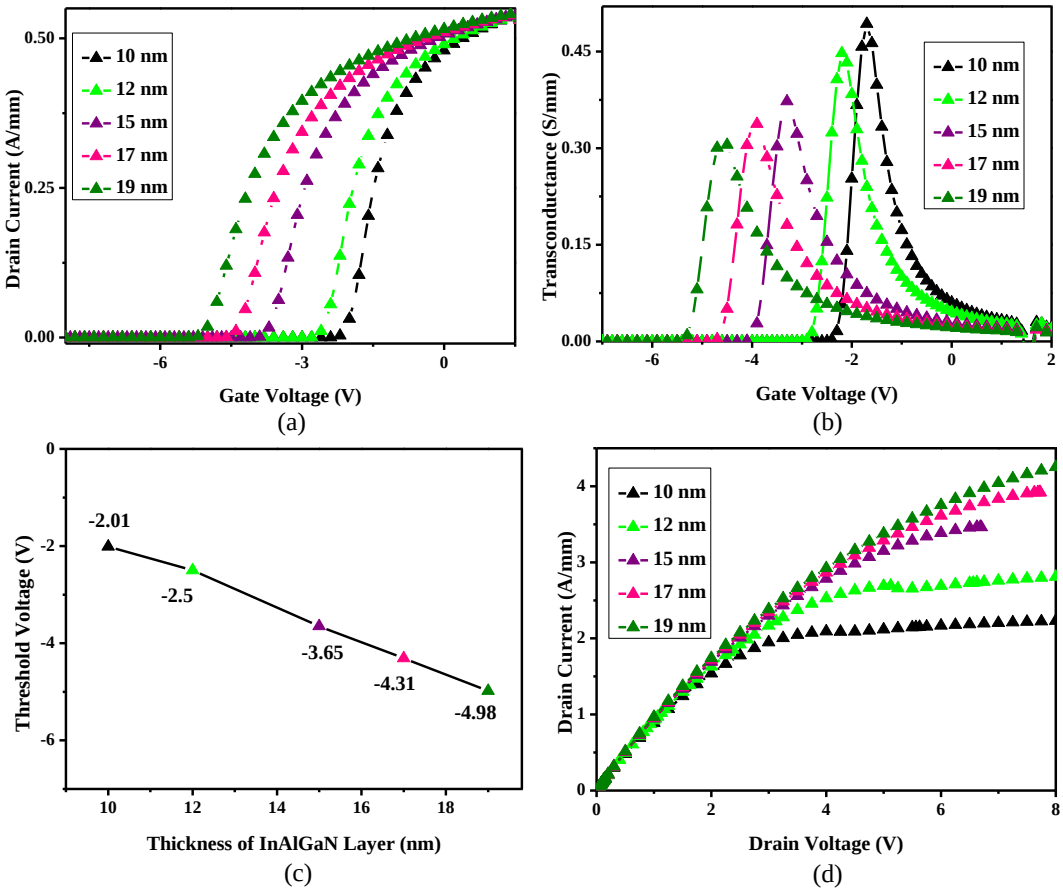


Fig. 5.4. InAlGaN/GaN HEMT structures (a) I_D-V_G, (b) g_m, (c) V_{th}, and (d) I_D-V_D with barrier thickness variation.

from 0.048 to 0.053 A/mm, which is found to exceed that of the AlGaN and InAlN-based HEMT structures. Additionally, the maximum I_{dss} increases with barrier thickness, from 2.230 A/mm at 10 nm to 4.251 A/mm at 19 nm (Fig. 5.4(d)).

Based on the simulation results, the InAlGaN barrier structure exhibits the highest $I_{G\_Leakage}$ current, while the AlGaN HEMT structure demonstrates the lowest leakage current. In terms of I_{dss} and g_m, the InAlN barrier structure outperforms both the AlGaN and InAlGaN configurations. Literature indicates that InAlN, when lattice-matched to GaN, exhibits stronger polarization than AlGaN, which leads to a denser 2DEG at the interface. This increased density enhances charge carrier

availability, leading to higher saturation drain current. Additionally, the AlGaN HEMT structure shows a higher V_{th} compared to the other barrier material configurations.

Three HEMT structures with different barrier materials—AlGaN, InAlN, and InAlGaN—were studied, and their various characteristics were compared for different barrier thicknesses. However, for the rest of the investigation, the barrier layer thicknesses were set at 17 nm for AlGaN, 12 nm for InAlN, and 10 nm for InAlGaN. Since a lower barrier thickness typically yields a higher g_m, thicknesses of 12 nm and 10 nm were selected for InAlN and InAlGaN, respectively. These thinner barrier layers, compared to AlGaN, result in higher I_{dss} values. Specifically, InAlN HEMT with a 12 nm barrier exhibits a high I_{dss} of 3.726 A/mm and a V_{th} of –3.31 V, while InAlGaN HEMT with a 10 nm barrier shows an I_{dss} of 2.230 A/mm and a V_{th} of –2.01 V. Although the AlGaN HEMT achieves a higher g_m at a barrier thickness of 10 nm, its I_{dss} is relatively low. Therefore, in this comparison, a barrier thickness of 17 nm was chosen for AlGaN, resulting in an I_{dss} of 0.893 A/mm and a V_{th} of -1.59 V.

Table 5.1. Comparison of AlGaN, InAlN, and InAlGaN barrier HEMT structures

Barrier materials	V_{th} **(V)**	I_{dmax} **(A/mm)**	I_{dss} **(A/mm)**	$I_{G\_Leakage}$ **(A/mm)**	***SS*** **(mV/d**	**2DEG (cm^{-2})**	V_{br} **(V)**	g_m **(mS/mm)**
AlGaN (17 nm)	-1.59	0.251	0.893	4.04e-06	91	7.13×10^{12}	712	247
InAlN (12 nm)	-3.31	0.638	3.726	5.59e-05	51	1.97×10^{13}	348	456
InAlGaN (10 nm)	-2.01	0.541	2.230	0.048	45	1.64×10^{13}	389	492

The V_{th} of AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN was measured at −1.59 V, -3.31 V, and -2.01 V, respectively. The observed leftward shift in V_{th} for the InAlN and InAlGaN barrier devices can be attributed to the reduced thickness of the barrier layers beneath the gate electrode and the higher 2DEG concentration. This investigation confirmed that the InAlN barrier yielded the highest I_{dss}. I_D-V_D

characteristics were obtained by sweeping V_D from 0 to 8 V while maintaining V_G at 0 V. The AlGaN barrier exhibited a peak g_m reduction of approximately 45.83 % relative to the InAlN barrier (247 mS/mm vs. 456 mS/mm) and 49.8 % lower than the InAlGaN barrier (247 mS/mm vs. 492 mS/mm). Additionally, the AlGaN barrier showed an output current approximately 76.01 % reduction relative to the InAlN barrier (0.893 A/mm vs. 3.726 A/mm), primarily due to the reduced 2DEG concentration in the GaN channel (7.13×10^{12} cm^{-3} vs. 1.97×10^{13} cm^{-3}). Similarly, the current was about 59.95 % lower than that of the InAlGaN devices (0.893 A/mm vs. 2.230 A/mm), which also stems from the decreased 2DEG density in the GaN channel (7.13×10^{12} cm^{-3} vs. 1.64×10^{13} cm^{-3}). Despite the superior output drain current and g_m observed in the InAlN HEMT structure, V_{br} simulations indicated that the InAlN device is predicted to experience a breakdown at 348 V (as detailed in Table 5.1). The V_{br} of the AlGaN barrier device is significantly higher than that of the InAlN and InAlGaN devices. Specifically, the drain current for the InAlN device begins to increase at approximately 348 V, for the InAlGaN device, at 389 V, and for the AlGaN device, a steep rise in current is observed at approximately 712 V.

5.3 Impact of Dual-Material Barriers on Electrical Performance

The characteristics of a single HEMT device that incorporates two different barrier materials is investigated in this section. Dual-material barrier structures are engineered to optimize the trade-off between achieving a high I_{dss} and improved V_{br}. The analysis encompasses both asymmetric and symmetric barrier structures. In the asymmetric structure, the thicknesses of the first and second barrier materials differ, whereas in the symmetric structure, they are identical. For asymmetric configurations, barrier thicknesses of 17 nm for AlGaN, 12 nm for InAlN, and 10 nm for InAlGaN were applied to the same device while maintaining all other dimensions constant. The asymmetric structure, which involves varying thicknesses of the barrier layers (such as AlGaN, InAlN, and InAlGaN), introduces additional fabrication complexity. Precise control over the deposition process is required to achieve the intended thickness variations, which can increase both the process time and the risk of deviation from the desired device characteristics. For that reason, symmetric structures are also studied here, offering a simplified and uniform growth process,

which enhances fabrication consistency, reduces production time, and minimizes variability. Symmetric structures, simulations were performed with uniform barrier layer thicknesses of 10 nm, 12 nm, and 17 nm, regardless of the material used. Four material combinations, namely Case I (AlGaN + InAlGaN), Case II (InAlGaN + AlGaN), Case III (AlGaN + InAlN), and Case IV (InAlN + AlGaN), are shown in Figs. 5.5-5.9, respectively. For each Case, two structural variations are examined. In the first variation, the first barrier material extends up to 1 µm (Fig. 5.5(a, c), Fig. 5.6(a, c), Fig. 5.7(a, c), Fig. 5.8(a, c)) while in the second it extends up to 1.25 µm (Fig. 5.5(b, d), Fig. 5.6(b, d), Fig. 5.7(b, d), Fig. 5.8(b, d)). These variations are applied consistently across all cases, for both symmetric (Fig. 5.5(c, d), Fig. 5.6(c, d), Fig. 5.7(c, d), Fig. 5.8(c, d)) and asymmetric (Fig. 5.5(a, b), Fig. 5.6(a, b), Fig. 5.7(a, b), Fig. 5.8(a, b)) configurations, in dual-material barrier structures.

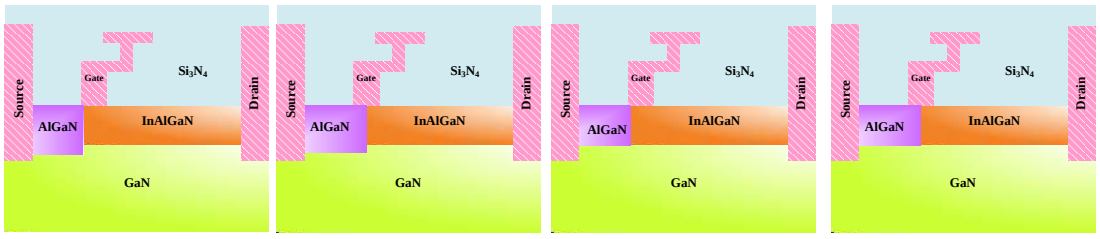


Fig. 5.5. Case I (a) asymmetric structure with AlGaN length up to 1µm, (b) asymmetric structure with AlGaN length up to 1.25 µm, (c) symmetric structure with AlGaN length up to 1µm, (b) symmetric structure with AlGaN length up to 1.25µm.

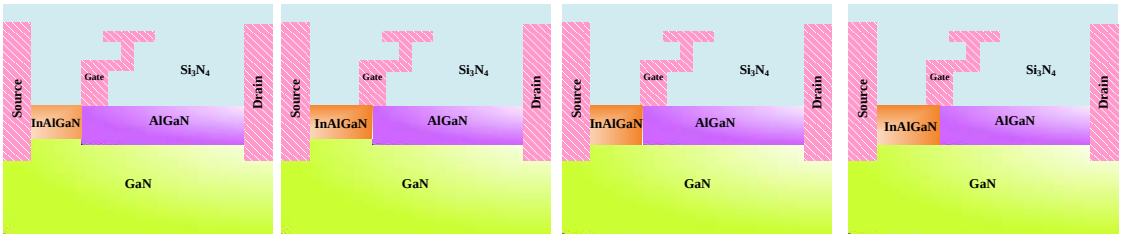


Fig. 5.6. Case II (a) asymmetric structure with InAlGaN length up to 1µm, (b) asymmetric structure with InAlGaN length up to 1.25 µm, (c) symmetric structure with InAlGaN length up to 1µm, (b) symmetric structure with InAlGaN length up to 1.25µm.

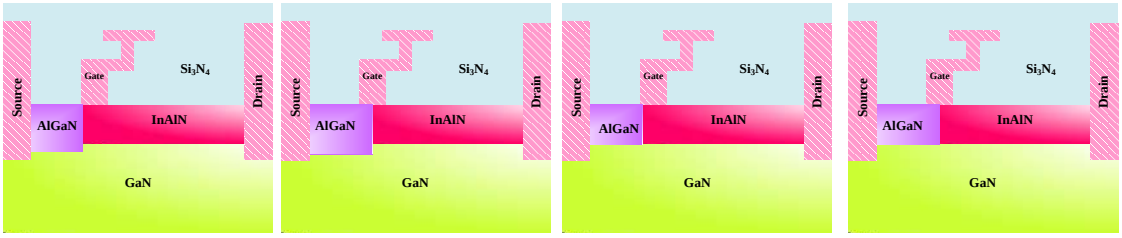


Fig. 5.7. Case III (a) asymmetric structure with AlGaN length up to 1µm, (b) asymmetric structure with AlGaN length up to 1.25 µm, (c) symmetric structure with AlGaN length up to 1µm, (b) symmetric structure with AlGaN length up to 1.25µm.

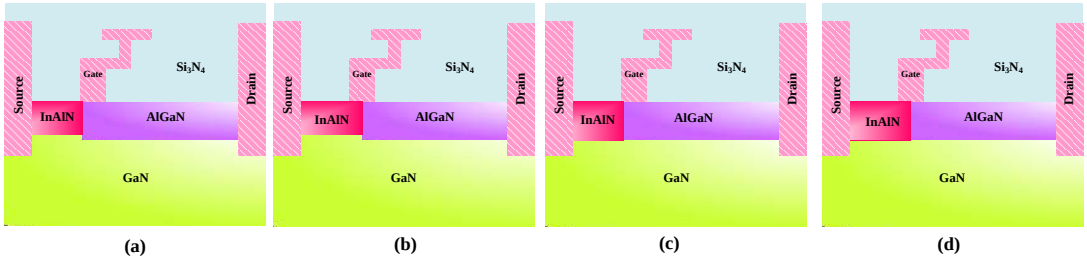


Fig. 5.8. Case IV (a) asymmetric structure with InAlN length up to 1µm, (b) asymmetric structure with InAlN length up to 1.25 µm, (c) symmetric structure with InAlN length up to 1µm, (b) symmetric structure with InAlN length up to 1.25µm.

Table 5.2 presents a comparison of parameters for HEMT structures with asymmetric and symmetric dual-material barriers with barrier thicknesses of 10, 12, and 17 nm. The comparison encompasses all configurations given in Figs. 5.5-5.8. I_D-V_G characteristics were assessed with a V_D of 0.5 V, and V_G was varied from -8 V to 1 V in increments of 0.1 V. The simulation results indicate that, in most instances, the g_m values exceed those observed for AlGaN (247 mS/mm). In Case I, for asymmetric structures, g_m values for the 1st barrier material lengths up to 1 µm are higher compared to lengths up to 1.25 µm. Conversely, in Case II, Case III, and Case IV of asymmetric structures, as well as all symmetric structures, g_m increases with the length of the first barrier layer. The maximum g_m values of 416 mS/mm and 488 mS/mm were observed in Case I (asymmetric structure) and Case III (10 nm symmetric structure) for 1st barrier material lengths up to 1 µm and 1.25 µm, respectively. The simulation results also indicate that, in some cases, V_{th} becomes more positive compared to the single AlGaN barrier structure, which has a V_{th} of -1.59 V (see Table 5.2). In asymmetric structures (Cases I and III), as well as in all

symmetric HEMT structures, V_{th} shifts to a more positive value as the length of the first barrier material is increased to 1.25 µm. In contrast, in Cases II and IV of asymmetric structures, V_{th} becomes more negative with increasing length of the first barrier layer. The least negative V_{th} values of -0.40 V (Cases II and IV) and -0.45 V (Case III) were observed in symmetric 10 nm HEMT structures for 1st barrier material lengths of up to 1 µm and 1.25 µm, respectively.

In dual-material barrier structures, $I_{G\_Leakage}$ generally increases compared to single-barrier material configurations. For asymmetric and symmetric structures (Case I and Case III), $I_{G\_Leakage}$ decreases as the length of the first barrier material extends to 1.25 µm. Conversely, in Cases II and IV of asymmetric and symmetric structures, $I_{G\_Leakage}$ increases with the increasing length of the first barrier layer. For single-material configurations, InAlN demonstrates an $I_{G\_Leakage}$ current of 55.9 µA, while AlGaN shows a considerably lower value of 4.04 µA. In dual-material barrier structures, the lowest $I_{G\_Leakage}$ is achieved at a barrier thickness of 10 nm in Case IV, where InAlN is used as the first barrier material and AlGaN as the second. Specifically, when the first barrier material extends to 1 µm, the leakage current is 11 µA. When it extends to 1.25 µm, the leakage current is 35 µA, marking the minimum values observed in all cases in this comparison. A comparative analysis of the I_{dss} is carried out in all cases, with I_D-V_D characteristics measured at V_G = 0 V with V_D swept up to 8 V (Table 5.2). The simulation results indicate that, in most cases, the I_{dss} values exceed those of the single AlGaN barrier layer structure, which has an I_{dss} of 0.893 A/mm. For both asymmetric and symmetric structures, specifically in Cases I and III, the I_{dss} values are higher when the barrier length is up to 1 µm compared to lengths extending to 1.25 µm. In contrast, in Cases II and IV, for both asymmetric and symmetric configurations, I_{dss} increases as the length of the first barrier layer extends to 1.25 µm. In most of the cases of 1st barrier material length up to 1 µm, it is observed that Case III shows higher I_{dss} values for both symmetric and asymmetric structures.

Table 5.2 also provides a comparison of V_{br} across all the cases. In Cases I and IV of asymmetric structures, as well as Cases II and IV of symmetric structures, V_{br} decreases when the length of the 1st barrier material is extended to 1.25 µm. In

contrast, Cases II and III of asymmetric structures, along with Cases I and III of symmetric structures, exhibit an increase in V_{br} with the longer barrier length. The V_{br} analysis indicates that the highest V_{br} values, 731 V for a 1µm 1st barrier length and 698 V for a 1.25 µm 1st barrier length, are achieved in Case II for both symmetric and asymmetric structures of 10 nm.

Table 5.2. Parameters comparison of dual-material barrier structures

	Barrier Thicknes	**Asymmetric**		**10 nm**		**12 nm**		**17 nm**	
	1st Materi-al Length	**Up to 1 µm**	**Up to 1.25 µm**	**Up to 1 µm**	**Up to 1.25 µm**	**Up to 1 µm**	**Up to 1.25 µm**	**Up to 1 µm**	**Up to 1.25 µm**
Parameter	**Cases**								
g_m (mS/mm)	Case I	416	364	351	454	416	364	351	454
	Case II	249	275	330	402	249	275	330	402
	Case III	386	391	364	488	386	391	364	488
	Case IV	260	311	334	412	260	311	334	412
V_{th} (V)	Case I	-2.02	-1.64	-2.01	-0.47	-2.67	-0.80	-4.32	-1.65
	Case II	-1.60	-1.67	-0.40	-0.47	-0.74	-0.80	-1.59	-1.65
	Case III	-3.34	-1.63	-2.55	-0.45	-3.32	-0.80	-5.24	-1.64
	Case IV	-1.59	-1.67	-0.40	-0.47	-0.74	-0.80	-1.59	-1.65
$I_{G\_Leakage}$ (A/mm)	Case I	0.040	0.023	0.031	0.030	0.031	0.030	0.031	0.030
	Case II	0.0002	0.026	0.0002	0.024	0.000	0.026	0.0004	0.033
	Case III	50.6×10^{-6}	48.3×10^{-6}	0.001	0.0006	0.001	0.0006	0.001	0.0005
	Case IV	16.5×10^{-6}	45.3×10^{-6}	11×10^{-6}	35.9×10^{-6}	11.7×10^{-6}	6.9×10^{-6}	4.5×10^{-6}	46×10^{-6}
I_{dss} (A/mm)	Case I	1.582	1.090	1.370	0.354	1.704	0.619	2.328	1.222
	Case II	0.797	1.012	0.262	0.476	0.471	0.738	0.972	1.306
	Case III	2.460	1.198	1.732	0.375	2.070	0.648	2.340	1.270
	Case IV	0.900	1.164	0.266	0.495	0.478	0.768	0.991	1.367
V_{br} (V)	Case I	395	312	402	419	406	442	406	493
	Case II	655	698	731	555	708	541	723	537
	Case III	353	375	335	389	371	406	404	459
	Case IV	664	509	671	544	710	533	698	527

The simulation results demonstrate that the use of a dual-material barrier significantly enhances both the I_{dss} and the V_{br}. The following summarization of the result is based on all the simulated structures with a 1st barrier material length of up to 1 µm. Comparing the traditional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMT structures with the dual-material asymmetric and symmetric structures, we have come to the following conclusions. First, in terms of g_m, the asymmetric structure of Case I (AlGaN+InAlGaN) with a g_m value of 416 mS/mm surpasses that of the AlGaN/GaN HEMT but remains lower than InAlN/GaN and InAlGaN/GaN HEMTs. In terms of V_{th}, Cases II (InAlGaN+AlGaN) and IV (InAlN+AlGaN) with a 10 nm barrier material achieve the maximum shift of V_{th} towards more positive values (-0.40 V), exceeding the values for AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMTs. For $I_{G\_Leakage,}$ Case IV (10 nm) records the lowest $I_{G\_Leakage}$ at 0.11 µA/mm, which is significantly lower than that of the traditional structures. In terms of $I_{dss,}$ Case III (AlGaN+InAlN) of an asymmetric structure achieves the highest I_{dss} of 2.46 A/mm, surpassing values seen in AlGaN/GaN and InAlGaN/GaN HEMTs. Case II (10 nm) achieves a maximum V_{br} of 731 V, which exceeds that of AlGaN/GaN HEMTs. Notably, in Case II and Case IV, the V_{br} improves when the second barrier material is AlGaN, whereas in Case I and Case III, the I_{dss} is enhanced when the second material is InAlN and InAlGaN. Furthermore, Case II (17 nm) shows a V_{br} of 723 V and an I_{dss} of 0.972 A/mm, outperforming AlGaN/GaN HEMTs in both metrics. If we analyze the values that fall somewhere in the middle of all three traditional devices, Case III (17 nm) yields the highest results, with V_{br} of 404 V and I_{dss} of 2.34 A/mm.

5.4 Impact of Triple-Material Barriers on Electrical Performance

This section examines the characteristics of a single HEMT device that incorporates three distinct barrier materials—AlGaN, InAlN, and InAlGaN. The purpose of this structure is to further optimize the device performance by combining the advantages of each material within a unified layer. The investigation evaluates six different combinations of materials, as detailed in Table 5.3. For simplicity, this part of the analysis focuses only on symmetric barrier structures with thicknesses of 10, 12, and 17 nm, while all other dimensions are kept constant. The barrier materials

are arranged so that the first barrier material extends to the beginning edge of the gate (1 µm), the second barrier material begins at the end of the first material and extends to the end of the FP, and the third barrier material starts after the second material.

Table 5.3. Triple-material barrier GaN HEMT structures

Cases	Barrier material combination
Case A	InAlN+ InAlGaN +AlGaN
Case B	AlGaN+InAlN +InAlGaN
Case C	AlGaN+InAlGaN+InAlN
Case D	InAlN+AlGaN+InAlGaN
Case E	InAlGaN+AlGaN+InAlN
Case F	InAlGaN+InAlN+AlGaN

Table 5.4 presents a comparison of parameters for HEMT structures with a symmetric triple-material barrier with barrier thicknesses of 10, 12, and 17 nm. The transfer characteristics (I_D-V_G) of these devices are compared at a V_D of 0.5 V, with the gate-source voltage varying from -8 V to 1 V in increments of 0.1 V. The simulation results (Table 5.4) indicate that, similar to dual-material barrier structures, the g_m values for all cases exceed those obtained with a single AlGaN barrier layer (247 mS/mm). In all cases, g_m increases as the length of the 1st barrier material increases to 1.25 µm. The maximum g_m values of 370 mS/mm and 471 mS/mm are obtained in Case F and Case C (symmetric structures of 10 nm) for barrier lengths of up to 1 µm and 1.25 µm, respectively. The simulation result for V_{th} shows that, in certain cases, the V_{th} shifts to more positive values compared to the structure of the single AlGaN barrier layer (V_{th} = -1.59 V, Table 5.2). Cases B, C, and F show a shift in V_{th} to a more positive value when the length of the first barrier material increases to 1.25 µm, while Cases A, D, and E show the reverse. Case E (symmetric structures of 10 nm) has the least negative V_{th} value of -0.39 V and -0.44 V for 1st barrier material lengths up to 1 µm and 1.25 µm, respectively.

For $I_{G\_Leakage,}$ in symmetric HEMT structures (10, 12, 17 nm), Cases A, B, and C show a decrease in $I_{G\_Leakage}$ as the length of the 1st barrier layer increases to

1.25 µm, while Cases D, E, and F show an increase (Table 5.4). Case D in the 10 nm symmetric structure has the lowest $I_{G\_Leakage}$ (0.011 and 0.038 mA/mm, respectively). Table 5.4 also shows the I_{dss} comparison for all scenarios when the I_D-V_D characteristics are measured at V_G = 0 V and a V_D of up to 8 V. The simulation results indicate that, in most cases, the I_{dss} values surpass those of the single-barrier AlGaN/GaN HEMT (0.893 A/mm). Cases B, C, and F show a decrease in I_{dss} as the length of the 1st barrier layer increases to 1.25 µm, while Cases A, D, and E show an increase. In particular, Case F in the 17 nm symmetric HEMT structure achieves the highest I_{dss} for both 1 µm and 1.25 µm lengths of the first barrier material. A comparison of V_{br} indicates that in Cases A, D, E, and F, V_{br} decreases as the length of the first barrier material increases to 1.25 µm, while in Cases B and C, an increase is observed. This trend holds true across all barrier thicknesses. Notably, the maximum V_{br} for first barrier material lengths of up to 1 µm and 1.25 µm is achieved in the 17 nm symmetric structure of Case F, with values of 569 V and 566 V, respectively.

Table 5.4. Parameters comparison of triple-material barrier structures

	Barrier Thickness	**10 nm**		**12 nm**		**17 nm**	
	1st Material Length	**Up to 1 µm**	**Up to 1.25 µm**	**Up to 1 µm**	**Up to 1.25 µm**	**Up to 1 µm**	**Up to 1.25 µm**
Parameters	**Cases**						
g_m (mS/mm)	Case A	361	404	334	372	272	312
	Case B	352	469	319	425	256	348
	Case C	364	471	324	428	263	350
	Case D	358	439	320	399	257	324
	Case E	370	444	332	407	266	332
	Case F	379	470	341	420	279	346
V_{th} (V)	Case A	-2.01	-2.06	-2.68	-2.73	-4.32	-4.39
	Case B	-2.55	-0.47	-3.32	-0.80	-5.25	-1.65
	Case C	-2.00	-0.46	-2.66	-0.80	-4.31	-1.65
	Case D	-0.40	-0.45	-0.73	-0.79	-1.58	-1.64
	Case E	-0.39	-0.44	-0.73	-0.79	-1.57	-1.64
	Case F	-2.55	-2.12	-3.32	-2.77	-5.24	-4.43
	Case A	3	2	3	2	3	2
	Case B	0.9	0.6	0.9	0.5	0.8	0.5
	Case C	20	19	21	19	20	19

$I_{G\_Leakage}$	Case D	0.011	0.038	0.011	0.039	0.014	0.044
	Case E	0.2	28	0.2	29	0.4	37
	Case F	0.6	68	0.7	28	1	35
I_{dss} (A/mm)	Case A	1.913	2.020	2.378	2.550	2.838	2.876
	Case B	1.721	0.375	2.069	0.648	2.335	1.269
	Case C	1.372	0.355	1.706	0.620	2.333	1.223
	Case D	0.266	0.500	0.480	0.778	1.001	1.400
	Case E	0.263	0.481	0.474	0.750	0.983	1.339
	Case F	2.375	2.183	2.784	2.645	2.961	2.912
V_{br} (V)	Case A	555	516	560	545	560	206
	Case B	365	511	395	429	426	486
	Case C	379	394	385	422	384	471
	Case D	541	368	535	359	567	351
	Case E	493	340	475	337	540	325
	Case F	493	470	532	531	569	566

Further observations were made while comparing the traditional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMT structures to the triple-material symmetric barrier structures. The following summary of the result is based on all the simulated structures with a 1st barrier material length of up to 1 µm. Firstly, the 10 nm symmetric structure of Case F (InAlGaN+InAlN+AlGaN) achieves the highest g_m of 379 mS/mm, surpassing AlGaN/GaN but falling short of InAlN/GaN and InAlGaN/GaN HEMT structures. In terms of V_{th}, Case E (InAlGaN+AlGaN+InAlN) in the 10 nm symmetric structure records the maximum shift of V_{th} toward a more positive value (-0.39 V), which is more positive compared to single-barrier HEMT structures. Case D (InAlN+AlGaN+InAlGaN) in the 10 nm symmetric structure shows the lowest $I_{G\_Leakage}$ at 0.011 mA/mm, outperforming traditional structures. Considering I_{dss}, Case F (InAlGaN+InAlN+AlGaN) in the 17 nm symmetric structure achieves the highest I_{dss} of 2.96 A/mm, exceeding AlGaN/GaN and InAlGaN/GaN HEMT structures, and also provides the highest V_{br} of 569 V, which is higher than InAlN/GaN and InAlGaN /GaN but lower than AlGaN/GaN HEMT structures.

The performance comparison (Fig. 5.9) of single-material, dual-material (Case III), and triple-material (Case F) barrier GaN HEMTs shows clear benefits for each setup. Among the single-material barriers, AlGaN demonstrates the highest V_{br}

at 712 V, making it ideal for applications requiring high reliability, though its I_{dss} of 0.893 A/mm is the lowest due to limited 2DEG density. In contrast, InAlN offers the highest I_{dss} of 3.726 A/mm, leveraging its superior 2DEG density, but suffers from a significantly lower V_{br} of 348 V and a higher gate leakage current. InAlGaN strikes a balance, with an I_{dss} of 2.230 A/mm and a V_{br} of 389 V, making it a middle-ground option. Moving to dual-material barriers, 17 nm Case III (AlGaN + InAlN) improves upon the single-material structures by achieving a V_{br} of 404 V and an I_{dss} of 2.34 A/mm, providing a balanced solution with enhanced current handling and moderate V_{br}. However, the triple-material barrier configuration of 17 nm Case F (InAlGaN + InAlN + AlGaN) outperforms all other structures, achieving the highest I_{dss} of 2.96 A/mm while sustaining a robust V_{br} of 569 V. This makes Case F the most promising design for ultra-high-power applications, as it effectively combines the strengths of the individual materials to deliver superior overall performance.

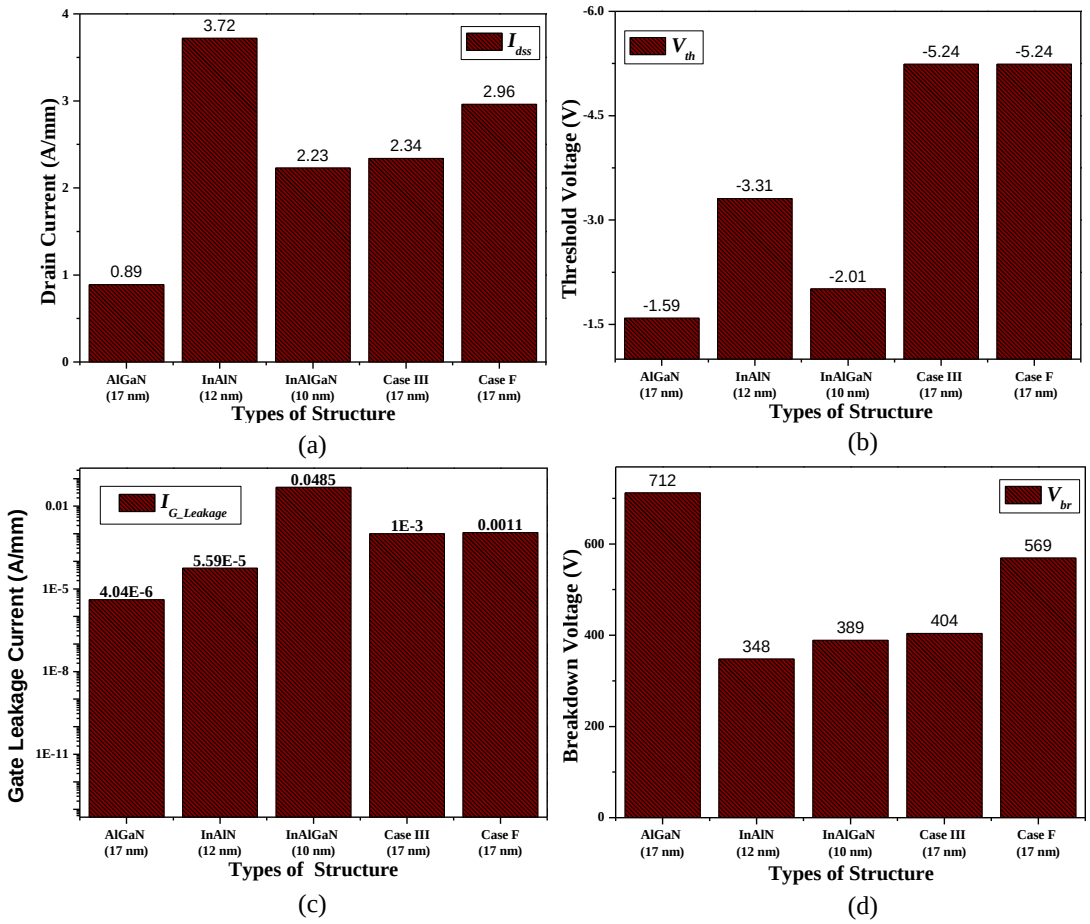


Fig. 5.9. Evaluation of electrical performance metrics (a), (b), (c), and (d) for single, dual (Case III, 17 nm), and triple (Case F, 17 nm) material barrier GaN HEMTs.

5.5 Summary

The investigation demonstrated that the electrical performance of devices can be significantly influenced by barrier layer engineering techniques, including adjustments in the composition and thickness of the alloy. InAlN/GaN and InAlGaN/GaN HEMTs are anticipated to demonstrate enhanced drain current and g_m compared to traditional AlGaN/GaN HEMTs, owing to the increased 2DEG density resulting from the effective polarization of InAlN and InAlGaN. Despite their advantages, the practical use of these materials in ultra-high-power applications has been limited due to their high leakage current and low breakdown voltages. Innovative asymmetric and symmetric designs utilizing InAlN, InAlGaN, and AlGaN barriers have been introduced to address the trade-off between achieving high drain current and maintaining high V_{br}. These structures integrate the positive aspects of conventional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMTs. This novel structure outperforms its conventional counterparts, with high drain current, excellent g_m, and superior V_{br}. This device is ideal for ultra-high-power applications.

Comparing the traditional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMT structures with the dual-material asymmetric and symmetric structures, we have seen that Case II (InAlGaN+AlGaN) in the 17 nm symmetric structure shows a V_{br} of 723 V and an I_{dss} of 0.972 A/mm, outperforming the AlGaN/GaN HEMT in both metrics with an I_{dss} value lower than InAlN/GaN and InAlGaN/GaN HEMT structures. On analyzing these values with the three traditional devices, Case III (AlGaN+InAlN) in the 17 nm symmetric structure yields the optimised results, with V_{br} of 404 V and I_{dss} of 2.34 A/mm. For triple-material symmetric barrier structures, Case F (InAlGaN+InAlN+AlGaN) of a 17 nm symmetric HEMT structure achieves the highest I_{dss} of 2.96 A/mm, exceeding AlGaN/GaN and InAlGaN/GaN HEMT structures, and also provides the highest V_{br} of 569 V, which is higher than InAlN/GaN and InAlGaN/GaN but lower than AlGaN/GaN HEMT structures. Overall, Case F (17 nm) of the triple-material barrier structure demonstrates superior performance compared to Case III (17 nm) of the dual-material barrier structure in terms of V_{br} and I_{dss}. Traditional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMTs exhibit $I_{G\_leakage}$ values ranging from 3.50-4.06 µA/mm, 57.5-72.6 µA/mm,

and 0.048-0.053 A/mm, respectively. In dual and triple-material barrier structures, improvements in $I_{G\_leakage}$ are noted primarily for InAlGaN material, though AlGaN and InAlN materials show no noticeable improvement. Thus, the HEMT structure can be optimized for the desired performance by selecting the appropriate barrier material combination.

CHAPTER 6

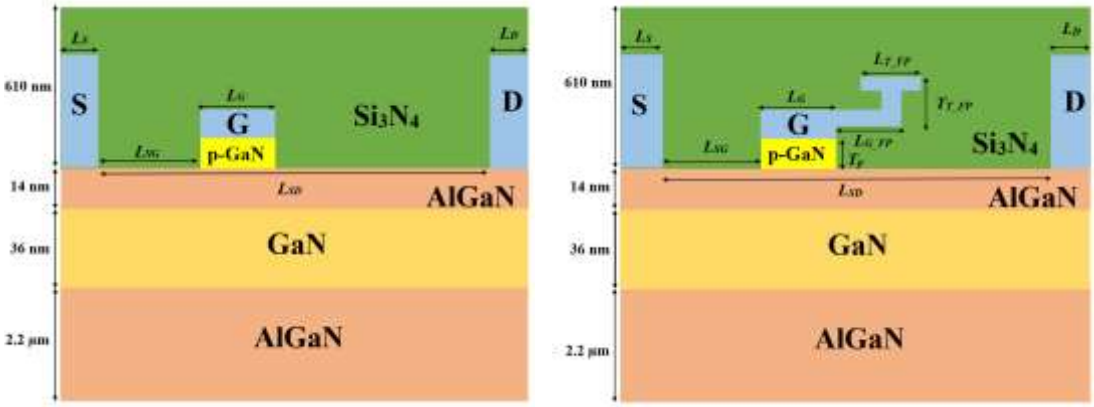
A Novel Double-Deck Gate Field Plate Design for Normally-Off AlGaN/GaN HEMTs

6.1 Introduction

GaN HEMTs are well-suited for high-power and high-frequency applications due to their heterojunction's 2DEG, which delivers both high charge carrier density and excellent electron mobility. However, because the 2DEG naturally exists in AlGaN/GaN heterostructures, conventional HEMTs operate in a Normally-On (depletion-mode) state. For power electronics, Normally-Off (enhancement-mode) operation is desirable to simplify circuit design and ensure safe operation. To achieve this, various techniques have been developed, including gate recess structures [258], p-GaN gate architectures [259]–[260], and fluorine treatment [89]. Among these, the p-GaN gate approach is widely studied due to its reliable performance and effective Normally-Off characteristics. As previously discussed, a high breakdown voltage (V_{br}) is vital for power devices, as it limits the maximum biasing voltage and impacts output power and reliability [261]. To achieve higher V_{br}, FP structures are employed in AlGaN/GaN HEMTs to reduce field crowding [262]–[263] and suppress virtual gate formation, thereby enhancing transient performance [112]. Field plate (FP) configurations can be categorized based on their placement, including single gate, source, and drain-FPs, as well as dual (source-gate, source-drain, gate-drain) and triple (source-gate-drain) FPs. This chapter presents a Normally-Off AlGaN/GaN HEMT with an innovative double-deck gate-FP structure to enhance V_{br}. Additionally, the study examines the impact of passivation materials with relative permittivity (ε_r) values ranging from 3.9 to 22 on breakdown and DC performance on a Normally-Off HEMT. The combined use of FPs and high-ε_r materials reduces the peak electric field near the gate's drain edge, thereby improving V_{br}. To evaluate breakdown behavior, multiple FP configurations—including triple, dual, and single gate-FPs—are implemented simultaneously in the HEMT structure. A detailed investigation is conducted, varying FP lengths and source-drain spacing to optimize performance.

6.2 Overview of the Normally-Off HEMT Structure

A normally-off AlGaN/GaN HEMT with and without a double-deck gate-FP design is proposed, as illustrated in the schematic cross-section view of Fig. 6.1 (not to scale). The device has an L_G of 1.4 µm, an L_{SG} of 1 µm, and a total L_{SD} of 13.4 µm. The epitaxial layers consist of an AlGaN buffer of 2.2 µm, a GaN channel of 36 nm thickness, and an AlGaN barrier of 14 nm thickness with 24% aluminum content. The p-GaN layer has a carrier concentration of 3×10^{19} cm^{-3}, while the Si_3N_4 passivation layer is 0.6 µm thick. The gate-FP (L_{G_FP}) extends 1.6 µm, the upper T-shaped gate-FP has a length (L_{T_FP}) of 1.4 µm and a height (T_T) of 0.1 µm, with all FPs having a uniform thickness of 0.05 µm. The same physics models and simulator validation approach described in Section 3.2 are applied here. The same simulation framework is maintained for all structural analyses in this work.



(a) (b)

Fig. 6.1. Structure of an AlGaN/GaN HEMT with Si_3N_4 passivation (a) without-FP, and (b) with a double-deck gate-FP.

Fig. 6.2 illustrates the preliminary fabrication steps for the proposed AlGaN/GaN HEMT. The process begins with the deposition of an AlGaN buffer layer on the substrate via metal-organic chemical vapor deposition (MOCVD) (Fig. 6.2(a)). Subsequently, the MOCVD technique can be employed to grow the GaN channel layer over the buffer layer (Fig. 6.2(b)), followed by the AlGaN barrier layer on the channel (Fig. 6.2(c)), and finally, the p-GaN cap layer atop the barrier layer (Fig. 6.2(d)). MOCVD is widely used in industry to produce highly pure crystalline semiconductor thin films. After forming the GaN cap layer, the source and drain ohmic contact regions can be patterned using reactive ion etching (RIE)

(Fig. 6.2(e)). Finally, the ohmic contacts are to be formed through electron beam evaporation (Fig. 6.2(f)). Next, the Schottky gate contact area are to be defined via

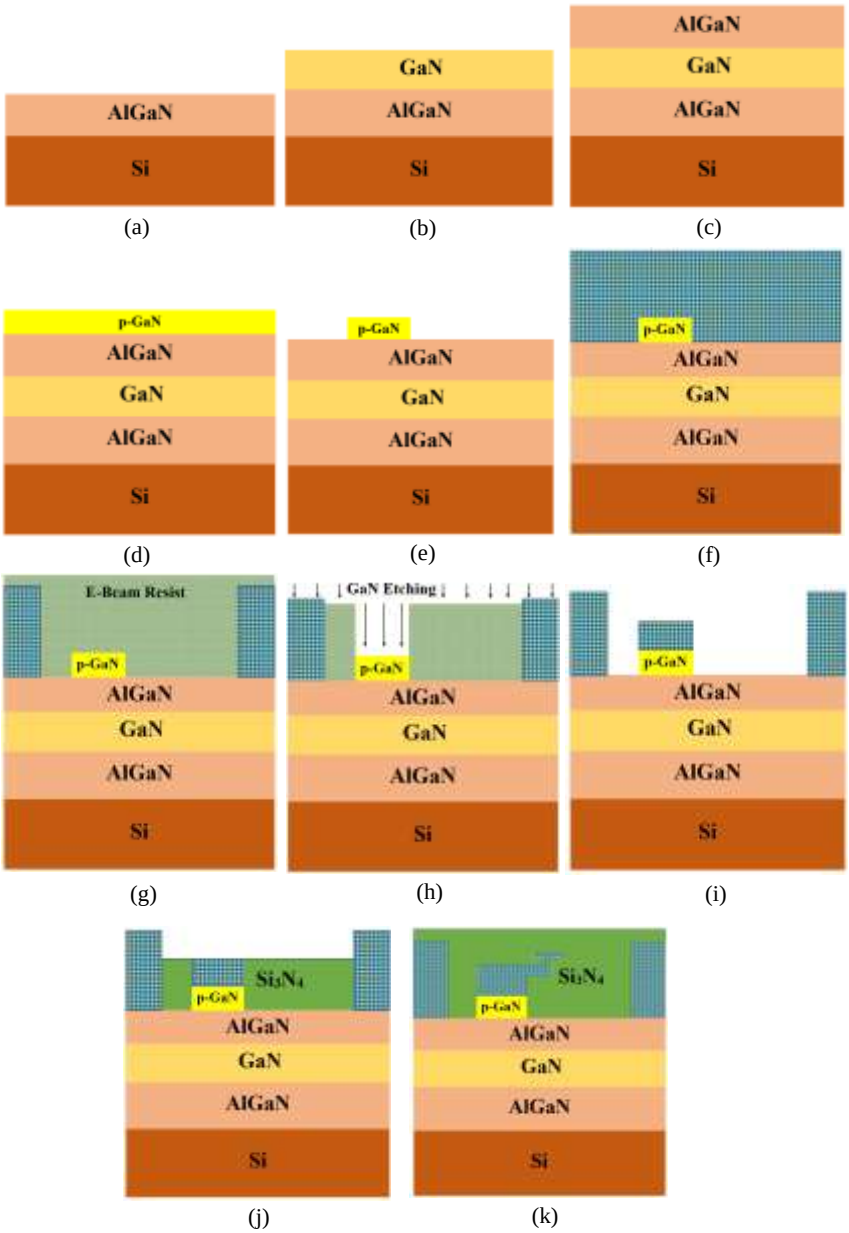


Fig. 6.2. Fabrication steps for the proposed AlGaN/GaN HEMT include: (a) Depositing a buffer layer on a Si substrate via MOCVD. (b) Forming the GaN channel layer using MOCVD. (c) Growing the AlGaN barrier layer through MOCVD. (d) Adding a GaN cap layer using MOCVD. (e) Performing mesa etching to define openings for ohmic source and drain contacts. (f) Fabricating source and drain ohmic contacts via e-beam evaporation. (g) Applying an e-beam resist coating. (h) Etching the GaN cap layer to prepare for gate formation. (i) Depositing gate metal to form the gate electrode. (j) Depositing a passivation layer using chemical vapor deposition (CVD). (k) Forming gate-FP by metal deposition.

RIE dry etching, followed by the application of an E-beam resist coating (Fig. 6.2(g)). The gate structure will be completed by etching the GaN cap layer after removing the E-beam resist (Fig. 6.2(h)), preparing the device for gate metal deposition (Fig. 6.2(i)). A passivation layer will then be deposited using chemical vapor deposition (CVD) (Fig. 6.2(j)). Finally, gate-FP will be fabricated through multiple stages of passivation and metallization (Fig. 6.2(k)).

First, an AlGaN/GaN HEMT with Si_3N_4 passivation but without FP structure is compared to the proposed design, which features a novel double-deck gate-FP, as illustrated in Fig. 6.1. Both the conventional and proposed double-deck gate-FP structures share identical channel, cap, buffer, and barrier layers. A comparison of their transfer (I_D-V_G) characteristics and g_m is presented in Fig. 6.3.

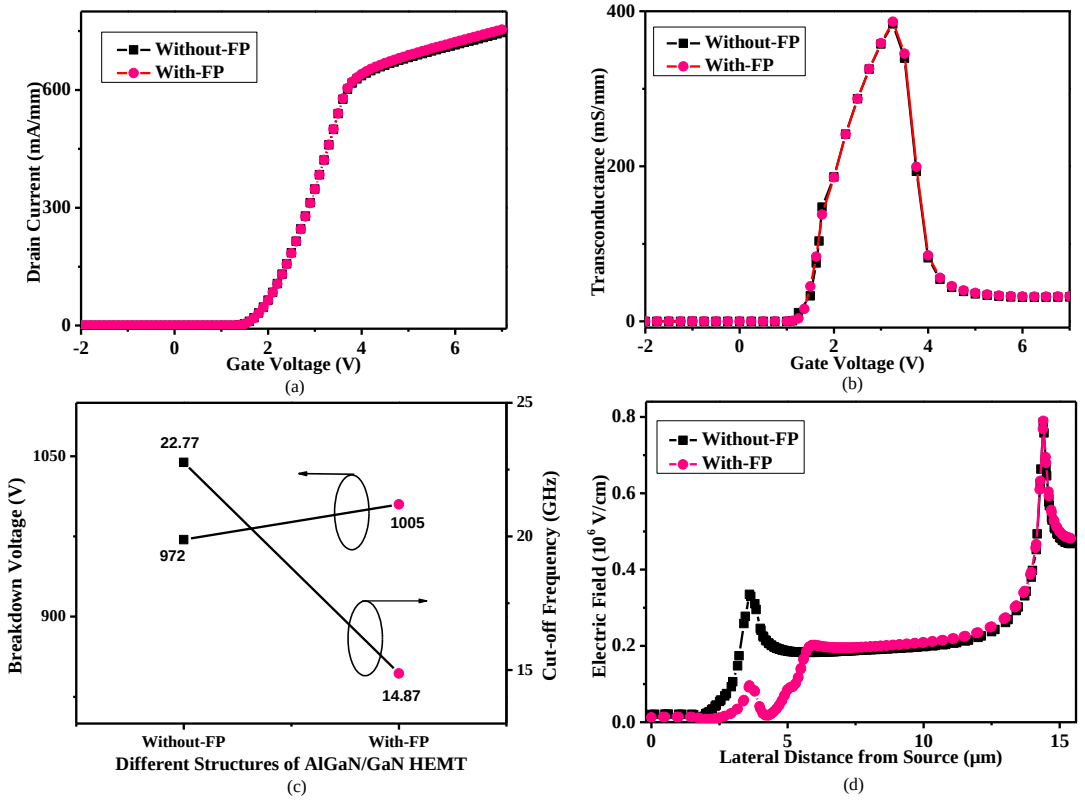


Fig. 6.3. Performance comparison between conventional and double-deck gate-FP AlGaN/GaN structures with Si_3N_4 passivation: (a) I_D-V_G characteristics, (b) g_m, (c) V_{br} and f_T, and (d) electric field distribution.

The I_D-V_G characteristics of both structures—with and without an FP—are shown for a drain voltage (V_D) of 15 V and a gate voltage (V_G) ranging from -2 V to 7 V. The

conventional structure (without-FP) exhibits a peak g_m of 0.383 S/mm, while the structure with double deck gate-FP reaches 0.386 S/mm. Both designs achieve a maximum drain current (I_{dmax}) of 739 mA/mm, which results from electron accumulation in the GaN channel. Surface states drive this accumulation on the GaN cap layer and the polarized charge at the AlGaN/GaN interface. Analysis of the breakdown characteristics shows that the traditional structure has a lower V_{br} of 972 V, whereas the proposed double-deck gate-FPs achieve a higher V_{br} of 1005 V (Fig. 6.3(c)). The accumulation of potential lines near the drain side of the gate creates an electric field peak. In contrast, the use of FPs results in a more spread-out electric field profile, enhancing the V_{br} in comparison to the conventional design, as illustrated in Fig. 6.3(d). Furthermore, incorporating an FP structure enhances the electric field uniformity [111], which is observable in Fig. 6.3(d).

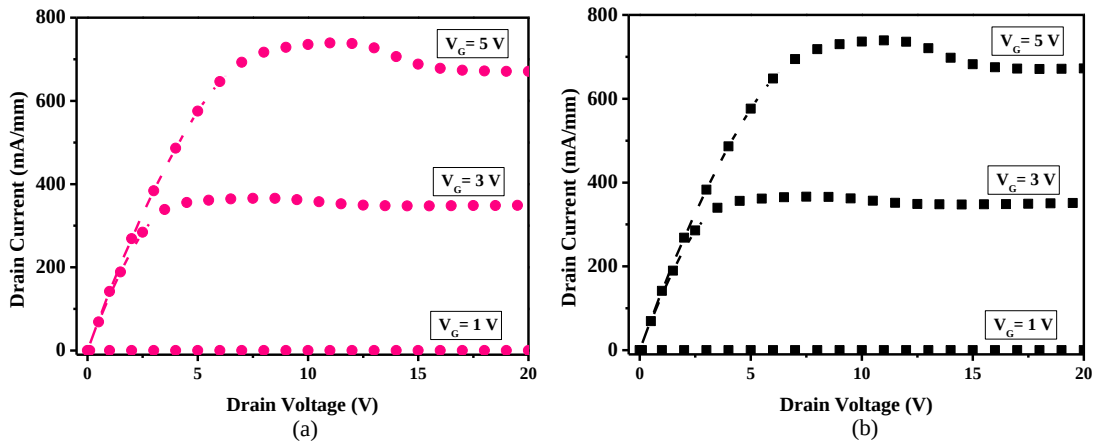


Fig. 6.4. Output characteristics of AlGaN/GaN HEMTs at different V_G: (a) with-FP, and (b) without-FP.

Fig. 6.4 shows the output characteristics of AlGaN/GaN HEMTs at different V_G, both with-FP (Fig. 6.4(a)) and without-FP (Fig. 6.4(b)). In both cases, the drain current increases with the V_D and tends to saturate at higher voltages. It can be observed that the drain current is slightly higher for the device with-FP, indicating improved current conduction and electric field distribution. The inclusion of the FP helps to reduce the peak electric field at the gate edge, thus enhancing device performance and reliability. As the V_G increases from 1 V to 5 V, the drain current

also increases significantly, demonstrating the typical output behavior of enhancement-mode AlGaN/GaN HEMTs.

6.3 Impact of Different Passivation Materials on Device Performance

Passivation layers shield the device surface from external environmental effects while also mitigating peak electric field concentrations near the drain-side gate edge, thereby enhancing the V_{br}. To analyze their impact, various passivation materials—including Si_3N_4, Al_2O_3, $HfSiO_4$, and HfO_2—were evaluated for the proposed AlGaN/GaN HEMT structures incorporating FPs. Key performance metrics such as threshold voltage (V_{th}), gate current (I_G) at V_G = +5 V, and I_{dmax} were assessed and tabulated in Table 6.1.

Table 6.1. Performance comparison of different passivation materials

Parameters	SiO_2	Si_3N_4	Al_2O_3	$HfSiO_4$	HfO_2
ε_r	3.9	7.5	9.3	12	22
V_{th} (V)	1.36	1.36	1.36	1.37	1.38
$I_{G,VG=5V}$ (μA/mm)	0.368	0.368	0.367	0.366	0.358
I_{dmax} (mA)	738	739	739	740	741
R_{on} (Ω mm)	2.60	2.58	2.57	2.55	2.39

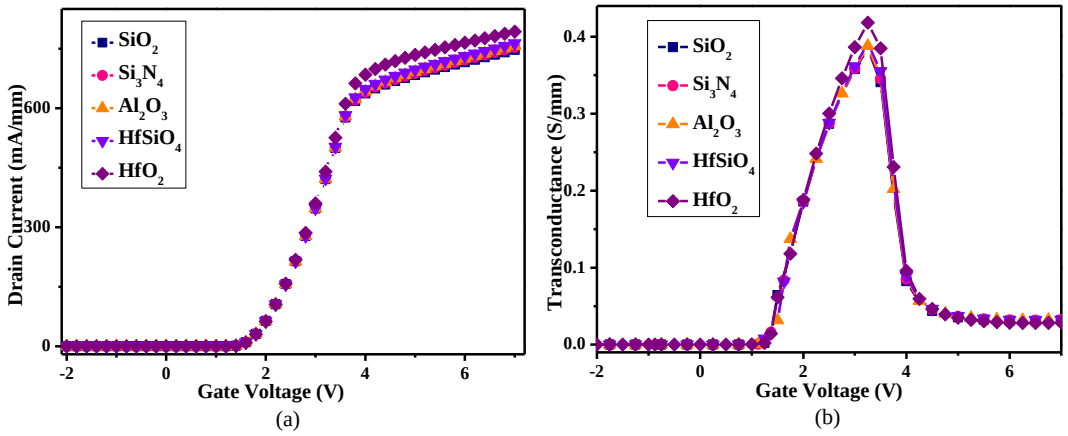


Fig. 6.5. Performance analysis of a double-deck gate-FPs AlGaN/GaN HEMT: (a) I_D-V_G characteristics and (b) g_m under different passivation materials.

I_D-V_G characteristics, on-resistance (R_{on}), and g_m comparisons across materials are illustrated in Fig. 6.5. The V_{th} exhibited minimal variation (1.36 V to 1.38 V) with different passivation layers. On-state gate current ranged between 0.358 µA/mm and 0.368 µA/mm, while I_{dmax} varied from 738 mA/mm to 741 mA/mm. Notably, both I_{dmax} and g_m improved with higher dielectric constants (ε_r), with HfO_2 delivering the highest I_{dmax} (741 mA/mm) and peak g_m (0.418 S/mm). In contrast, SiO_2-passivated structures exhibited the lowest g_m (0.384 S/mm). Conversely, R_{on} increased for lower-ε_r materials, with SiO_2 yielding the highest R_{on} (2.60 Ω·mm) and HfO_2 the lowest (2.39 Ω·mm).

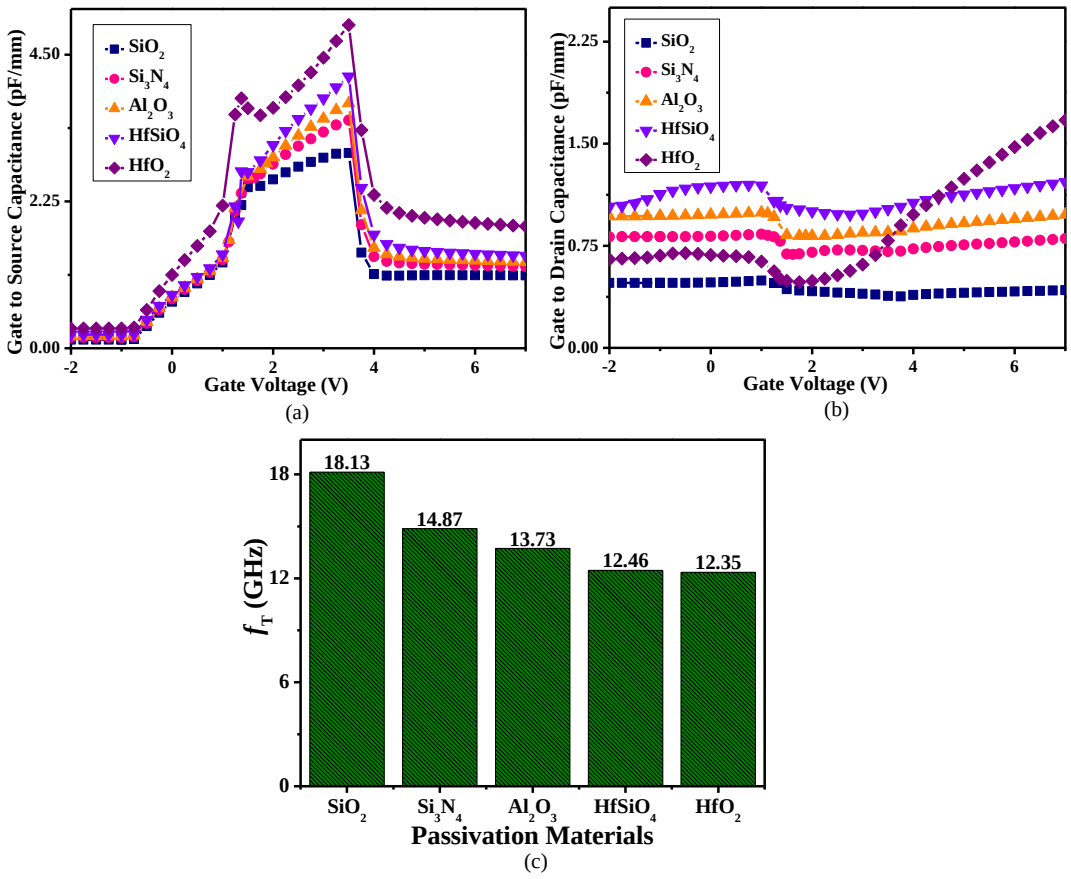


Fig. 6.6. A double-deck gate-FPs AlGaN/GaN HEMT evaluated with various passivation materials, analyzing (a) C_{gs}, (b) C_{gd}, and (c) f_T.

Fig. 6.6 illustrates the variation in gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and cut-off frequency (f_T), for different dielectric passivation materials. The results indicate that a higher ε_r of the passivation layer leads to a

significant rise in both C_{gs} and C_{gd}, consequently reducing f_T. This increase in capacitance is primarily due to enhanced electron accumulation in the channel. For instance, an AlGaN/GaN HEMT passivated with SiO_2 exhibits a C_{gs} of 2.981 pF/mm, whereas the HfO_2-passivated device shows a much higher C_{gs} of 4.710 pF/mm. Since f_T is directly influenced by C_{gs} and C_{gd}, it degrades from 18.13 GHz (SiO_2) to 12.35 GHz (HfO_2).

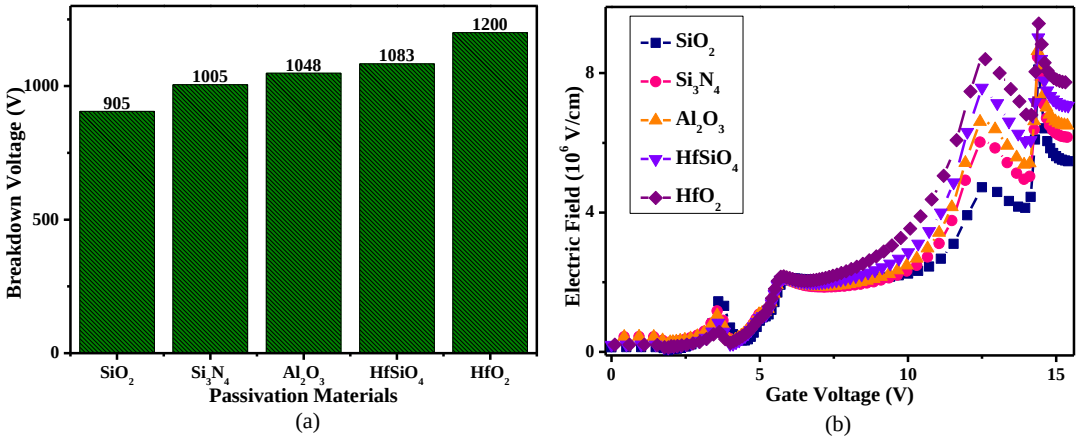


Fig. 6.7. Comparison of (a) V_{br} and (b) electric field in AlGaN/GaN HEMTs with-FPs using various passivation materials.

Fig. 6.7 compares the V_{br} and electric field distribution for various passivation materials. The findings show that a higher ε_r of the passivation material leads to a gradual reduction in the maximum electric field near the edge of the gate electrode. Among the assessed materials, the HfO_2-passivated structure achieves the highest V_{br} (1200 V), demonstrating that V_{br} improves with higher ε_r. The higher permittivity of the passivation layer shifts the high-field region closer to the drain. It decreases electric field buildup near the gate's drain-side edge at the AlGaN/GaN interface, improving breakdown performance [229]. Based on these findings, HfO_2 is selected as the optimal passivation dielectric for this study. Further analysis examines breakdown characteristics across different device structures, varying source-to-drain distances (L_{SD}), and multiple FP lengths.

6.4 Comparative Study of Different Field Plate Configurations

To investigate the influence of multiple FPs on the proposed structure, four different FP configurations (Fig. 6.8) are analysed. The first configuration (Case I) incorporates conventional FPs at the source and drain, along with a double-deck FP at the gate. The second (Case II) employs a dual-FP arrangement, combining a double-deck FP at the gate with a conventional FP at the drain. The third (Case III) consists of a conventional FP at the source and a double-deck FP at the gate. Finally, the fourth configuration (Case IV) uses only a single double-deck FP at the gate. These configurations are evaluated to assess their DC and analog performance. Structure dimensions are given in section 6.2 with the addition of source-FP length (L_{S_FP}) and drain-FP length (L_{D_FP}).

The source-FP consists of a metal layer linked to the HEMT's source electrode, situated over the AlGaN barrier layer and stretching towards the gate region. Its main functions are to improve current distribution throughout the channel and minimize leakage current. The gate-FP is a metal layer above the gate electrode, extending toward the drain and overlapping the source-FP, enhancing gate control and reducing access resistance. The drain-FP, a metal layer connected to the drain electrode and placed over the AlGaN barrier, extends toward the gate, reducing impact ionization and preventing current collapse.

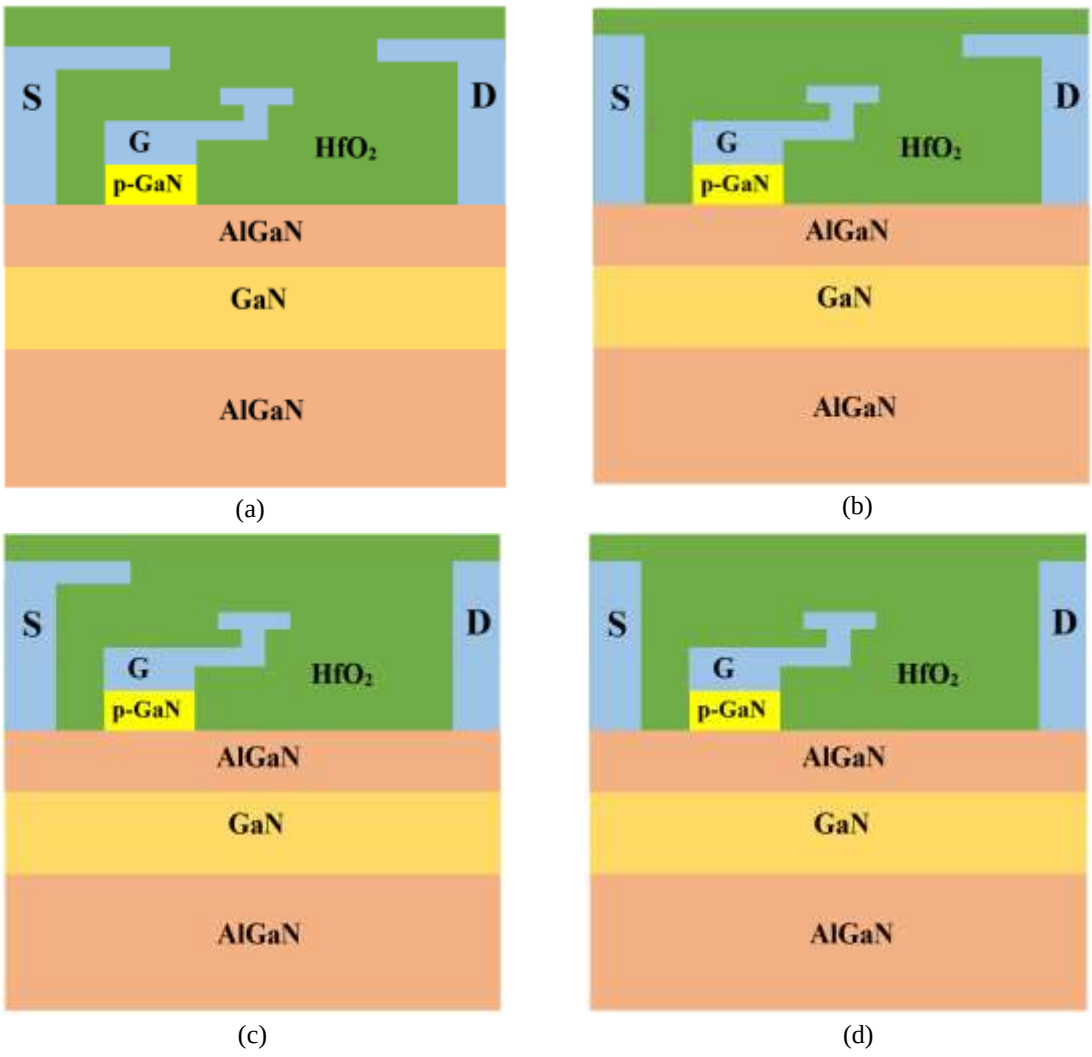


Fig. 6.8. Schematic illustrations of various AlGaN/GaN HEMT structures featuring different FP designs: (a) Case I, (b) Case II, (c) Case III, and (d) Case IV.

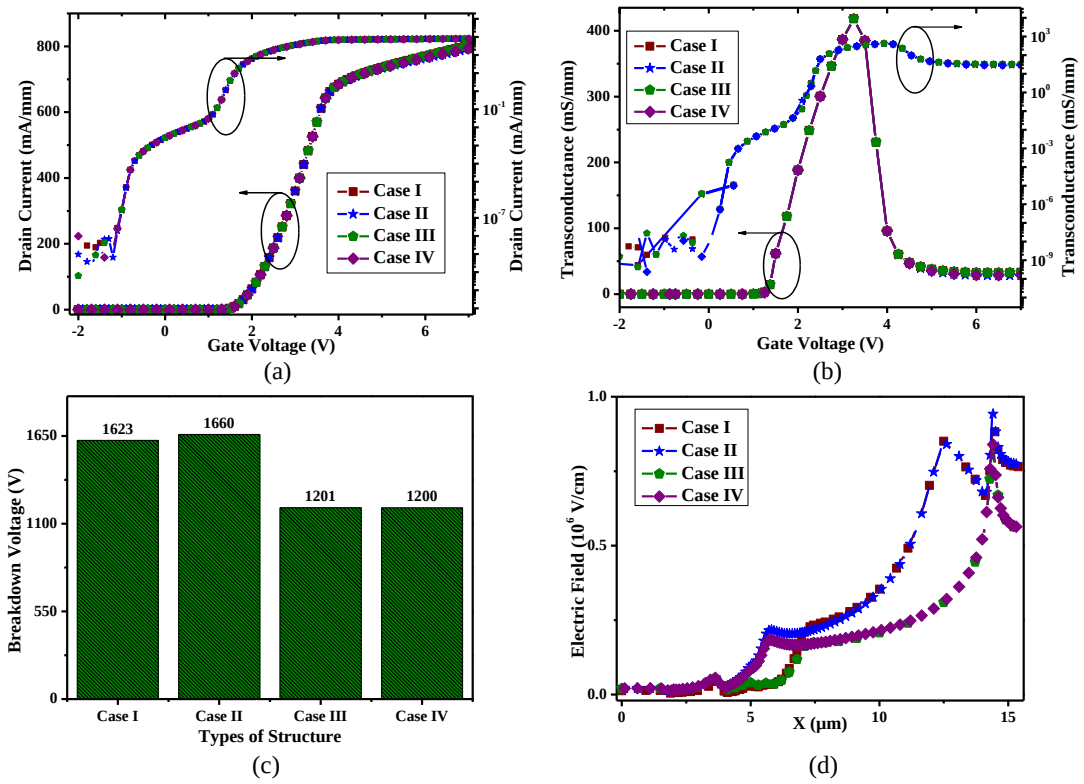


Fig. 6.9. Comparison of various AlGaN/GaN HEMT structures in terms of (a) I_D-V_G characteristics and (b) g_m, (c) V_{br}, and (d) electric field characteristics.

Fig. 6.9 presents the I_D-V_G characteristics and g_m comparison for the structures mentioned above. The evaluated drain current and g_m (0.418 S/mm) remain nearly identical across all configurations. Table 6.2 summarizes the V_{th}, $I_{G,VG=5V}$, and I_{dmax} for the four structures. In the on-state, the gate current varies between 0.356 μA/mm and 0.358 μA/mm, while the drain current ranges from 740 mA/mm to 741 mA/mm. Notably, the gate current is five orders of magnitude lower than the drain current, with all structures exhibiting gate leakage well within acceptable limits. These results indicate that modifying the FP configuration has minimal impact on DC performance. However, significant improvements are observed in breakdown characteristics and electric field distribution within the channel.

Fig. 6.9(d) shows the electric field distributions for all four cases. The FPs redistribute the peak field, spreading it between the gate and drain. In Case I, the electric field peaks appear at the edges of the gate, source-FP, and drain-FP. Similarly, in Case II, peaks are observed at the gate edge, gate-FP, and drain-FP.

Both cases demonstrate a more even electric field distribution, resulting in a higher V_{br}. The drain-connected FP further reduces the peak field near the drain, improving V_{br}. Cases I and II achieve the highest V_{br} values (1623 V and 1660 V, respectively), while Cases III and IV, lacking a drain-FP, show lower V_{br} (1201 V and 1200 V, Fig. 6.9(c)).

Table 6.2. Performance comparison of various AlGaN/GaN HEMT configurations

Parameters	**Case I: Double deck gate-FP and conventional FP at the Source and Drain**	**Case II: Double deck gate-FP and conventional FP at the Drain**	**Case III: Double deck gate-FP and conventional FP at the Source**	**Case IV: Double deck gate-FP**
V_{th} (V)	1.38	1.38	1.38	1.38
$I_{G,\ VG\ =\ 5V}$ (μA/mm)	0.356	0.358	0.356	0.358
I_{dmax} (mA/mm)	740	741	740	741

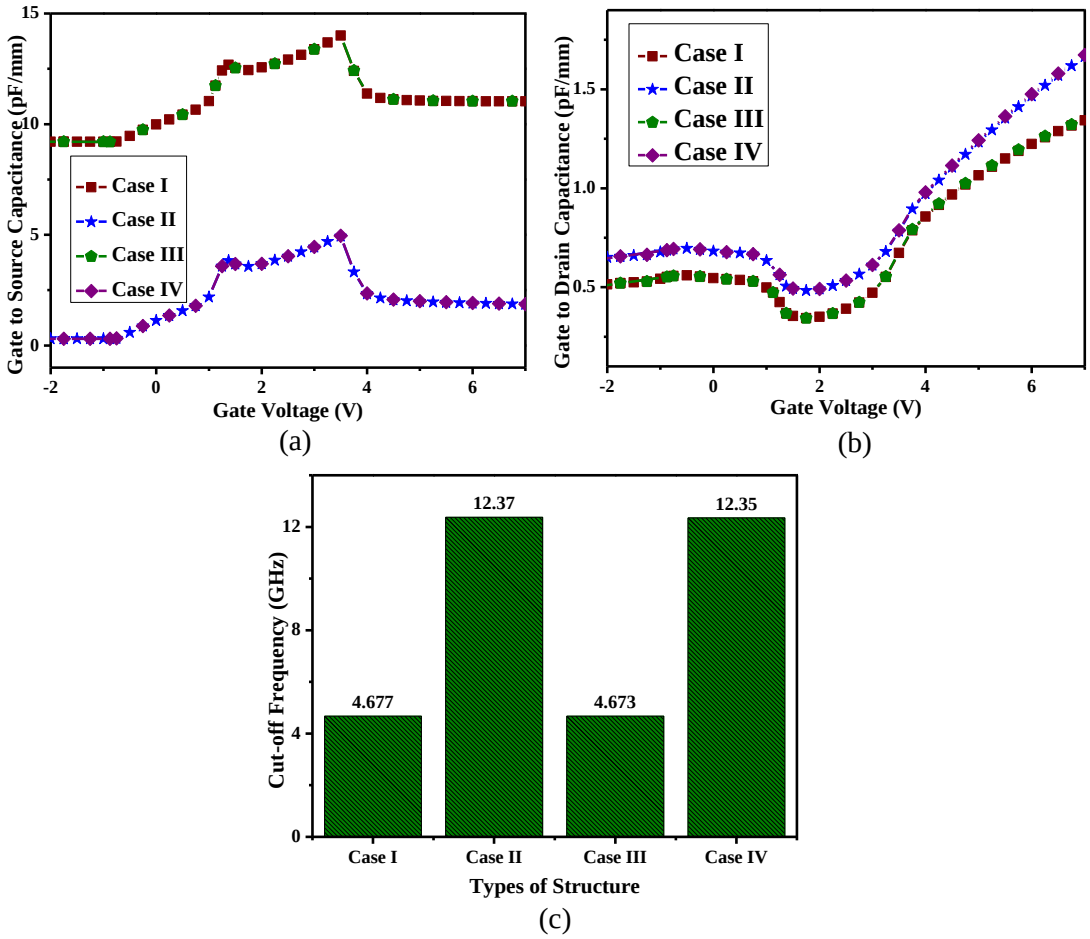


Fig. 6.10. Comparison of various AlGaN/GaN HEMT structures in terms of (a) C_{gs}, (b) C_{gd}, and (c) f_T.

Fig. 6.10 compares C_{gs}, C_{gd} and f_T across different cases. The results indicate that Case I and Case III exhibit similar capacitance values, which is also true for Case II and Case IV. Specifically, both Cases I and III have a C_{gs} of 13.6 pF/mm, while Cases II and IV show lower C_{gs} values of 4.69 pF/mm and 4.71 pF/mm, respectively. Consequently, Cases I and III yield lower f_T values of 4.677 GHz and 4.673 GHz, while Cases II and IV demonstrate comparably higher f_T of 12.3 GHz each.

6.5 Impact of Structural Parameters on Various Field Plate Designs

Key structural parameters—such as the FP design, dimensions, thickness, and source-to-drain spacing—can significantly impact device performance. In the subsequent section, a detailed analysis of variations in L_{SD}, $L_{S\text{-}FP}$, $L_{D\text{-}FP}$ and $L_{G\text{-}FP}$ is

conducted across all structural configurations. The resulting device characteristics are compared to identify the optimal design for enhanced performance.

6.5.1 Impact of Source-Drain Spacing

Initially, the influence of L_{SD} is examined across four distinct structural configurations (Cases I to IV). To isolate this effect, all other parameters remain fixed while L_{SD} is varied. The relationship between V_{br} and electric field as a function of L_{SD} is illustrated in Fig. 6.11. Results indicate that V_{br} consistently rises with increasing L_{SD} in all cases. For this study, L_{SD} values range from 8.4 µm to 15.4 µm. Fig. 6.11 illustrates that as the L_{SD} increases across all structures, the peak electric field shifts from the gate edge toward the drain edge. This redistribution of the electric field leads to device breakdown occurring at higher V_D. For Case I, where the L_{SD} is 8.4 µm, as the V_D increases, the high-field region expands toward the drain. When the electric field at the drain-side edge of the gate reaches the critical breakdown threshold, breakdown occurs at V_D = 488 V. With larger L_{SD} values, the electric field intensity at the gate's drain edge diminishes. Notably, at L_{SD} = 15.4 µm, the electric field remains below the critical threshold even at V_D = 488 V, resulting in an increased V_{br} with greater L_{SD}. The highest V_{br} of 1717 V is achieved in Case I at an L_{SD} (lateral spacing distance) of 15.4 µm. The presence of three FPs helps distribute the electric field more effectively, reducing peak field concentration. In Case II, the high electric field region (Fig. 6.11(b)) extends to the drain, achieving a V_{br} of 927 V at L_{SD} = 8.4 µm, with a peak V_{br} of 1704 V at L_{SD} = 15.4 µm. For Cases III and IV, the maximum V_{br} values are 1215 V and 1211 V, respectively, both at L_{SD} of 15.4 µm. Beyond the FP edge, the electric field weakens, so increasing L_{SD} further does not improve V_{br} [223].

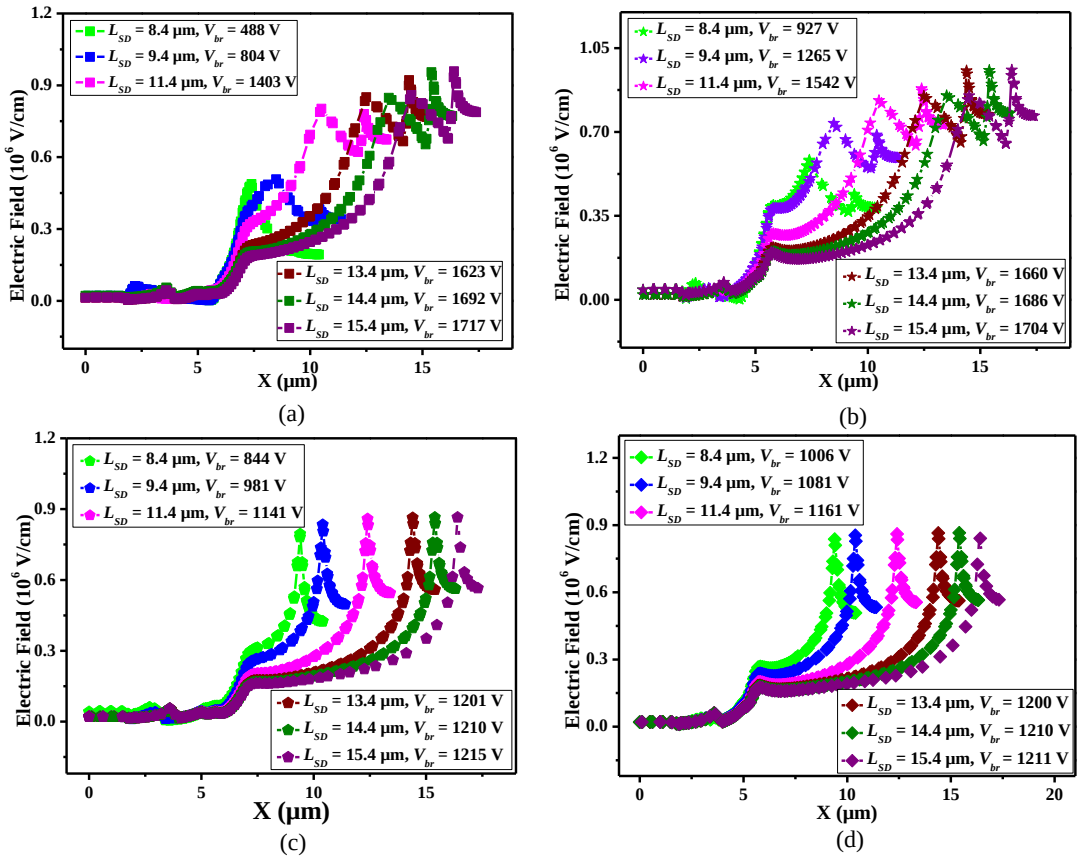


Fig. 6.11. Distribution of the electric field across the AlGaN/GaN heterojunction for four L_{SD} variations: (a) Case I, (b) Case II, (c) Case III, (d) Case IV.

Table 6.3. Electrical performance comparison of AlGaN/GaN HEMT structures with varying L_{SD}

L_{SD} (µm) / **Parameters**	**8.4**	**9.4**	**11.4**	**13.4**	**14.4**	**15.4**
g_m (S/mm)						
Case I	0.417	0.417	0.417	0.418	0.418	0.419
Case II	0.417	0.417	0.417	0.418	0.418	0.419
Case III	0.417	0.417	0.417	0.418	0.418	0.419
Case IV	0.417	0.417	0.417	0.418	0.418	0.419
C_{gs} (pF/mm)						
Case I	13.27	13.35	13.49	13.68	13.80	13.90
Case II	4.22	4.30	4.48	4.69	4.82	4.95
Case III	13.29	13.35	13.50	13.69	13.81	13.94
Case IV	4.23	4.31	4.49	4.71	4.83	4.97
C_{gd} (pF/mm)						
Case I	0.41	0.44	0.49	0.55	0.58	0.62
Case II	0.56	0.58	0.62	0.68	0.71	0.74

Case III	0.41	0.41	0.49	0.55	0.58	0.62
Case IV	0.56	0.58	0.62	0.68	0.71	0.74
f_T (GHz)						
Case I	4.85	4.81	4.75	4.67	4.63	4.58
Case II	13.89	13.60	13	12.37	12.04	11.69
Case III	4.84	4.81	4.75	4.67	4.62	4.58
Case IV	13.86	13.57	12.98	12.35	12.01	11.66
R_{on} (Ω. mm)						
Case I	2.397	2.395	2.393	2.389	2.387	2.384
Case II	2.395	2.394	2.392	2.390	2.388	2.386
Case III	2.396	2.395	2.393	2.389	2.387	2.384
Case IV	2.395	2.394	2.392	2.390	2.388	2.866

Table 6.3 shows a comparison of the total gate capacitance ($C = C_{gs}+C_{gd}$), f_T, g_m, and R_{on} across the four cases, plotted against L_{SD}. According to the analysis, Cases I and III demonstrate higher C values than Cases II and IV. This difference arises because Case I incorporates both source and drain-FPs (FPs), whereas Case IV has only a gate-FP. Similarly, in Case III, the addition of a source-FP alongside the gate-FP contributes to the increased capacitance. As L_{SD} increases, C rises for all cases, reaching peak values of 14.52 pF/mm (Case I) and 14.56 pF/mm (Case III) at L_{SD}= 15.4 µm. In contrast, Cases II and IV achieve maximum C values of 5.69 pF/mm and 5.71 pF/mm, respectively, at the same L_{SD}. Conversely, f_T declines with increasing L_{SD} in both structures. The highest f_T values occur at L_{SD} = 8.4 µm, with Case I, II, III, and IV yielding 4.85 GHz, 13.89 GHz, 4.84 GHz, and 13.86 GHz, respectively. Meanwhile, g_m shows an upward trend with L_{SD}, increasing from 0.417 S/mm (at L_{SD} = 8.4 µm) to 0.419 S/mm (at L_{SD} = 15.4 µm) in Case I. Cases II–IV follow a similar pattern, also reaching 0.419 S/mm at the maximum L_{SD}. On the other hand, R_{on} decreases slightly with L_{SD} across all cases. The lowest R_{on} values are 2.484 Ω·mm (Cases I and III) and 2.385 Ω·mm (Cases II and IV) at L_{SD} = 15.4 µm.

6.5.2 Impact of Source Field Plate Length Variation

This section examines the impact of source-FP length (L_{S_FP}) variation in Case I and Case III structures, as the other two structures lack a source-FP. Key device characteristics such as channel electric field profile, g_m, C, f_T, R_{on} and V_{br} are analysed and compared. The L_{S_FP} is adjusted from 1 to 7 µm. Results indicate that

V_{br} declines with increasing L_{S_FP} in both cases (Fig. 6.12). A longer L_{S_FP} leads to higher parasitic capacitance, particularly for materials with high permittivity. As shown in Fig. 6.12, the reduction in V_{br} with longer L_{S_FP} is attributed to the decreased distance between the FP edge and the drain, resulting in an intensified electric field that triggers breakdown [111]. For Case I (Fig. 6.12(a)), V_{br} measures 1651 V at an L_{S_FP} of 1 µm but drops to 1525 V at 7 µm. Similarly, in Case III (Fig. 6.12(b)), V_{br} starts at 1200 V for a 1 µm L_{S_FP} and progressively decreases with longer FP lengths, reaching 1183 V at 7 µm.

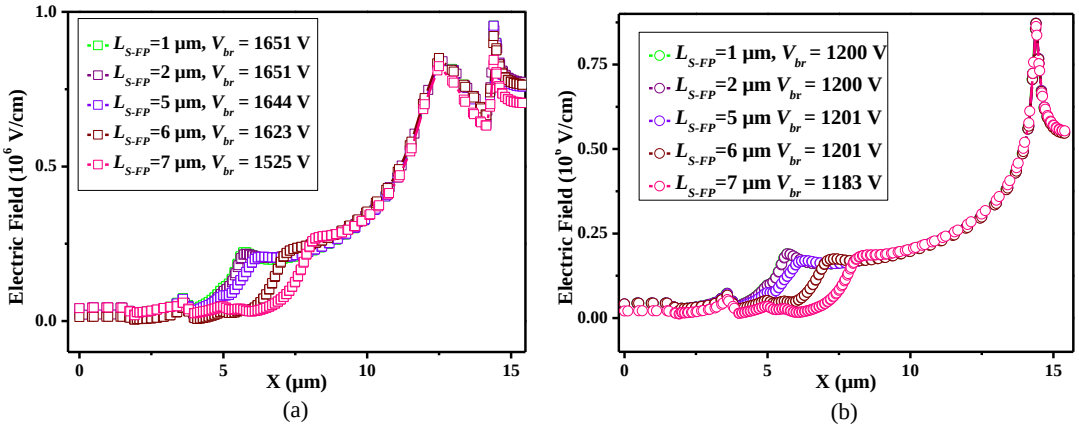


Fig. 6.12. Distribution of the electric field along the AlGaN/GaN heterojunction interface for varying Source-FP lengths: (a) Case I and (b) Case III.

Table 6.4. Electrical performance comparison of AlGaN/GaN HEMT structures with varying $L_{S\text{-}FP}$

Parameters \ $L_{S\text{-}FP}$ (µm)	**1**	**2**	**5**	**6**	**7**
g_m (S/mm)					
Case I	0.417	0.417	0.417	0.418	0.419
Case III	0.417	0.417	0.417	0.418	0.419
C_{gs} (pF/mm)					
Case I	4.98	6.26	13.49	13.68	13.90
Case III	5.00	6.31	13.50	13.69	13.91
C_{gd} (pF/mm)					
Case I	0.68	0.67	0.54	0.55	0.56

Case III	0.68	0.68	0.54	0.55	0.56
f_T (GHz)					
Case I	11.72	9.58	4.73	4.67	4.60
Case III	11.70	9.51	4.73	4.67	4.60
R_{on} (Ω.mm)					
Case I	2.394	2.393	2.392	2.389	2.385
Case III	2.393	2.393	2.392	2.389	2.3857

Table 6.4 presents a comparison of C, f_T, g_m and R_{on} between Case I and Case III structures with varying L_{S_FP}. In both cases, the capacitance rises as L_{S_FP} increases. For Case I, C increases from 5.66 pF/mm at L_{S_FP} = 1 µm to 14.46 pF/mm at L_{S_FP} = 7 µm, while in Case III, it increases from 5.68 pF/mm to 14.47 pF/mm over the same L_{S_FP} range. The f_T drops from 11.72 GHz at L_{S_FP} = 1 µm to 4.60 GHz in Case I, and from 11.70 to 4.60 GHz for Case III. Meanwhile, the g_m improves with longer L_{S_FP}, whereas the R_{on} decreases. The peak g_m for both Case I and Case III is 0.419 S/mm at L_{S_FP} = 7 µm, while the highest R_{on} (2.39 Ω·mm) occurs at L_{S_FP} = 1 µm for both structures.

6.5.3 Impact of Drain Field Plate Length Variation

The study analyses and compares Case I and II configurations by adjusting the drain field FP length (L_{D_FP}) between 0.9 µm and 4.9 µm. Fig. 6.13 illustrates that as L_{D_FP} increases, the electric field at the gate edge intensifies. This occurs because the effective distance between the gate and drain shrinks, leading to a higher overall electric field in the channel. Consequently, the V_{br} decreases. In Case I (Fig. 6.13(a)), V_{br} peaks at 1700 V (L_{D_FP} = 0.9 µm) but drops to 1165 V at 4.9 µm. Similarly, in Case II (Fig. 6.13(b)), V_{br} reaches 1690 V at 0.9 µm but falls to 1440 V at 4.9 µm. When S-FP and D-FP are too close, the electric field near D-FP increases sharply, causing early breakdown at lower voltages.

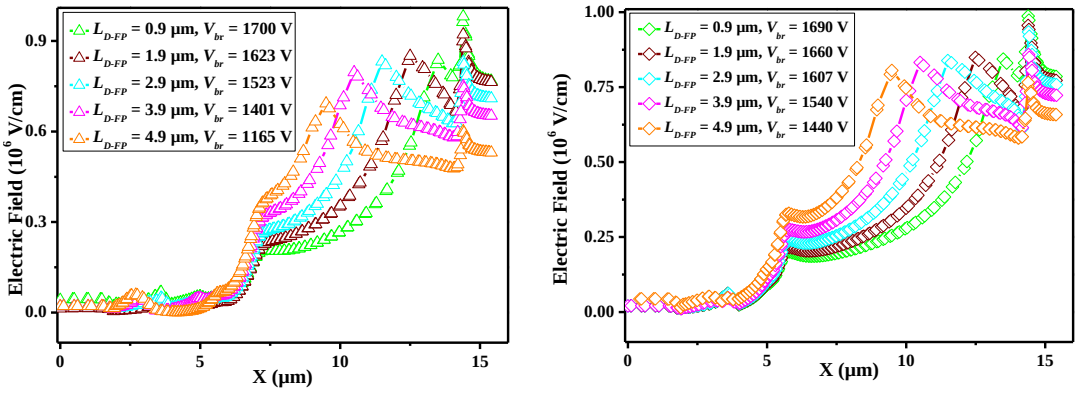


Fig. 6.13. The electric field distribution along the AlGaN/GaN heterojunction interface for varying Drain-FP lengths: (a) Case I and (b) Case II.

Table 6.5. Electrical performance comparison of AlGaN/GaN HEMT structures with varying $L_{D\text{-}FP}$

Parameters / $L_{D\text{-}FP}$ (µm)	**0.9**	**1.9**	**2.9**	**3.9**	**4.9**
g_m (S/mm)					
Case I	0.418	0.418	0.418	0.418	0.418
Case II	0.418	0.418	0.418	0.418	0.418
C_{gs} (pF/mm)					
Case I	13.69	13.68	13.67	13.66	13.65
Case II	4.70	4.69	4.69	4.67	4.66
C_{gd} (pF/mm)					
Case I	0.55	0.55	0.55	0.54	0.54
Case II	0.68	0.68	0.67	0.67	0.67
f_T (GHz)					
Case I	4.67	4.67	4.68	4.68	4.68
Case II	12.36	12.37	12.40	12.43	12.46
R_{on} (Ω.mm)					
Case I	2.389	2.389	2.389	2.390	2.390
Case II	2.390	2.390	2.390	2.390	2.390

Table 6.5 presents a comparison of C, f_T, g_m and R_{on} between Case I and Case II structures as the L_{D_FP} varies. For Case I, C shows a minor reduction from

14.24 pF/mm (L_{D_FP} = 0.9 µm) to 14.19 pF/mm (L_{D_FP} = 4.9 µm), leading to a slight rise in f_T from 4.67 GHz to 4.68 GHz. Similarly, Case II shows a small C reduction (5.38 to 5.33 pF/mm) over the same L_{D_FP} range, raising f_T from 12.36 to 12.46 GHz. As illustrated in Table 6.5, g_m stays approximately constant at 0.418 S/mm for both cases, regardless of L_{D_FP}. Meanwhile, R_{on} for Case I shows a marginal increase from 2.38 Ω·mm to 2.39 Ω·mm as L_{D_FP} varies from 0.9 µm to 4.9 µm. In contrast, R_{on} for Case II remains steady at 2.39 Ω·mm across all L_{D_FP} values.

6.5.4 Impact of Gate Field Plate Length Variation

This section examines the impact of gate-FP length ($L_{G\text{-}FP}$) variation on the characteristics of all four structures. Key parameters such as the channel's electric field profile, g_m, C, f_T, R_{on} and V_{br} are analysed and compared. The $L_{G\text{-}FP}$ is varied from 0.9 to 2.3 µm. As $L_{G\text{-}FP}$ increases, V_{br} shows a gradual rise, as the FP's modulation effect is not strong enough to lower the electric field peak near the gate edge. For Case I (Fig. 6.14(a)), the V_{br} starts at 1621 V for an $L_{G\text{-}FP}$ of 0.9 µm, increases slightly to 1623 V at 1.6 µm, and then drops to 1600 V at 2.3 µm. Due to the closer proximity between the gate-FP edge and the D-FP, the electric field at the FP gate edge attains breakdown levels earlier. In Case II (Fig. 6.14(b)), the highest V_{br} (1666 V) occurs at $L_{G\text{-}FP}$ = 0.9 µm but declines as $L_{G\text{-}FP}$ increases, reaching 1624 V at 2.3 µm. For Cases III and IV (Fig. 6.14(c)-(d)), V_{br} at $L_{G\text{-}FP}$ = 0.9 µm is 1200 V and 1187 V, respectively, while at 2.3 µm, they are 1181 V and 1185 V, respectively.

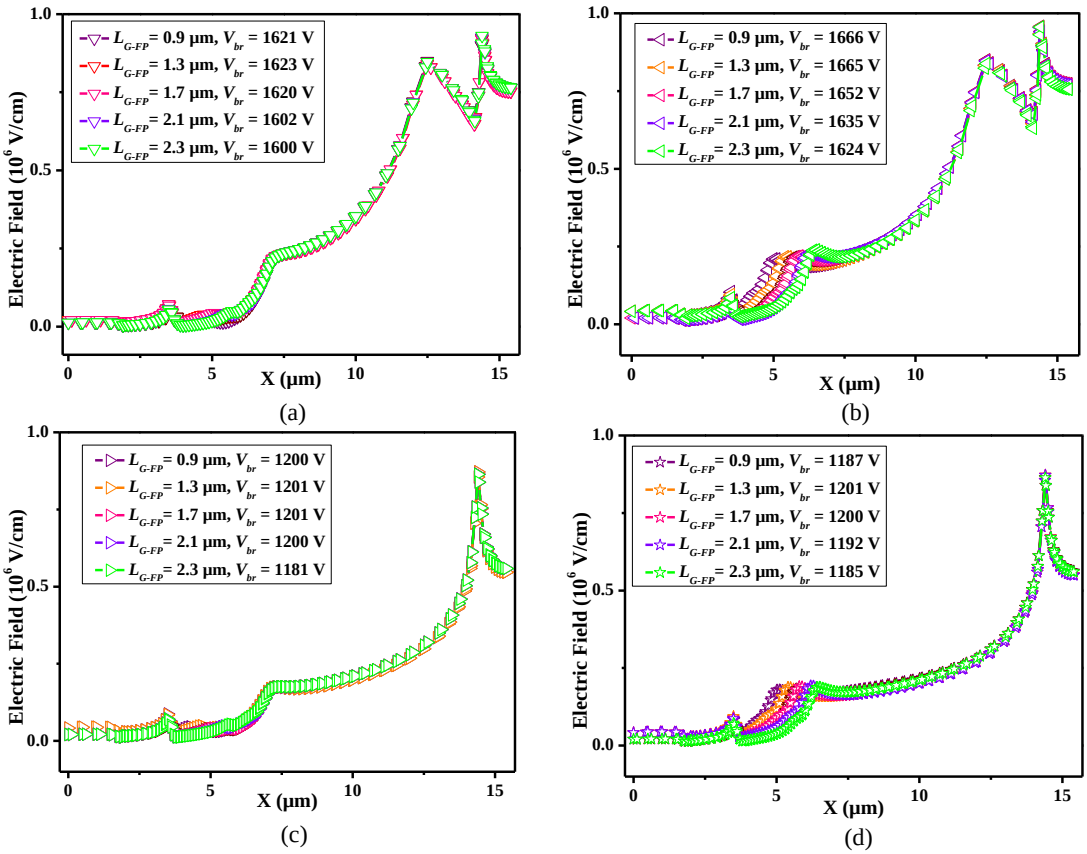


Fig. 6.14. Electric field variations at the AlGaN/GaN heterojunction interface for different gate-FP lengths: (a) Case I, (b) Case II, (c) Case III, (d) Case IV.

The $L_{G\text{-}FP}$ is adjusted to analyse and compare the C, f_T, g_m and R_{on} (Table 6.6). An increase in $L_{G\text{-}FP}$ leads to a larger gate-FP coverage, resulting in a higher overall capacitance, as evident in Table 6.6. Cases I and III exhibit greater C compared to Cases II and IV. At $L_{G\text{-}FP}$ = 2.3 μm, the simulated C values are 15.63 pF/mm and 15.64 pF/mm for Cases I and III, respectively, whereas Cases II and IV reach 5.98 pF/mm and 5.99 pF/mm at the same $L_{G\text{-}FP}$. Since f_T is inversely proportional to capacitance, it decreases as C rises. The peak f_T occurs at $L_{G\text{-}FP}$ = 0.9 μm, with values of 4.95 GHz (Case I), 13.52 GHz (Case II), 4.95 GHz (Case III), and 13.49 GHz (Case IV). Meanwhile, g_m improves with increasing $L_{G\text{-}FP}$, reaching maxima of 0.397 S/mm (Cases I and III) and 0.398 S/mm (Cases II and IV) at $L_{G\text{-}FP}$ = 2.3 μm. Conversely, R_{on} reduces with larger L_{SD}, yielding values of 2.52 Ω·mm (Cases I and III) and 2.51 Ω·mm (Cases II and IV).

Table 6.6. Electrical performance comparison of AlGaN/GaN HEMT structures with varying $L_{G\text{-}FP}$

Parameters \ $L_{G\text{-}FP}$ **(µm)**	**0.9**	**1.3**	**1.7**	**2.1**	**2.3**
g_m (S/mm)					
Case I	0.392	0.393	0.394	0.396	0.397
Case II	0.393	0.394	0.395	0.397	0.398
Case III	0.392	0.393	0.394	0.396	0.397
Case IV	0.393	0.394	0.395	0.397	0.398
C_{gs} (pF/mm)					
Case I	12.10	12.94	13.78	14.63	15.07
Case II	3.97	4.31	4.68	5.08	5.29
Case III	12.11	12.95	13.78	14.64	15.08
Case IV	3.98	4.32	4.69	5.08	5.30
C_{gd} (pF/mm)					
Case I	0.51	0.54	0.55	0.56	0.56
Case II	0.64	0.67	0.68	0.69	0.69
Case III	0.51	0.54	0.56	0.56	0.56
Case IV	0.65	0.67	0.68	0.69	0.69
f_T (GHz)					
Case I	4.95	4.64	4.38	4.15	4.04
Case II	13.52	12.56	11.71	10.94	10.58
Case III	4.95	4.64	4.38	4.14	4.04
Case IV	13.49	12.54	11.69	10.92	10.56
R_{on} (Ω.mm)					
Case I	2.545	2.539	2.531	2.521	2.515
Case II	2.541	2.536	2.528	2.518	2.512
Case III	2.545	2.539	2.531	2.521	2.515
Case IV	2.541	2.536	2.528	2.518	2.512

A comparison between the proposed work and existing studies is presented in Table 6.7, with results at L_{GD} = 11 µm chosen for evaluation. The table summarizes various FP configuration structures along with their performance metrics as documented in prior research. Reported device dimensions include an

L_G (gate length) range of 0.5 µm to 3 µm and an L_{GD} range of 2 µm to 24 µm. According to studies [148], [264]-[265], a traditional single gate-FP structure achieves V_{br} of 160 V, 500 V, and 740 V. Meanwhile, a single 3D-FP (three-dimensional FP) design at the gate yields a drain current of 360 mA/mm, an R_{on} of 17.3 Ω·mm, and a V_{br} of 700 V [147]. Research on a micro-FP [150] demonstrates a V_{br} of 1278 V, along with a drain current of 744 mA/mm and R_{on} of 5.24 Ω·mm. A dual-FP design (with-FPs at gate and source) improves performance, reaching 1118 V V_{br}, 494 mA/mm drain current, and 9.2 Ω·mm R_{on} [266]. Other dual-FP designs show V_{br} values of 250 V [144], 327 V [220] and 680 V [267]. Multi-finger FP [146] and multiple-FP [268] structures also achieve V_{br} values of 130 V and 900 V, respectively.

Table 6.7. Comparison of the proposed device's V_{br} with reported literature values

Variations in FP Configurations	L_{GD} **(µm)**	L_G **(µm)**	R_{on} **(Ω mm)**	I_{dmax} **(mA/mm)**	V_{br} **(V)**	**References**
Gate-FP	1.5	0.3	--	--	500	Ref. [148]
Gate-FP	10	3	9.5-10.7	500	700-740	Ref. [265]
Gate-FP	4.5	1	--	610	160	Ref. [264]
Microfield Plate	9.3	1-2.4	5.24	744	1278	Ref. [150]
3-Dimensional FP	10	3	17.3	360	700	Ref. [147]
Dual-FP (Gate and Source)	15	1	13.3	367	680	Ref. [267]
Dual-FP (Gate and Source)	12	1.5	≈8.5	≈310	327	Ref. [220]
Dual-FP (Gate and Source)	15	2	9.2	494	1118	Ref. [266]
Dual-FP (Gate and Source)	3.5	0.5	--	1050	250	Ref. [144]
Multi-finger FP	2	0.7	--	--	130	Ref. [146]
Multiple FP	24	1.5	--	700	900	Ref. [268]

Double deck gate-FP with a conventional FP at the source and drain	11	1.4	2.38	740	1623	This work (Case I)
Dual FPs structure (Double deck FP at the gate and a conventional FP at the drain)	11	1.4	2.38	741	1660	This work (Case II)
Dual FPs structure (Double deck FP at the gate and a conventional FP at the Source)	11	1.4	2.38	740	1201	This work (Case III)
Single double deck gate-FPs structure	11	1.4	2.38	741	1200	This work (Case IV)

6.6. Summary

The chapter examines the electrical behavior of Normally-Off Si_3N_4-passivated AlGaN/GaN HEMTs with double-deck gate-FPs and compares their performance with traditional FP-free structures. The results demonstrate that the proposed FP design outperforms the conventional HEMT configuration. Additionally, HfO_2-passivated AlGaN/GaN HEMTs with-FPs exhibit a higher V_{br} compared to materials with lower ε_r. The study further examines the structure with source and drain-FPs in various configurations (Case I to Case IV). Electrical and breakdown characteristics are evaluated, and optimizations are performed for key parameters, including L_{SD}, $L_{S\text{-}FP}$, $L_{D\text{-}FP}$, and $L_{G\text{-}FP}$, to enhance performance. L_{SD} varies from 8.4 µm to 15.4 µm, revealing that V_{br} consistently increases with larger L_{SD} values. The highest V_{br} of 1717 V (at L_{SD} = 15.4 µm) is achieved in a double-deck gate-FP structure with a conventional source (L_{S_FP} = 6 µm) and drain-FPs ($L_{D\text{-}FP}$ = 1.9 µm), while maintaining a low R_{on} of 2.38 Ω·mm. However, increasing V_{br} also raises capacitance, adversely affecting the f_T, which degrades accordingly. A single double-deck gate-FP ($L_{G\text{-}FP}$ = 1.6 µm) configuration and a dual-FP structure—

comprising a double-deck gate-FP and a drain-FP—yield highest f_T values of 13.86 GHz and 13.89 GHz, respectively, at L_{SD} = 8.4 µm, $L_{G\text{-}FP}$ = 1.6 µm, and $L_{D\text{-}FP}$ = 1.9 µm. The study also finds that extending the FP lengths (source, drain, or gate) reduces V_{br} due to intensified electric fields, leading to premature breakdown as the FP edges approach the drain. Optimizing FP lengths and source-drain spacing is crucial for maximizing breakdown voltage. The novel FP structure effectively modulates the potential distribution and generates peaks in the electric field at the FP edges of the gate, source, and drain. Among dual-FP configurations, drain and gate-FPs (Case II) deliver superior performance compared to source-FP designs (Case III). Notably, this structure enhances V_{br} even without a source-FP, demonstrating its effectiveness in high-voltage applications.

CHAPTER 7

Physics-Based Analytical Device Modeling

7.1 Introduction

AlGaN/GaN HEMTs are favourable for high-temperature, high-frequency, high-power, and high-breakdown applications due to the strong polarization fields at the heterointerface of AlGaN and GaN. In comparison to other devices based on compound semiconductors in the group III-V, GaN-based HEMTs readily attain a 2DEG sheet carrier density (n_s) exceeding 10^{13} cm^{-2}. The strong polarization field at the heterointerface bends the conduction band, sharply increasing the carrier concentration, leading to high n_s [192]. Strong polarization fields, both spontaneous and piezoelectric, further improve the functionality of these devices [269]-[270]. Furthermore, increasing the mole fraction of Al in AlGaN material will deepen the quantum well, therefore facilitating the confinement of more electrons in the channel [193]. The Al mole fraction (n), thickness, and doping density of the AlGaN barrier layer (N_D) can regulate the amount of polarization and conduction band discontinuities that determine the density of the sheet carrier at the AlGaN/GaN HEMT interface, which provides designers with the freedom to optimise device performance. Due to the existence of interface roughness and high piezoelectric effects, AlGaN/GaN HEMTs differ greatly from AlGaAs/GaAs or InAlAs/InGaAs HEMTs [271]. To demonstrate that the main source of electron charge in an AlGaN/GaN HEMT is the polarization field, Zhang and Singh [272] investigated the impact of the piezoelectric effect and interface roughness on device properties in addition to proposing a numerical formula based on a self-consistent solution of the Schrodinger and Poisson equations. An analytical model integrating spontaneous and piezoelectric polarisations is presented in this study. Charge concentrations at the heterointerface due to polarization were computed using charge control models [188], [194]. A non-linear model [194] was considered to study the variation of the Fermi level with n_s. In this section, a simple analytical model of current-voltage characteristics of AlGaN/GaN HEMTs has been formulated to study the effect of AlGaN barrier thickness (d_{AlGaN}), Al mole fraction (n), and doping concentration (N_D) on threshold voltage (V_{th}) variation and n_s. The suggested model's results have been validated using simulated data and demonstrate good agreement.

7.2 Analytical Model Formulation

A cross-sectional view of the AlGaN/GaN HEMT structure used for modeling is shown in Fig. 7.1. In general, the HEMT structure consists of two layers in which the material with a wider bandgap is doped and the material with a narrower bandgap energy is normally undoped. The principle of HEMT operation involves the transfer of electrons from ionized donors into a narrow bandgap energy material to form a conducting layer. The transfer of electrons occurs because of the critical difference in electron affinity values of the two materials. The potential well formed at the hetero-junction interface is narrow enough to accommodate the accumulated electrons. The high value of 2DEG sheet density obtained in a HEMT device cannot be attributed only to the bandgap discontinuity, but is dominantly determined by the polarization electric fields at the hetero-interface. The spontaneous and piezoelectric coefficients of the GaN material are generally quite high, which is an added advantage. The total polarization charge density ($\sigma(n)$) as a function of n at the hetero-junction interface is given by [63], [64].

$$|\sigma(n)| = \left|P_{SP}(AlGaN) - P_{SP}(GaN) - P_{PZ}(AlGaN)\right| \tag{7.1}$$

Where P_{PZ} is the piezoelectric polarization, and P_{SP} is the spontaneous polarization of AlGaN and GaN [273]-[274].

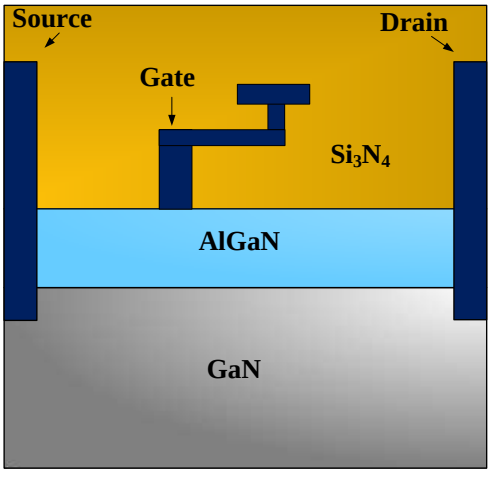


Fig. 7.1. AlGaN/GaN HEMT basic structure.

The piezoelectric polarization in GaN is zero because it is entirely relaxed. As a result, the overall polarization component of GaN incorporates spontaneous polarization. σ is

computed at the AlGaN and GaN interface based on the Al-content *n* of the AlGaN barrier using the following set of linear interpolations between the physical parameters of GaN and AlN [65], [275]. The strain-induced piezoelectric polarization of AlGaN along the [001] direction can be specified by [201]

$$P_{PZ}(AlGaN) = 2\left(\frac{a(0)-a(n)}{a(n)}\right)\left(e_{31}(n) - e_{33}(n)\frac{c_{13}(n)}{c_{33}(n)}\right) \tag{7.2}$$

Where $e_{31}(n)$ and $e_{33}(n)$ are the piezoelectric constants, $a(n)$ is the lattice constant, $c_{13}(n)$ and $c_{33}(n)$ are the elastic constants. Eq. (7.1) now becomes

$$|\sigma(n)| = \left|2\left(\frac{a(0)-a(n)}{a(n)}\right)\left(e_{31}(n) - e_{33}(n)\frac{c_{13}(n)}{c_{33}(n)}\right) + P_{SP}(AlGaN) - P_{SP}(GaN)\right| \tag{7.3}$$

Piezoelectric constants are given by [192]:

$$e_{31}(n) = (-0.11n-0.49)\ \text{cm}^{-2}, \tag{7.4}$$

$$e_{33}(n) = (-0.73n-0.73)\ \text{cm}^{-2}, \tag{7.5}$$

Lattice constant is given by:

$$a(n) = (-0.077n+1.389)10^{-10}\ \text{m}, \tag{7.6}$$

Elastic constants are given by:

$$c_{13}(n) = (5n+103)\ \text{GPa}, \tag{7.7}$$

$$c_{33}(n) = (-32n+405)\ \text{GPa}, \tag{7.8}$$

$P_{SP}(AlGaN)$ and $P_{SP}(GaN)$ can be expressed as [64], [192]

$$P_{SP}(AlGaN) = -0.052n-0.029 \tag{7.9}$$

$$P_{SP}(GaN) = -0.029 \tag{7.10}$$

7.2.1 Modeling of Sheet Carrier Concentration (n_s)

In the low longitudinal-field region with the applied gate-to-source bias (V_G), the sheet carrier density n_s in the channel can be obtained by the self-consistent solution of the 1-D Poisson's and Schrödinger equations [193], [194].

$$n_s = \frac{\varepsilon_{AlGaN}}{qd_{AlGaN}}[V_G - V_{th} - E_F] \tag{7.11}$$

Where, ε_{AlGaN} is the permittivity of the AlGaN layer, q is the electronic charge, d_{AlGaN} is the AlGaN layer thickness, E_F is the Fermi level relative to the conduction band edge of the GaN layer, V_G is the gate-source voltage, and V_{th} is the threshold voltage. E_F can be described as a linear function of n_s, yet there seems to be an inconsistency between the experimental and linear model results [193]. As a result, a non-linear model of HEMT is constructed. For varying the Fermi level with n_s, an empirical formula is required. It should be written in such a way that a straightforward yet valid analytical model for HEMT is provided. Although using an exponential function for non-linear modeling of HEMT provides a better approximation, it complicates the process of finding an analytical solution for n_s. As a result, it is appropriately given by a polynomial function of n_s, and it is challenging to derive an analytical model for current-voltage relations from polynomials of order greater than two. The Fermi level in Eq.(7.11) can be described by a second-order formula [189], [191], [194], which fits the numerical solution of Eq.(7.11) well.

$$E_F(n_s) = k_1 + k_2 n_s^{1/2} + k_3 n_s \tag{7.12}$$

Where, k_1, k_2 and k_3 are dependent on E_F and n_s. Where, k_1 = -0.0802 eV, k_2 = 1.039 x 10^{-9} eV. m and k_3 = 1.0454 x 10^{-18} eV. m^2. Using Eq. (7.12) in Eq. (7.11), n_s is obtained as,

$$n_s = \left[-P + \sqrt{P^2 + Q - R}\right]^2 \tag{7.13}$$

Where,

$$P = \frac{\varepsilon_{AlGaN} k_2}{2Z} \tag{7.13a}$$

$$Q = \frac{V_G \varepsilon_{AlGaN}}{Z} \tag{7.13b}$$

$$R = \frac{\varepsilon_{AlGaN}\left(k_1 + V_{th}\right)}{Z} \tag{7.13c}$$

$$Z = \left(\varepsilon_{AlGaN} k_3 + q d_{AlGaN}\right) \tag{7.13d}$$

Polarization charge density determines the V_{th} of AlGaN/GaN HEMT, given by [201]

$$V_{th} = \phi_b(n) - \Delta E_C(n) - \frac{q N_D d^2{}_{AlGaN}}{2\varepsilon_{AlGaN}(n)} - \frac{d_{AlGaN}\sigma(n)}{\varepsilon_{AlGaN}(n)} \tag{7.14}$$

Where, σ denotes the overall net polarization charge, ΔE_C denotes the conduction band discontinuity, ϕ_b denotes the metal–semiconductor Schottky barrier height, and N_D represents the AlGaN layer doping concentration.

7.2.2 Current-Voltage Characteristics

The drain drift current equation [12] can be used to get the drain current (I_D),

$$I_D(x) = W q v_d(x)\left(n_s(x)\right) \tag{7.15}$$

Where, n_s represents the sheet carrier density, W is the width of the gate, $V_C(x)$ refers to the channel potential, and $v_d(x)$ indicates the electron drift velocity [188].

Where the electron drift velocity is given as,

$$v_d(x) = \frac{\mu_0\left(dV_C(x)/dx\right)}{\left\{1 + \left(1/E_C\right)\left(dV_C(x)/dx\right)\right\}} \tag{7.16}$$

Where, E_C corresponds to the critical field, and μ_0 represents the low field mobility.

The sheet charge density is given as,

$$n_s = \frac{\varepsilon_{AlGaN}}{q d_{AlGaN}}\left[V_G - V_{th} - V_C(x)\right] \tag{7.17}$$

Using Eq. (7.16) and Eq. (7.17) in Eq. (7.15), one obtains,

$$I_D(x)\left(1 + \frac{1}{E_C}\frac{dV_C(x)}{dx}\right) = W\frac{\varepsilon_{AlGaN}\mu_0}{(d_{AlGaN})}\left(V_G - V_{th} - V_C(x)\right)\frac{dV_C(x)}{dx} \tag{7.18}$$

The boundary conditions for Eq. (7.18) are provided by the inherent voltages at the channel's ends immediately below the gate. Here, parasitic drain (R_d) and source (R_s) resistances have been considered, resulting in the following boundary conditions:

$$V_C(x)|_{x=0} = I_D R_s \tag{7.19}$$

$$V_C(x)|_{x=L} = V_D - I_D R_d \tag{7.20}$$

Eq. (7.18) is integrated with the boundary conditions to yield the linear region I_D equation as,

$$I_D(x) = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \tag{7.21}$$

Where,

$$A = R_{Tot} - \frac{\alpha E_C}{2}\left(R_d{}^2 - R_s{}^2\right) \tag{7.21a}$$

$$B = \alpha E_C \left(R_d V_D - R_{Tot} V'_G\right) - V_D - E_C L_G \tag{7.21b}$$

$$C = \alpha E_C \left(V_D V'_G - \frac{V_D{}^2}{2}\right) \tag{7.21c}$$

Where,

$$V'_G = V_G - V_{th} \tag{7.21d}$$

$$R_{Tot} = R_s + R_d \tag{7.21e}$$

and

$$\alpha = \frac{W \mu_0 \varepsilon_{AlGaN}(n)}{d_{AlGaN}} \tag{7.21f}$$

Where the gate length is L_G and the applied drain voltage is V_D. The I_D reaches its saturation as V_D increases. I_{dss} represents the drain saturation current, represented by,

$$I_{dss} = \frac{W V_{sat} \varepsilon_{AlGaN}(n)}{d_{AlGaN}}\left(V'_G - V_{DSAT}\right) \tag{7.22}$$

The drain saturation voltage (V_{DSAT}) is calculated by equating I_{dss} in Eq. (7.22) with Eq. (7.21) and inserting $V_{D} = V_{DSAT}$ in Eq. (7.21). As a result, V_{DSAT} is given as

$$V_{DSAT} = \frac{-T \pm \sqrt{T^2 - 4SU}}{2S} \tag{7.23}$$

Where,

$$S = \frac{1}{2} + \alpha R_s E_C - \frac{E_C{}^2 \alpha^2}{2}\left(R_d{}^2 - R_s{}^2\right) \tag{7.23a}$$

$$T = LE_C - \alpha E_C R_s V'_G + (\alpha E_C)^2\left(R_d{}^2 - R_s{}^2\right) \tag{7.23b}$$

$$U = \frac{\left(\alpha E_C V'_G\right)^2}{2}\left(R_s{}^2 - R_d{}^2\right) - E_C L V'_G \tag{7.23c}$$

7.3 Results and Discussions

An analytical model of AlGaN/GaN HEMT for a 0.5 µm gate length is constructed. Along with this, a non-linear Fermi level model is used to study the variation of E_F with n_s. MATLAB [276] and the 2D Silvaco TCAD software [210] are employed to simulate the formulated equations. To demonstrate the model's validity, the equations derived above are plotted and compared to the simulated results**.** The GaN HEMT device structure provided in Fig. 7.1 is used for TCAD simulations and analytical calculations. The suggested structure features a 30 nm wide GaN channel and a 20 nm thick n-doped AlGaN barrier layer. A 600 nm thick Si_3N_4 passivation layer was applied over the barrier layer. The distance between the gate and the drain (L_{GD}) is 3.2 µm, while the distance between the source and the gate (L_{SG}) is 0.5 µm, respectively. The work function of the Schottky gate contact is 4.91 eV. To achieve maximal sheet concentration of 2DEG at the interface, the polarisation fields can be completely exploited by adjusting the *n*, d_{AlGaN}, and N_D. Fig. 7.2(a) and 2(b) show the comparison of transfer (I_D-V_G) and output (I_D-V_D) characteristics of AlGaN/GaN HEMT obtained from analytical and TCAD numerical simulation results. Poisson's and continuity equations for electrons and holes are solved self-consistently in 2D TCAD numerical simulations [273]. The polarization charges computed using equations already described are included at the AlGaN/GaN and AlGaN/nitride interfaces. A good agreement between the TCAD physical simulation and analytical model confirms the validity of the proposed intrinsic drain current model. To obtain the I_D-V_G characteristics depicted in Fig. 7.2(a), the drain current (I_D) is calculated using Eq. (7.21) and plotted against the V_G while keeping the

V_D constant at 0.1 V. The results show that I_D rises with increasing V_G. For the proposed HEMT structure in Fig. 7.1, the V_{th} is found to be -5.2 V. Similarly, Fig. 7.2(b) presents the I_D-V_D characteristics at a fixed V_G of -3 V, where I_D is plotted against V_D. The data indicate that I_D increases as V_D increases, reaching a peak value of 1.04 A/mm at V_G = -3 V. These calculations were conducted with an Al mole fraction (n) of 0.25, a barrier thickness of 20 nm, and a doping density of 2×10^{18} cm^{-3}. A good agreement is observed between the model and the simulated structure.

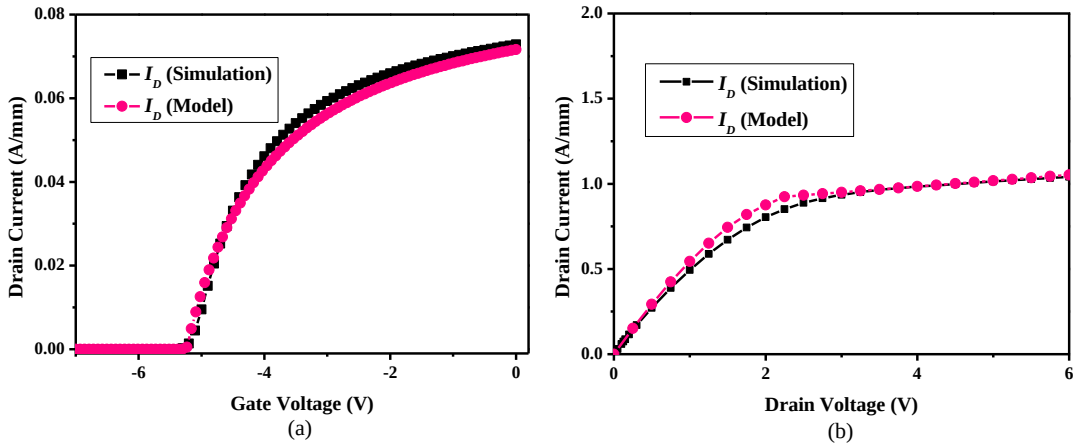


Fig. 7.2. Comparison of (a) I_D-V_G, and (b) I_D-V_D characteristics.

Table 7.1. List of model parameters (for n = 0.25)

Parameter	Value	Unit
K_B	1.380649×10^{-23}	J/K
ε_0	8.854×10^{-14}	F/cm
ε_{AlGaN}	(-0.5 n+9.5) ε_0	F/cm
ϕ_b	(1.3 n+0.84)	eV
N_D	2×10^{18}	cm^{-3}
V_{sat}	1.4×10^{7}	cm/s
E_C	1.5×10^{5}	V/cm
μ_0	900	$cm^2/(Vs)$

The variation of n_s and V_{th} with AlGaN barrier layer thickness for an n value of 0.25 is shown in Fig. 7.3.

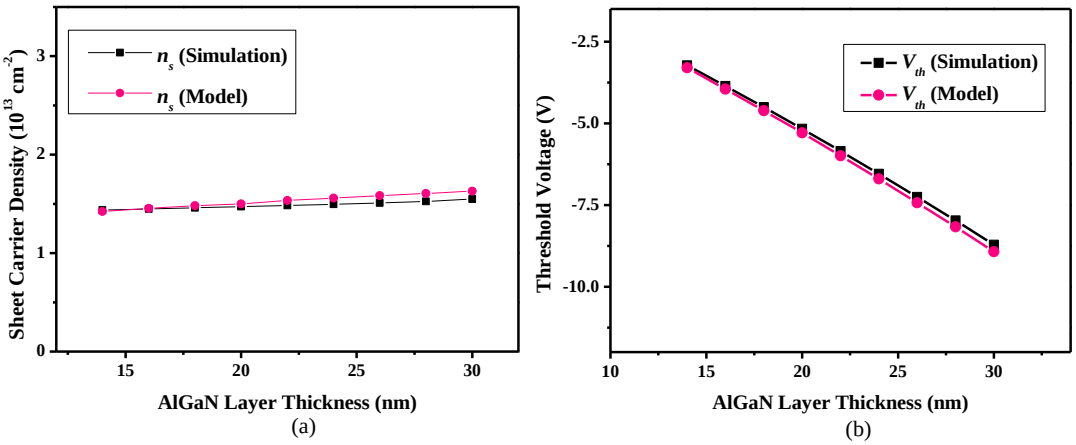


Fig. 7.3. Effects of variation of AlGaN layer thickness on (a) n_s, (b) V_{th}.

As the thickness of the AlGaN layer increases, so does the effective distance between the gate and the 2DEG, resulting in reduced gate control and, as a result, an increase in the V_{th} and n_s. Because there are more electrons available in the quantum well, more negative voltage should be applied to the gate terminal to totally drain the channel or turn the device off. The n_s increases with AlGaN thickness, rising from 1.4×10^{13} cm^{-2} at 14 nm to 1.54×10^{13} cm^{-2} at 30 nm. Meanwhile, the V_{th} negativity increases from -3.2 V to -8.7 V. A larger value of AlGaN layer thickness is preferred to get a high value of 2DEG density. Nevertheless, the maximum thickness of the AlGaN layer is limited by the parasitic MESFET conduction in HEMTs [277].

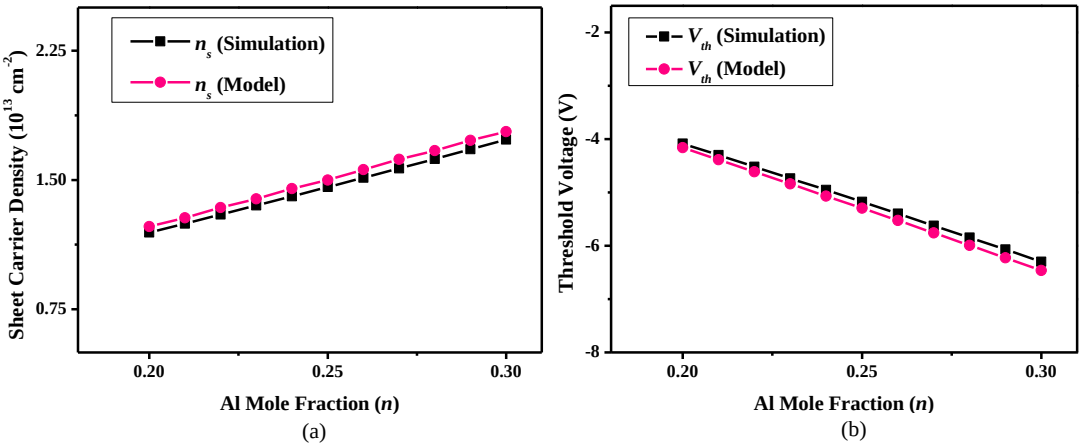


Fig. 7.4. Influence of Al-mole fraction on (a) n_s (b) and V_{th}.

The Al content of the AlGaN layer is also altered to examine its impact on n_s and V_{th}. The piezoelectric and spontaneous polarization of AlGaN increases as the barrier Al content increases, increasing the interface electrons. The study is performed for the case where the barrier is strained, i.e., the mole fraction of the barrier layer is less than 0.38. The Al-

concentration changes from n = 0.20 to 0.30, where the n_s increases due to the differing total polarizations of AlGaN and GaN (Fig. 7.4(a)). The density of the sheet carrier rises with increasing Al concentration, from 1.1×10^{13} cm^{-2} at n = 0.20 to 1.7×10^{13} cm^{-2} at n = 0.30. Meanwhile, the V_{th} negativity increases from -4.0 V to -6.2 V at n = 0.20 and 0.30, respectively. Higher Al concentration values result in a bigger bandgap, greater conduction band discontinuities, and stronger polarisation effects, which result in improved carrier confinement and higher 2-DEG density values.

Fig. 7.5(a) depicts the variation of 2-DEG n_s with different AlGaN barrier layer doping densities. As the AlGaN layer doping density rises, n_s increases because the 2-DEG can accommodate more free electrons. Fig. 7.5(b) depicts how the AlGaN layer's doping concentration is affected by the polarization-dependent V_{th}. The V_{th} falls and n_s rose as the doping density increases. n_s rose from 1.4×10^{13} cm^{-2} to 1.8×10^{13} cm^{-2} and V_{th} falls from -4.8 V to -6.5 V with the change in N_D from 1×10^{18} cm^{-3} to 6×10^{18} cm^{-3}. As shown in Eq. (7.14), the V_{th} in AlGaN/GaN HEMTs is dominated by the polarization-induced charge density rather than by the doping density.

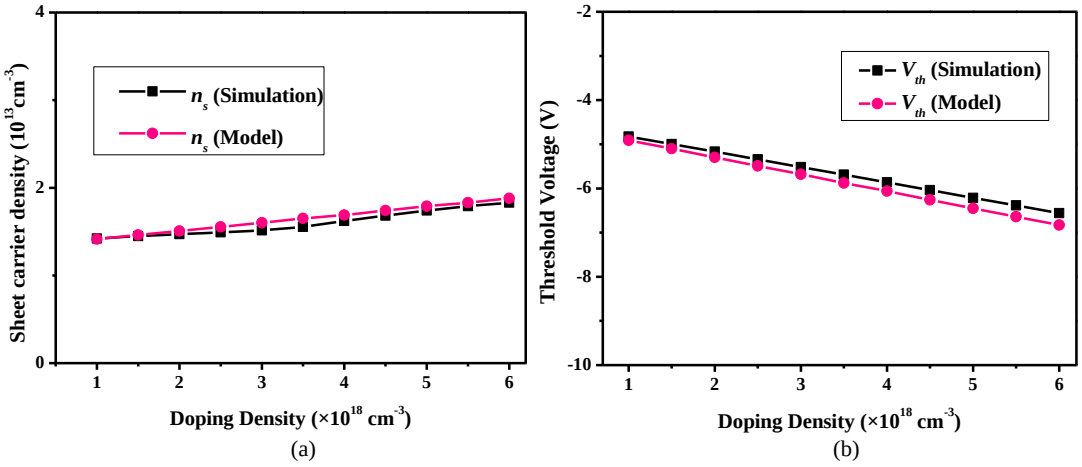


Fig. 7.5. Dependence of (a) n_s, and (b) V_{th} for various values of AlGaN layer doping density.

7.4 Summary

The most essential parameter in characterising and evaluating the performance of AlGaN/GaN HEMT is the 2DEG sheet charge density, for which an analytical model is developed. For varying sheet electron concentration in a quantum well, a non-linear model for the Fermi level is used. In predicting the 2-DEG density and V_{th} with variable mole percentage, barrier thickness, and doping density, the effects of piezoelectric and spontaneous polarization have been appropriately taken into consideration. The n_s increased

with AlGaN thickness, from 1.4×10^{13} cm^{-2} at 20 nm to 1.54×10^{13} cm^{-2} at 30 nm, while the V_{th} decreased from -3.2 V to -8.7 V. This is because the effective distance between the gate and the 2DEG increases as the AlGaN layer becomes thicker, resulting in less gate control and, as a result, lower V_{th} and higher n_s. The density of the sheet carrier increases with increasing Al concentration, from 1.1×10^{13} cm^{-2} at n = 0.20 to 1.7×10^{13} cm^{-2} at n = 0.30. Meanwhile, the V_{th}'s negativity increases from -4.0 V to -6.2 V at n = 0.20 to 0.30, respectively. Higher n values result in a larger bandgap, greater conduction band discontinuities, and stronger polarisation effects, which result in raising the 2-DEG density values and enhance carrier confinement. n_s increased with increasing AlGaN layer doping density (1×10^{18} cm^{-3} to 6×10^{18} cm^{-3}), from 1.4×10^{13} cm^{-2} to 1.8×10^{13} cm^{-2} and V_{th} falls from -4.8 V to -6.5 V. This is because more free electrons are available to fill the 2-DEG, causing the density of the 2-DEG to increase as the doping density of the AlGaN layer does. Additionally, current voltage characteristics are also calculated and compared to the simulated data, demonstrating a high level of agreement.

CHAPTER 8

Conclusion and Future Work

8.1 Conclusion

This dissertation presents an in-depth investigation into the design, and optimization of AlGaN/GaN and related HEMT structures, emphasizing performance improvement through field-plate (FP) design, passivation techniques, and barrier layer engineering. The simulation-based analysis offered significant understanding of how structural parameters, material configurations, and electrical performance metrics are interconnected—key factors in enhancing GaN HEMT technology for high-power and high-frequency applications. The investigation of FP configurations revealed the vital role of FP geometry and positioning in determining the device's breakdown characteristics. Gate-connected FPs were found to be the most efficient in reducing electric-field crowding, which in turn improved the breakdown voltage (V_{br}). More advanced configurations, such as the double-deck gate-FP, exhibited significant enhancements in V_{br}; however, they also introduced larger parasitic capacitances, highlighting the inherent trade-off between voltage handling capability and high-frequency performance. The optimization of FP length and placement showed that extending the FP beyond the high-field region yields minimal improvement, offering useful insights for designing efficient FP structures.

The investigation of passivation methods showed that the selection and configuration of dielectric layers play a crucial role in determining the trade-off between V_{br} improvement and RF performance. High-*k* HfO_2 layers enhanced the V_{br} by smoothing out the electric-field distribution, while SiO_2 and Si_3N_4 passivations provided better high-frequency characteristics owing to their lower capacitance. The dual-layer passivation schemes—specifically Type-A (HfO_2/Si_3N_4) and Type-B (Si_3N_4/HfO_2)—exhibited notable improvements in performance compared to single-layer designs. Overall, the V_{br} analysis confirms that both dual-layer passivation schemes offer higher V_{br} values for Type-A (~798 V) and Type-B (~797 V) substantially exceeding those of single-layer structures. Type-A provided the highest V_{br}, whereas Type-B offered superior overall RF characteristics, highlighting the importance of optimizing interface quality and layer thickness to attain balanced device performance.

Barrier layer engineering using InAlN, InAlGaN, and their hybrid combinations further expanded the performance envelope of GaN HEMTs. The results confirmed that

compositional and thickness tuning of barrier alloys significantly affects drain current, transconductance, and breakdown strength. The introduction of asymmetric and symmetric dual- and triple-material barriers effectively combined the advantages of conventional AlGaN, InAlN, and InAlGaN structures, leading to improved drain current density, enhanced V_{br}, and reduced gate leakage. Comparative analysis of traditional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMTs with dual-material configurations shows that the 17 nm symmetric Case II (InAlGaN + AlGaN) structure achieves a V_{br} of 723 V and an I_{dss} of 0.972 A/mm, surpassing the AlGaN/GaN HEMT in both metrics, while maintaining a lower I_{dss} than the InAlN/GaN and InAlGaN/GaN devices. Further evaluation indicates that Case III (AlGaN + InAlN) in the same configuration provides optimized results, achieving a V_{br} of 404 V and I_{dss} of 2.34 A/mm. Notably, the triple-material symmetric structure (InAlGaN+InAlN+AlGaN) exhibited superior trade-offs suitable for ultra-high-power operations. Specifically, Case F (InAlGaN+InAlN+AlGaN) with a 17 nm symmetric HEMT structure delivering the highest I_{dss} of 2.96 A/mm, and a V_{br} of 569 V—values that exceed those of InAlN/GaN and InAlGaN/GaN structures, while slightly trailing the AlGaN/GaN HEMT in breakdown strength.

The double-deck gate-FP configuration proved effective for Normally-Off AlGaN/GaN HEMTs, achieving a high V_{br} of up to 1717 V and maintaining a reasonable f_T of ~12–14 GHz. The results highlight that precise tuning of gate, source, and drain FP lengths, along with source–drain spacing (L_{SD}) can significantly enhance device performance. Hence, optimized combinations of FP geometries and L_{SD} are key to realizing high-voltage, high-frequency Normally-Off HEMTs.

Finally, the analytical modeling of two-dimensional electron gas (2DEG) sheet charge density provided deeper theoretical understanding of carrier behavior at the heterointerface. The nonlinear Fermi-level model accurately captured the dependence of 2DEG density and threshold voltage on barrier thickness, Al composition, and doping concentration, aligning well with simulation observations. The sheet carrier density (n_s) rises with increasing AlGaN thickness—from 1.4×10^{13} cm^{-2} at 20 nm to 1.54×10^{13} cm^{-2} at 30 nm—while the threshold voltage (V_{th}) drops from –3.2 V to –8.7 V due to reduced gate control over the 2DEG. Similarly, higher Al composition (n = 0.20 to 0.30) increases n_s from 1.1×10^{13} to 1.7×10^{13} cm^{-2} and shifts V_{th} from –4.0 V to –6.2 V, attributed to stronger polarization and larger band offsets. Increasing AlGaN doping (1×10^{18} to 6×10^{18} cm^{-3}) further raises n_s from 1.4×10^{13} to 1.8×10^{13} cm^{-2} and lowers V_{th} from –4.8 V to –6.5 V, as

more free electrons populate the 2DEG channel. Thus, this model serves as a predictive tool for tailoring HEMT designs to desired electrical characteristics.

In summary, this research provides a unified framework for the design of high-performance GaN-based HEMTs through the synergistic optimization of FP geometry, passivation engineering, and barrier material selection. The results offer practical design strategies that balance the competing requirements of high V_{br}, low on-resistance, and superior frequency response. The findings contribute significantly to the understanding and advancement of GaN-based power and RF electronics, paving the way for their deployment in next-generation high-efficiency, high-power, and high-frequency systems.

8.2 Future Scope

Although this research has provided significant insights into the optimization of GaN-based HEMTs through FP, passivation, and barrier engineering, several areas remain open for further exploration to advance device performance, reliability, and practical applicability. The proposed double-deck gate field plate (FP) structure presents a scalable approach to enhance the performance of GaN HEMTs in high-voltage applications, addressing key challenges in power electronics. Future research could focus on the fabrication and integration of this double-deck gate-FP with other enhancement-mode techniques, such as gate recess engineering or fluorine plasma treatment, to further improve threshold voltage stability and reduce gate leakage. Such optimizations could lead to significant improvements in device efficiency and reliability. Additionally, the multi-material barrier design, particularly the triple-material Case F (InAlGaN + InAlN + AlGaN), demonstrates strong potential for optimizing GaN HEMT performance by balancing high breakdown voltage and high drain current—critical for ultra-high-power applications. Future studies should explore interface engineering to minimize gate leakage and enhance long-term reliability. Experimental fabrication of this structure would also be valuable to validate its real-world performance and feasibility in practical power electronics systems. By combining these advancements—novel FP architectures with multi-material barriers—future work could lay the foundation for next-generation GaN HEMTs with superior power handling, efficiency, and robustness.

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List of Publications

Journal Publications:

[1] **P. Kharei**, A. Baidya, N. P. Maity, and R. Maity, "An insight to current collapse in GaN HEMT and suppressing techniques," *Engineering Research Express*, vol. 5, no. 1, p. 012001, 2023. [ISSN: 2631-8695] [IF: 2.07 (2024, Clarivate Analytics), ESCI].

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TOPICAL REVIEW

An insight to current collapse in GaN HEMT and suppressing techniques

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Keywords: 2DEG, donor complex defect (DX) centre, passivation, field plate, cap layer, current collapse

Abstract

High Electron Mobility Transistors (HEMT) made of aluminum gallium nitride/gallium nitride (AlGaN/GaN) have become a major focus for all electronic devices based on gallium nitride due to its excellent system characteristics. AlGaN/GaN HEMTs have severe problems that degrade their performance and the drain current collapse (CC) is one of them. During switching operations, the CC increases the on-resistance (R_{ON}) leading to an increase in device loss and temperature. This review features the basics related to the CC in HEMT and its significance in performance degradation. This paper is concerned with the various advancements reported in recent years to suppress CC in GaN HEMT. Various techniques such as passivation, illumination, free-standing GaN substrate, GaN cap layer including high resistivity GaN cap layer, device structure, surface treatment and deposition techniques, buffer design, and field plates (FP) have been introduced by various researchers to combat CC. This review analysis will help researchers to employ suitable techniques in their HEMT design for future development.

1. Introduction

Due to its abundance, simplicity of processing, and 'wealthy information availability' [1], silicon (Si)is always chosen to manufacture power devices. However Si has reached its operational limits and as a result, the study of new materials to build better power semiconductors is necessary. GaN and associated alloys have been utilised to create high-voltage, high-speed, high-power, and high-frequency electronic devices worldwide. It has been acknowledged by researchers all over the world as the preferred large bandgap semiconductor material [2].With high saturation velocity with the presence of two-dimensional electron gas (2DEG) at its heterojunction with AlGaN, a high output current can also be obtained [3]. Also, because of its high thermal conductivity and high power density, it can dissipate heat more efficiently than any other semiconductor. Since 2010 GaN power transistors are in volume manufacturing. Nonetheless, as first mentioned in 1993, AlGaN/GaN HEMT is basically normal-ON [4]. Hence their main applications were concentrated on devices with high frequency and low voltage. In comparison, transistors needed for power-switching applications should be normally OFF. It is not just important for security reasons yet additionally decreases the leakages in current, thereby reducing power loss, simplifying the driving circuit, and improving the device's stability [5]. In 1996 an initial demonstration of the AlGaN/GaN HEMT enhancement mode was made [6]. Several approaches were also made to generate normally-off GaN-based HEMTs [7, 8]. While substantial advancement has been made in high-frequency performance, some issues still need to be solved, including current collapse, increased temperature brought by high thermal resistance, and knowledge of high temperature transport properties. Current collapse is one of these, and it's crucial because it restricts the output power of the microwave. As high voltage switching is one of the main concerns for power electronics applications, on-resistance modification under the influence of CC becomes a matter of concern. Developments are been reported to minimize the electron trapping at defects which is a cause of CC. It was found that the CC increases and leakage current decreases with higher buffer layer's trap density [9]. A compact analysis of the techniques employed by different researchers in recent years is

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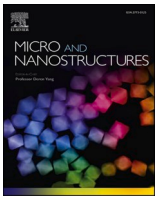

Novel double deck gate field plate structure on a normally-off AlGaN/GaN HEMT- An extensive analysis

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ABSTRACT

A novel double deck gate field plate structure on a normally-off AlGaN/GaN HEMT is proposed and compared with the conventional no field plate structure. Several passivation materials with relative permittivity (ε_r) ranging from 3.9 to 22 is taken into consideration to study the breakdown and DC characteristics. The implementation of field plate along with a higher ε_r material helps in improving breakdown voltage (V_{Br}) as they both decrease the electric field at the gate's drain edge. Aiming device optimization several field plate configurations are studied including tri field plate structure, dual field plate structures and single gate FP structure. Extensive analysis in these structures are done with different lengths of the field plates and distance between source and drain. Distance between source and drain (L_{SD}) is varied from 8.4 to 13.4 μm, source FP lengths (L_{S_FP}) varies from 1 to 7 μm, gate FP lengths (L_{G_FP}) varies from 0.9 to 2.3 μm and drain FP lengths (L_{D_FP}) varies from 0.2 to 4.9 μm. In all scenarios with varying L_{SD}, V_{Br} rises with increasing L_{SD}. For source, gate and drain FP lengths variation, V_{Br} decreases as it gets longer because the electric field becomes very high. As the distance between the FP edge and the drain becomes narrower with increase in FP lengths, the breakdown occurs at lower voltage. At L_{SD} 13.4 μm, this novel double deck gate FP structure with conventional drain field plate structure gives highest V_{Br} of 1660 V and a small R_{on} of 2.39 Ω mm as compared to other structures. It also outperforms the other three structures in F_T (9.84 GHz) at this particular L_{SD}. Analysis of the simulated structures shows that the union of gate-drain field plate boosts the V_{Br} while decreasing the R_{on}, resulting in improved electrical performance and a wider application range.

1. Introduction

The high carrier density and high electron mobility of the two dimensional electron gas (2DEG) makes the high electron mobility transistors (HEMTs) based on gallium nitride (GaN) excellent devices for high power and high frequency applications. HEMTs are innately normally-on devices due to the presence of the 2DEG at the interface of AlGaN/GaN heterostructures. In power electronics, normally-off operation is preferred for simplification of device circuity and safety purposes. Thus, a variety of structures, such as gate recess [1–4], p-GaN gate [5–7], fluorine incorporation [8,9], and so on are implemented to achieve enhancement-mode transistors. The p-GaN gate structure is frequently investigated and used due to its stable operation and good realization of the device's

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Investigation of Multi-Material Barrier GaN-based High Electron Mobility Transistors with Double-Deck Gate Field Plate

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Abstract—This study analyses a gallium nitride (GaN) high electron mobility transistor (HEMT) featuring a double-deck gate field plate (FP) structure to achieve enhanced performance metrics by integrating dual and triple-material barrier configurations. The proposed structure is evaluated using aluminum gallium nitride (AlGaN), indium aluminum nitride (InAlN), and indium aluminum gallium nitride (InAlGaN) as barrier materials in symmetric and asymmetric configurations. The results indicate that AlGaN, when used as a barrier material, offers a higher breakdown voltage (V_{Br}) than InAlN and InAlGaN. Conversely, although InAlN and InAlGaN exhibit lower breakdown voltages, they demonstrate significantly higher drain saturation currents (I_{dss}) than AlGaN. The objective of this research is to develop a structure capable of achieving both high V_{Br} and I_{dss}. To this end, dual and triple-material barrier configurations were evaluated within a single device structure. The analysis of dual-material barrier structures revealed that the symmetric Case III (AlGaN+InAlN) configuration with 17 nm barrier thickness provided the most favourable results, yielding a V_{Br} of 404 V and an I_{dss} of 2.34 A/mm. When comparing traditional AlGaN/GaN, InAlN/GaN, and InAlGaN/GaN HEMT structures to those incorporating triple symmetric barrier materials, it was observed that the symmetric Case F (InAlGaN+InAlN+AlGaN) configuration, with a thickness of 17 nm, achieved the highest I_{dss} value of 2.96 A/mm. This same configuration also produced the highest V_{Br} of 569 V, which, while higher than that of InAlN and InAlGaN, was still lower than that of AlGaN. Overall, the results demonstrate that the triple-barrier structure (Case F, 17 nm) outperforms the dual-material barrier structure (Case III, 17 nm) in terms of both breakdown voltage and drain saturation current.

Keywords: GaN HEMT, dual and triple-material barrier, V_{Br}, I_{dss}, g_m

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1. INTRODUCTION

High-power and high-frequency amplifiers employ GaN-based high electron mobility transistors (HEMTs) due to their superior material properties, including high electron saturation velocity and strong breakdown electric field [1]. Thanks to these characteristics, GaN HEMTs can outperform other semiconductor devices like silicon metal oxide semiconductor field effect transistors (MOSFETs) and gallium arsenide (GaAs) -based heterostructure devices in terms of output power density at high operating frequencies [2]. GaN-based materials are widely used in advanced applications, including light-emitting diodes (LEDs), laser diodes, and terahertz (THz) applications due to their wide bandgap, high thermal stability, and excellent electronic properties [3–8]. However, advancements in GaN HEMT technology have pushed the performance of traditional AlGaN/GaN HEMTs toward the upper limits of their material structure, necessitating further enhancements. One proposed approach to improve high-frequency performance involves increasing the aluminum content in the AlGaN barrier layer. However, this strategy reduces the critical thickness of the fully strained AlGaN barrier due to the increasing lattice mismatch between AlGaN and GaN, leading to local relaxation at the heterointerface through the formation of misfit dislocations and cracks [9]. To address this issue, InAlN and InAlGaN have been proposed as alternative barrier materials to AlGaN. InAlN/GaN [10–16] and InAlGaN/GaN [17–22] heterostructures exhibit stronger spontaneous polarization-induced electric fields compared to AlGaN/GaN, resulting in higher electron concentrations in the two-dimensional electron gas (2DEG). Specifically, InAlN-based heterostructures achieve an electron density in

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Breakdown Voltage Improvement and RF Analysis of T-gate AlGaN/GaN HEMTs with Various High-k Passivation Materials

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Abstract—AlGaN/GaN-based high electron mobility transistor (HEMT) with a T-gate field plate (FP) structure is proposed for high power applications. Analysis of breakdown voltage (V_{br}) characteristics, analog and RF (Radio-frequency) properties of the proposed structure, is carried out to evaluate the device's performance potential. Additionally, the structure is analyzed using various high-k materials in the passivation layer to enhance device performance. As the passivation layer's relative permittivity rises, the V_{br} gets better. However, as the V_{br} rises, the cut-off frequency (f_T) deteriorates. Short Channel Effects (SCEs) such as drain induced barrier lowering (DIBL) and subthreshold swing (SS), along with analog and RF figures of merit (FOMs) such as early voltage (V_{EA}), intrinsic gain (A_V), gain transconductance frequency product (GTFP), transconductance frequency product (TFP), and gain frequency product (GFP), are studied by changing the passivation material. Owing to its elevated transconductance (g_m) and high f_T, SiO_2 passivated T-gate FP AlGaN/GaN HEMT provides improved GFP and TFP performance compared to other high-k materials. The highest V_{br} of 751 V is achieved in La_2O_3 passivated T-gate field plate (FP) AlGaN/GaN HEMTs. Maximum f_T of 38.72 GHz is obtained in the SiO_2 passivated structure. The resulting device has an improved drain current of 1.887 A/mm and g_m of 613 mS/mm. These findings demonstrate the suitability of the T-gate FP AlGaN/GaN HEMT suggested structure for high-power applications.

Keywords: HEMT, field plate, passivation layer, high-k dielectric, breakdown voltage

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1. INTRODUCTION

Gallium nitride (GaN) and its related III-nitride alloys have garnered significant interest owing to their wide bandgap, high thermal stability, and excellent electronic and optical properties. These characteristics make GaN-based materials suitable for a wide spectrum of applications, including light-emitting diodes (LEDs) [1–6], high-efficiency solar cells [7], high-electron-mobility transistors (HEMTs) [8, 9], and terahertz and optoelectronic devices [10]. These diverse applications further emphasize the importance of understanding and optimizing GaN-based heterostructures for next-generation electronic and optoelectronic devices. The high critical electric fields of AlGaN/GaN HEMTs enable them to achieve high V_{br}. In addition, high carrier mobility and high V_{br} in the 2DEG allow high power density operation with minimum power loss in RF and power electronic systems [11, 12]. These features enable HEMTs to operate at frequencies significantly higher than those of conventional wide-bandgap semiconductor devices [13]. Several techniques can be utilised to raise HEMT's V_{br}, including the use of field plates (FPs) [14, 15], Schottky source drain contact technology (SSD) [16], and the insertion of passivation layers between the gate and drain [17]. The insertion of an FP increases the V_{br} by suppressing the electric field concentration around the drain-side of the gate. Despite this, the inclusion of a gate FP also increases parasitic gate capacitance, which negatively impacts high-frequency performance [18]. Although frequency performance is reduced, the use of FP and SSD technology leads to improved V_{br} [19]. Adding a passivation layer primarily serves two purposes: first, it shields the device's top layer from outside influences, and second, it lessens the maximum field intensity near the drain end of the gate region [20]. Ultimately, a smoother drain current (I_D) flow is achieved, leading to an increase in V_{br}. The results indicate that passivated devices attain higher V_{br}

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Non-Linear Analytical Approach to Investigate Barrier Layer Parameter Effect on 2DEG and DC Characteristics in AlGaN/GaN HEMTs

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Abstract—This paper investigates the DC characteristics of a two-dimensional (2D) analytical model of AlGaN/GaN High Electron Mobility Transistor (HEMT), based on the solution of Poisson's equation and incorporating the effects of spontaneous (P_{SP}) and piezoelectric (P_{PZ}) polarization. The behaviour of the sheet carrier density (n_s) is studied using a non-linear model of the Fermi level, and the two-dimensional electron gas (2DEG) current–voltage characteristics incorporate the effects of velocity saturation, field-dependent mobility, and parasitic resistances. Additionally, variations in the threshold voltage (V_{th}) and n_s are examined in relation to barrier thickness (d_{AlGaN}), aluminum mole fraction (n), and the doping density (N_D) of the barrier layer. In predicting the 2DEG density and V_{th} with varying n, d_{AlGaN} and N_D, both P_{SP} and P_{PZ} polarization effects were considered. The n_s increased with d_{AlGaN}, from 1.3×10^{13} cm^{-2} at 20 nm to 1.4×10^{13} cm^{-2} at 34 nm, while V_{th} shifted negatively from −4.7 to −9.4 V due to reduced gate control at higher thickness. For n, n_s rose from 1.0×10^{13} to 1.7×10^{13} cm^{-2} as n increased from 0.20 to 0.30, with V_{th} moving from −4.0 to −6.2 V, driven by enhanced polarization and carrier confinement. Similarly, increasing N_D from 1×10^{18} to 6×10^{18} cm^{-3} elevated n_s from 1.3×10^{13} to 1.4×10^{13} cm^{-2} and shifted V_{th} from −4.3 to −6.1 V, due to a higher supply of free electrons. The results obtained from this work closely match simulated data, confirming the validity of the model.

Keywords: HEMT, 2DEG, polarization, charge sheet density, threshold voltage

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1. INTRODUCTION

AlGaN/GaN HEMTs are favourable for high temperature, high frequency, high power, and high breakdown applications [1, 2] due to the strong polarization fields at the heterointerface of AlGaN and GaN. In addition to their significance for high-power and high-frequency transistors, GaN-based materials are also attractive for a wide range of other applications, including light-emitting diodes (LEDs) [3–7], terahertz (THz) devices [8], ultraviolet (UV) detectors [9], solar cells [10], and radiation-hardened electronics [11]. Recent studies have reported progress in stress analysis of GaN-based heterostructures on silicon [12]. Other works have explored bulk InGaN layer formation [13], mechanisms of optical gain in heavily doped AlGaN [14], normally-off GaN transistors [15], and p-channel GaN-based devices [16]. Collectively, these studies underline the versatility of GaN-based materials across optoelectronic, photovoltaic, and high-frequency domains, reinforcing their importance as a material platform for next-generation electronic and photonic devices. In comparison to other devices based on Group III–V compound semiconductors, GaN-based HEMTs may readily attain a value of n_s far beyond 10^{13} cm^{-2}. Strong bending of the conduction band and higher carrier concentration due to the substantial polarization field at the heterointerface lead to high n_s [17, 18]. Strong polarization fields, both P_{SP} and P_{PZ}, further improve these devices' func-

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Performance Trade-Offs and Optimization of Single and Dual-Layer Passivation AlGaN/GaN HEMTs with Double-Deck Gate Field Plate

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Abstract—This study presents a comprehensive evaluation of AlGaN/GaN-based high electron mobility transistors (HEMTs) with various passivation schemes, providing critical insights for device optimization. HfO_2-passivated devices exhibit superior breakdown characteristics, achieving a remarkable breakdown voltage (V_{br}) of 788 V, which confirms the advantage of high-k dielectrics in enhancing voltage withstand capability. In contrast, SiO_2-passivated HEMTs exhibit optimal radio frequency (RF) performance, including the highest cut-off frequency (f_T), which is attributed to their lower parasitic capacitance, making them ideal for high-frequency applications. This reflects a fundamental trade-off between breakdown strength and frequency response in HEMT devices. To overcome this limitation, a dual-passivation approach is investigated. Type-A exhibits superior DC performance, with higher drain saturation current (I_{dss}), transconductance (g_m), and V_{br}, owing to the stronger gate control and electric field modulation provided by the high-k HfO_2 top layer. Both dual-layer passivation schemes significantly enhance V_{br} (~798 V for Type-A, ~797 V for Type-B) compared to single-layer passivation. In RF analysis, Type-B (Si_3N_4 on top, HfO_2 below) outperforms Type-A. Although Type-A exhibits higher f_T up to 0.4 μm, thicker HfO_2 increases parasitic capacitances, degrading GFP, TFP, and GTFP. In contrast, Type-B improves with thicker Si_3N_4, validating the advantage of placing a low-k on top of a high-k dielectric. Considering composite FOMs (TFP, GFP, GTFP, V_{EA}, A_V), Type-B achieves superior overall RF performance.

Keywords: breakdown voltage, 2DEG, GaN HEMT, high-k passivation layer

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1. INTRODUCTION

AlGaN/GaN HEMTs are gaining prominence for applications in high-voltage switching and power conversion. This advantage stems from the remarkable features of GaN-based wide-bandgap materials, including high two-dimensional electron gas (2DEG) density, high saturation velocity, superior electron mobility, a wide bandgap, a strong breakdown field, and excellent thermal conductivity [1–3]. The distinctive properties of the III-nitride material system allow GaN-based HEMTs to deliver efficient performance in high-power, high-frequency, and high-temperature applications [4]. Consequently, III-nitride materials are now widely employed in light-emitting diodes (LEDs) [5–9], ultraviolet photodetectors [10], high electron mobility transistors (HEMTs) [11–14], and terahertz/optoelectronic devices [15]. Recent advancements further highlight their versatility, including optimized AlGaN/GaN HEMTs for biosensing applications [16], negative-capacitance and delta-doped structures for RF and Normally-Off operation [17, 18], and hybrid GaN/β-Ga_2O_3 FETs for wide-bandgap power switching [19, 20]. Recent years have seen notable advancements in GaN power devices, achieving reduced on-resistance and higher breakdown voltages [21–24]. Despite their promising performance, fundamental research on GaN remains crucial to achieve further advancements and optimization. Several techniques have been proposed to improve the V_{br} of HEMTs, including field plates (FPs) [25–27], Schottky source-drain contacts (SSD) [28], and passivation layers between the gate and drain [29]. In AlGaN/GaN HEMTs, the passivation layer extends from the gate to the source and from the gate to the drain, preventing current degradation and thereby enhancing device performance [30]. Since surface passivation is crucial in these devices, selecting an appropriate passivation material can further improve overall performance [31]. SiO_2, though widely used in MOSFETs, has a low dielectric con-

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ABSTRACT

MODELING AND PERFORMANCE ANALYSIS OF GAN BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT)

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ABSTRACT

Semiconductors power most modern digital technologies and are vital for emerging fields like autonomous driving, 5G, IoT, and AI. With heavy R&D investment, they continue to drive innovation, making devices smarter, faster, and more efficient. The International Semiconductor Technology Roadmap (ITRS) has long tracked challenges in Metal Oxide Semiconductor (MOS) technology, where continuous miniaturization enhances performance and circuit density. Following Moore's 1965 prediction that transistor density doubles every 18 months, the industry has pursued smaller, faster, and more efficient devices. However, scaling introduces short-channel effects (SCEs), leading to the development of advanced transistor structures such as HEMTs, HBTs, CN-FETs, FinFETs, and others with high-κ dielectrics and novel gate designs to sustain progress in integrated circuit technology. GaN-based HEMTs are leading candidates for high-power, high-frequency, and low-noise applications due to their high electron velocity, wide bandgap, strong polarization, and high breakdown field. These devices are a type of field-effect transistor (FET) featuring a compound semiconductor heterojunction, which enables an exceptional combination of low noise and high performance at microwave frequencies. HEMTs are essential components in high-speed and high-frequency digital circuits as well as low-noise microwave circuits, where no other technology can match their performance. Their versatile applications span computing, satellite broadcasting receivers, mobile communication systems, millimeter-wave automotive radar, GPS navigation, broadband wireless access, and precision instrumentation. Additionally, HEMTs are widely employed in radio frequency (RF) design, providing superior performance at very high RF frequencies.

This thesis presents a comprehensive study on the optimization of AlGaN/GaN HEMTs for high-power and high-frequency applications through a systematic analysis of field plate (FP) configurations, passivation techniques, and barrier layer engineering. The research aims to elucidate and improve the inherent trade-offs between breakdown voltage (V_{br}), transconductance (g_m), cut-off frequency (f_T), and overall device reliability, with the objective of attaining an optimal balance

between voltage robustness and high-speed performance in GaN-based power devices. Various FP configurations—namely gate-connected, source-connected, and drain-connected structures—were examined to assess their influence on electric field distribution and breakdown behavior. The results indicate that gate-connected FPs consistently exhibit better breakdown performance than both source-connected and drain-connected designs. Among the various novel FP designs investigated, double-deck gate-FP structures exhibited the highest V_{br} improvement due to effective electric field modulation around the gate edge. However, these designs also introduced increased parasitic capacitance, which limited high-frequency performance. The findings underscore a critical trade-off between V_{br} enhancement and RF characteristics, suggesting that optimized FP placement near the gate region can provide significant performance benefits without excessive degradation of f_T. Additionally, the inclusion of HfO_2 passivation demonstrated a remarkable enhancement in V_{br} by smoothing electric field peaks and mitigating impact ionization effects.

After this, a passivation engineering was explored in depth using single- and dual-layer dielectric materials. Comparative analyses of passivated devices (from SiO_2 to HfO_2) indicated that HfO_2-based structures achieved superior breakdown performance ($V_{br} \approx 788$ V), whereas SiO_2-passivated devices exhibited the best RF characteristics due to reduced parasitic capacitance. To combine these benefits, dual-layer passivation stacks were proposed and evaluated as Type-A (HfO_2/Si_3N_4) and Type-B (Si_3N_4/HfO_2) structures. Type-A devices provided higher V_{br} (~798 V) and superior DC performance due to stronger gate control, while Type-B offered improved RF figures of merit, confirming the effectiveness of using a low-k dielectric as the top layer over a high-k material. These results establish that both material choice and layer ordering critically influence the overall DC and RF behavior of GaN HEMTs.

This thesis further explored barrier-layer engineering employing InAlN, InAlGaN, and AlGaN alloys to enhance the two-dimensional electron gas (2DEG) density and improve carrier transport characteristics. Both dual- and triple-material symmetric and asymmetric barrier structures were investigated to optimize current

handling and voltage capability. Among them, the triple-material symmetric barrier (InAlGaN/InAlN/AlGaN) at 17 nm thickness demonstrated the most balanced performance, delivering a high drain current (I_{dss} = 2.96 A/mm) and V_{br} (569 V), surpassing conventional AlGaN/GaN and InAlN/GaN HEMTs. This configuration effectively harnesses the polarization benefits of multiple alloys, establishing it as a promising design for next-generation ultra-high-power electronic devices.

After this, a Normally-Off Si_3N_4-passivated AlGaN/GaN HEMT with a double-deck gate field plate (FP) structure was analyzed for optimized performance. Parametric variations in FP lengths (L_{G_FP}, L_{S_FP}, L_{D_FP}) and source–drain spacing (L_{SD}) revealed that precise geometric tuning significantly enhances breakdown voltage (V_{br}) while maintaining acceptable frequency response. The optimized configuration achieved a record V_{br} of 1717 V and low on-resistance (R_{on}) of 2.38 Ω·mm, confirming its suitability for high-voltage switching applications

Finally, an analytical model was developed to accurately predict 2DEG sheet charge density (n_s) and threshold voltage (V_{th}) variations with Al mole fraction, barrier thickness, and doping concentration. The model accounts for both spontaneous and piezoelectric polarization effects and shows excellent agreement with simulation results. The analysis confirms that increasing Al content, barrier thickness, or doping density enhances n_s while making V_{th} more negative, providing valuable insight into design dependencies for V_{th} control in GaN HEMTs.

Overall, this thesis provides a comprehensive framework for optimizing GaN-based HEMTs through coordinated FP, passivation, and barrier engineering strategies. The proposed designs and modeling approaches contribute to the advancement of high-efficiency, high-voltage, and high-frequency GaN transistor technologies, thereby extending their applicability to next-generation power electronics and RF systems.